Advanced Micro Devices

Linear and Interface Data Book

4102517

Advanced Micro Devices

Linear and Interface Data Book

Section I

NUMERIC INDEX

NUMERIC INDEX (Cont.)

FUNCTIONAL INDEX

Section 1

Comparators – Section II

Application Notes

Data Conversion Products – Section III

Application Notes

Line Drivers/Receivers – Section IV

Line Drivers/Receivers – Section IV (Cont.)

Line Drivers/Receivers — Section IV (Cont.)

MOS Memory and Microprocessor Interface — Section V

Operational Amplifiers — Section VI

Operational Amplifiers – Section VI (Cont.)

Special Functions – Section VII

Voltage Regulators – Section VIII

Section IX

SELECTION GUIDE

OPERATIONAL AMPLIFIERS

UNCOMPENSATED

	Page No.	
LM101	6-1	General Purpose, 500nA I_B, 5mV Vos
LM748	6-84	General Purpose, 500nA I_B, 5mV Vos
LM101A	6-5	Improved General Purpose, 75nA I_B, 2mV Vos
AM1501	6-90	Dual Improved General Purpose, 75nA I_B, 2mV Vos
LH2101A	6-99	Dual Improved General Purpose, 75nA I_B, 2mV Vos
725	6-59	Instrumentation, 100nA I_B, 1mV Vos, 5.0V/°C TCVIO
SSS725	6-64	Improved Instrumentation, 80nA I_B, .5mV Vos, 1.0V/°C TCVIO
LM108	6-18	Low Input Current Precision, 2nA I_B, 2mV Vos, 0.2nA IOS
LM108A	6-18	Low Input Current and Offset Voltage Precision, 2nA I_B, 0.5mV Vos, 0.2nA IOS, 5μV/°C TCVIO
715	6-55	High Speed, 15V/μsec slew rate, 750nA I_B, 5mV Vos

INTERNALLY COMPENSATED

741	6-70	General Purpose, 500nA I_B, 5mV Vos
741A,E	6-70	Improved General Purpose, 80nA I_B, 3mV Vos, 30nA I_{OS}, 50μV/VPSRR
SSS741	6-64	High Performance, 50nA I_B, 2mV Vos
747	6-77	Dual General Purpose, 500nA I_B, 5mV Vos
747A,E	6-77	Dual Improved General Purpose, 80nA I_B, 3mV Vos, 30nA I_{OS}, 50μV/VPSRR
SSS747	6-64	Dual High Performance, 50nA I_B, 2mV Vos
AM1558	6-95	Dual General Purpose, 500nA I_B, 5mV Vos
LM124	6-36	Quad General Purpose, 150nA I_B, 5mV
LM124A	6-36	Vos, Single or Dual Supply, 3 to 30V, 1mW/op amp at +5V
LM148	6-41	Quad 741, 500nA I_B, 5mV Vos
LM149	6-41	Quad Decompensated, 500nA I_B, 5mV Vos $A_{V(min.)} = 5$
LM107	6-14	Improved General Purpose, 75nA I_B, 2mV Vos
LM112	6-26	Low Input Current Precision, 2nA I_B, 2mV Vos
LM216	6-51	Very Low Input Current Precision, 150pA I_B, 10mV Vos
LM216A	6-51	Very Low Input Current Precision, 50pA I_B, 3mV Vos
LM118	6-30	High Speed, 50V/μsec slew rate, 4mV Vos, 250nA I_B
LF155	6-43	FET Input General Purpose, 5mV Vos, 20pA I_{OS}, 100pA I_B
LF155A	6-43	FET Input General Purpose, 2mV Vos, 5μV/°C TC V_{IO}, 10pA I_{OS}, 50pA I_B
LF156	6-43	FET Input Wideband, 5mV Vos, 20pA I_{OS}, 100pA I_B, 7.5V/μsec SR
LF156A	6-43	FET Input Wideband, 2mV Vos, 5μV/°C TC V_{IO}, 10pA I_{OS}, 50pA I_B, 10V/μsec SR
LF157	6-43	FET Input Wideband Decompensated, 5mV Vos, 20pA I_{OS}, 100pA I_B, 30V/μsec SR ($A_V = 5$)
LF157A	6-43	FET Input Wideband Decompensated, 2mV Vos, 5μV/°C TC V_{IO}, 10pA I_{OS}, 50pA I_B, 40V/μsec SR ($A_V = 5$)

VOLTAGE FOLLOWERS

	Page No.	
LM102	6-10	Low Input Current, High Speed, 10nA I_B, 5mV Vos, 20V/μsec slew rate, $10^{10}\Omega$ Rin
LM110	6-22	Improved Low Input Current, High Speed, 3nA I_B, 4mV Vos, 20V/μsec slew rate, $10^{10}\Omega$ Rin

VOLTAGE COMPARATORS

	Page No.	
LM111	2-5	General Purpose, 100nA I_B, 3mV Vos, 250ns Response Time, 50V and 50mA Output
LH2111	2-35	Dual General Purpose, 100nA I_B, 3mV Vos, 250ns Response Time, 50V and 50mA Output
AM1500	2-31	Dual General Purpose, 100nA I_B, 3mV Vos, 250ns Response Time, 50V and 50mA Output
LM106	2-1	High Speed, 20μA I_B, 2mV Vos, 40ns Response Time, 24V and 100mA Output
LM119	2-9	Dual General Purpose, 500nA I_B, 4mV Vos, 80ns Response Time, 35V and 25mA Output, +5 or +15V Supply
LM139	2-13	Quad General Purpose, 100nA I_B, 2mV
LM139A	2-13	Vos, Single or Dual Supply 2 to 36V, 1mW/comp. at +5V
AM685	2-19	Very Fast ECL Output, 10μA I_B, 2mV Vos, 6.5ns Response Time
AM686	2-27	Very Fast TTL Output, 10μA I_B, 2mV Vos, 12ns Response Time
AM687	2-29	Dual Very Fast ECL Output, 10μA I_B, 2mV Vos, 6.5ns Response Time

VOLTAGE REGULATORS

	Page No.	
723	8-5	General Purpose, 2-37V Output, 0.15% load reg., 50V input, 150mA Output
LM105	8-1	General Purpose, 4.5-40V Output, 0.05% load reg., 50V input, 12mA Output

DATA CONVERSION PRODUCTS

	Page No.	
AM1508	3-14	8-Bit Multiplying D-to-A Converter, Accuracy 0.19%, Settling Time 300nsec typ.
SSS1508A	3-14	8-Bit Multiplying D-to-A Converter, Accuracy 0.1%, Settling Time 135nsec
DAC-08	3-1	8-Bit High-Speed Multiplying D/A Converter
AM6070	3-28	Companding D-to-A Converter for Control Systems
AM6071	3-40	Companding D-to-A Converter for Control Systems
AM6072	3-52	Companding D-to-A Converter for PCM Communication Systems
AM6073	3-64	Companding D-to-A Converter for PCM Communication Systems
AM6080	3-76	Microprocessor System Compatible 8-Bit High-Speed Multiplying D/A Converter
AM6081	3-84	Microprocessor System Compatible 8-Bit High-Speed Multiplying D/A Converter
LF198, 298, 398	3-7	Monolithic Sample and Hold Circuits
AM2502, 03, 04	3-18	8-Bit/12-Bit Successive Approximation Registers

SELECTION GUIDE (Cont.)

LINE DRIVERS

DUAL DIFFERENTIAL		Use With
75109	Open collector differential outputs typical current 6mA, inhibit controls	75107B 75108B
75110	12mA output current version of Am75109	75107B 75108B
8830	Designed for single 5.0V supply operation	7820 or 7820A
8831	Dual differential device which may also be used as a quad single-ended driver. Three-state output.	9615 or 2615
8832	Similar to 8831 but no V_{CC} clamp diodes	9615 or 2615
9614	5 volt supply driver with complementary outputs	9615
9621	200mA transient capability with 130Ω back matching resistor	9620
DIFFERENTIAL EIA RS-422, FEDERAL STD 1020		
26LS31	Quad, high-speed, low output skew	26LS32 or
26LS30	Dual, high output CMR	26LS33
SINGLE ENDED		
2614	High-speed quad driver for multi-channel, common ground operation.	2615
SINGLE ENDED, EIA RS-232-C		
1488	Quad EIA RS-232C driver (14 pins)	1489/ 1489A
2616	Quad 16-pin driver for EIA RS-232C, CCITT V.24 and MIL-188C interface	2617
9616	Triple EIA RS-232C driver (14 pins)	9617
SINGLE ENDED, EIA RS-423, FEDERAL STD 1030		
26LS29	Quad, three-state	26LS32 or
26LS30	Quad, mode control	26LS33

BUS BUFFERS/DRIVERS

		t_{pd} (TYP)	I_{OL} (MAX)
25LS240 74LS240 74S240 81LS96	Inverting octal buffer/driver with three-state output	10 10 4.5 9.0	48 24 68 16
25LS241 74LS241 74S241 81LS95	Non-inverting octal buffer/driver with three-state output	12 12 6.0 12	48 24 68 16
25LS242 74LS242 †74S242	Inverting buffer/driver with two quad data paths connected input-to-output	10 10 4.5	48 24 68
25LS243 74LS243 †74S243	Non-inverting buffer/driver with two quad data paths connected input-to-output	12 12 6.0	48 24 68
25LS244 74LS244 74S244 81LS97	Non-inverting octal buffer/driver with three-state output and two inverting enables	12 12 6.0 12	48 24 68 16
81LS98	Inverting octal buffer/driver with three-state output and two inverting enables	9.0	16

†In development

LINE RECEIVERS

DUAL DIFFERENTIAL		Use With
3603	Receiver with differential input to detect signals > 25mV. Three-state outputs.	75110
75107B	Totem-pole TTL output version of Am363	75109 or 75110
75108B	Open collector TTL output version of Am363	75109 or 75110
8820	Designed for ±15V common mode using 5.0V supply	8830
8820A	Higher speed, tighter spec 8820	8830
9615	±15 volt common mode, 5 volt supply receivers with uncommitted collector and active pull-up controls	9614
9620	±15 volt common mode receiver with direct and attenuated inputs	9621
QUAD DIFFERENTIAL		
26LS33	±15 volt common mode, 5 volt supply, three-state output	26LS31
QUAD DIFFERENTIAL EIA RS-422, FEDERAL STD 1020		
26LS32	±7 volt common mode, 5 volt supply, three-state output	26LS31
SINGLE ENDED		
2615	Receiver for 3 volt single-ended TTL level data	2614
SINGLE ENDED, EIA RS-232-C		
1489	Quad EIA RS-232C receiver with input threshold hysteresis	1488
1489A	Higher threshold version of Am1489	1488
2617	Quad EIA RS-232 receiver specified over military temperature range (same pinout as Am1489A)	2616
9617	Triple EIA RS-232 receiver with adjustable hysteresis	9616
SINGLE ENDED, EIA RS-423, FEDERAL STD 1030		
26LS32	±7 volt common mode, 5 volt supply, three-state output	26LS29 26LS30

SPECIAL FUNCTIONS

TIMERS	
555	Single, Precision oscillator/timer
556	Dual version 555

MOS MEMORY

DRIVERS	
0026	Dual 5MHz Two-Phase MOS clock driver
0056	0026 with added V_{BB} terminal
SENSE AMPLIFIERS	
3604	Differential input for signals > 10mV, Three-state outputs
75207	Totem-pole TTL output 3604
75208	Open-collector 3604

MOS-MICROPROCESSOR INTERFACE CIRCUITS

8080A/9080A	
8212	8-Bit input/output port, with storage
8216	4-Bit parallel bidirectional bus driver
8224	Clock generator and driver
8226	Inverting version 8216
8228	System controller and bus driver
8238	System controller and bus driver with extended IOW/MEMW
8303B	Two 8226's in one 20 pin package
8304B	Two 8216's in one 20 pin package

BUS TRANSCEIVERS

Device	Output	Function	Hysteresis	Speed (Note 1)	Comments
QUAD					
Am26S10	100mA-O.C.	Inverting	No	20ns	SN55/75138 pin out
Am26S11	100mA-O.C.	Non-Inverting to bus; Inverting off bus	No	22ns	Same as Am26S10 except non-inverting to bus
Am26S12	100mA-O.C.	Inverting	Yes-0.6V	32ns	Same pin out as DS78/8838 and 8T38
Am26S12A	100mA-O.C.	Inverting	Yes-1.05V	32ns	Wider threshold Am26S12
Am2905	100mA-O.C.	Inverting	No	31ns (Note 2)	Has 2-input multiplexer
Am2906	100mA-O.C.	Inverting	No	31ns (Note 2)	Has 2-input multiplexer and parity
Am2907	100mA-O.C.	Inverting	No	31ns (Note 2)	Includes parity, 2.0V receiver V_{TH}
Am2908	100mA-O.C.	Inverting	No	31ns (Note 2)	Includes parity, 1.5V receiver V_{TH}
Am2915A	48mA/3-St.	Inverting	No	31ns (Note 2)	Has 2-input multiplexer
Am2916A	48mA/3-St.	Inverting	No	31ns (Note 2)	Has 2-input multiplexer and parity
Am2917A	48mA/3-St.	Inverting	No	31ns (Note 2)	Includes parity
Am3216	50mA/3-St.	Non-Inverting	No	34ns	Same as 8216 except different A.C. loading spec
Am3226	50mA/3-St.	Inverting	No	30ns	Same as 8216 except different A.C. loading spec
Am3448A	48mA/3-St.-O.C.	Non-Inverting	Yes	32ns	IEEE 488 compatible
Am78/8838	50mA-O.C.	Inverting	No	38ns	Same pin out and function as Am26S12A and 8T38
Am8T26A	48mA/3-St.	Inverting	No	19ns	V_{OH} MOS compatible
Am8T28	48mA/3-St.	Non-Inverting	No	25ns	V_{OH} MOS compatible
Am8216	50mA/3-St.	Non-Inverting	No	34ns	Similar to 8T28
Am8226	50mA/3-St.	Non-Inverting	No	30ns	Similar to 8T26A
OCTAL					
Am8303B	48mA/3-St.	Inverting	No	14ns	Same as two 8226's in one 20 pin package
Am8304B	48mA/3-St.	Non-Inverting	No	24ns	Same as two 8216's in one 20 pin package

Notes: 1. Typical delay at 28°C for input to bus plus receiver to output.
2. Bus enable to bus plus bus to receiver output. All parts include register or driver plus receiver with latch.

SELECTION GUIDE (Cont.)

MONOSTABLES (ONE SHOTS)

Device No.	Description	Dual	Retrig-gerable	Reset Table	Initial Accuracy %	Min. Output t_{pw}(ns)	Pulse Width Variation (%) Temp.	V_{CC}	Power Dissipation (mW typ.)	No. Package Leads
Am2600	t_{pw} = 55ns to ∞, with guaranteed < 1% change over temperature range	X	X	X	±10	45	±0.5	±1.5	95	14
Am2602	t_{pw} = 55ns to ∞, with guaranteed < 1% change over temperature range	X	X	X	±10	45	±0.5	±1.5	175	16
Am26L02	Low-Power version 2602, t_{pw} = 100ns to ∞	X	X	X	±10	110	±0.3	±1.0	50	16
Am26L123	Low-Power version 26123, t_{pw} = 120ns to ∞	X	X	X	±10	120	±0.3	±1.0	60	16
Am26S02	High speed Schottky version 2602, t_{pw} = 28ns to ∞	X	X	X	±5.0	33	±0.4	±1.5	240	16
Am26123	t_{pw} = 45ns to ∞, with guaranteed < 1% change over temperature range. Output stability latch improves noise immunity	X	X	X	±10	45	±0.5	±0.5	230	16
Am54/74123	Same as 26123, except no output latch, no Δt_{pw} guarantee	X	X	X	±10	45	±2.7	±1.0	230	16
Am54/74221	Schmitt-trigger input	X		X	±7.0	30	±0.3	±0.3	130	16
Am9600	Same as 2600, except no Δt_{pw} guarantee		X	X	±10	50	±1.5	±1.5	95	14
Am9601	Non-resettable version of 9600, t_{pw} = 55ns to ∞		X		±10	45	±2.7	±1.0	95	14
Am9602	Same as 2602, except t_{pw} = 60ns to ∞, no Δt_{pw} guarantee	X	X	X	±10	50	±1.5	±1.5	175	16
Am96L02	Same as 26L02, except t_{pw} guaranteed <1.6% change over temperature range	X	X	X	±10	110	±0.3	±0.5	50	16

INDUSTRY CROSS REFERENCE

	AMD*	Fairchild	Intel	Motorola	National	Signetics	Texas Instruments
Manufacturer Identification Cross Reference							
	AM	µA, or None	None	M,MC	DM, DS, LM, MH	None	SN
Temperature Range Cross Reference							
Commercial	C	C	–	14, 34, 88	3, 86, 88	NE, N	72, 74, 75
Military	M	M	M	15, 35, 96	1, 96, 78	SE, S	52, 54, 55
Package Cross Reference							
Hermetic DIP	D	D	C, D	L	D	F, I	J
Molded DIP	P	P	P	P_2	N	A, B	N
Mini-Molded DIP	T	T	–	P_1	N	V	P
Flat Pack	F	F	–	F	F, W	W, Q	H, U, Z, W
TO-5 Type Can	H	H	–	G, R	H	DB, K, T	L
TO-8 Type Can	G	–	–	H	G	–	–

*The original manufacturers' part number and package code are used for second source devices.

FAIRCHILD

9614 D M

9614 — Device Type; D — Package Type; M — Temperature Range

Fairchild	AMD Direct Replacement	AMD Functional Replacement
µA101D	LM101D	
µA101H	LM101H	
µA101AD	LM101AD	
µA101AF	LM101AF	
µA101AH	LM101AH	
µA102H	LM102H	
µA105H	LM105H	
µA107H	LM107H	
µA108AH	LM108AH	
µ108H	LM108H	
µA110H	LM110H	
µA111H	LM111H	
µA139D	LM139D	
µA1458H	AM1458H	
µA1558H	AM1558H	
µA201D	LM201D	
µA201H	LM201H	
µA201AD	LM201AD	
µA201AF	LM201AF	
µA201AH	LM201AH	
µA207H	LM207H	
µA208H	LM208H	
µA208AH	LM208AH	
µA301AD	LM301AD	
µA301AH	LM301AH	
µA301AN	LM301AN	
µA302H	LM302H	
µA305H	LM305H	
µA305AH	LM305AH	
µA307H	LM307H	
µA308H	LM308H	
µA308AH	LM308AH	
µA310H	LM310H	
µA311H	LM311H	

FAIRCHILD (Cont.)

µA 556 D M

µA — Mfg.'s Ident.; 556 — Device Type; D — Package Type; M — Temperature Range

Fairchild	AMD Direct Replacement	AMD Functional Replacement
µA311P	LM311N	
µA339D	LM339D	
µA339P	LM339N	
µA715DC	715DC	
µA715DM	715DM	
µA715HC	715HC	
µA715HM	715HM	
µA723DC	723DC	
µA723DM	723DM	
µA723HC	723HC	
µA723HM	723HM	
µA725HC	725HC	
µA725HM	725HM	
µA725PC	725CN	
µA733DC	733DC	
µA733DM	733DM	
µA733FM	733FM	
µA733HC	733HC	
µA733HM	733HM	
µA741DC	741DC	
µA741DM	741DM	
µA741FM	741FM	
µA741HC	741HC	
µA741HM	741HM	
µA741ADM	741ADM	
µA741AFM	741AFM	
µA741AHM	741AHM	
µA741EDC	741EDC	
µA741EHC	741EHC	
µA747DC	747DC	
µA747DM	747DM	
µA747HC	747HC	
µA747HM	747HM	
µA747PC	747PC	

FAIRCHILD (Cont.)

Fairchild	AMD Direct Replacement	AMD Functional Replacement
µA747ADM	747ADM	
µA747AHM	747AHM	
µA747EDC	747EDC	
µA747EHC	747EHC	
µA748DC	748DC	
µA748DM	748DM	
µA748FM	748FM	
µA748HC	748HC	
µA748HM	748HM	
µA748PC	748PC	
µA760DC		AM686DC
µA760DM		AM686DM
µA760HC		AM686HC
µA760HM		AM686HM
µA775DM	LM139D	
µA775DC	LM339D	
µA775PC	LM339N	
54123DM	SN54123J	
54123FM	SN54123W	
55107ADM	SN55107BJ	
55107BDM	SN55107BJ	
55107AFM	SN55107BW	
55107BFM	SN55107BW	
55108ADM	SN55108BJ	
55108AFM	SN55108BW	
55108BDM	SN55108BJ	
55108BFM	SN55108BW	
55109DM	SN55109J	
55109FM	SN55109W	
55110DM	SN55110J	
55110FM	SN55110W	
5520DM	SN5520J	
5521DM	SN5521J	
55234DM	SN55234J	
55234FM	SN55234W	
55235DM	SN55235J	
55235FM	SN55235W	
55238DM	SN55238J	
55238FM	SN55238W	
55239DM	SN55239J	
55239FM	SN55239W	
5524DM	SN5524J	
5525DM	SN5525J	
55325DM	SN55325J	
55325FM	SN55325W	
74123DC	SN74123J	
74123PC	SN74123N	
75107ADC	SN75107BJ	
75107APC	SN75107BN	
75107BDC	SN75107BJ	
75107BPC	SN75107BN	
75108ADC	SN75108BJ	
75108APC	SN75108BN	
75108BDC	SN75108BJ	
75108BPC	SN75108BN	
75109DC	SN75109J	
75109PC	SN75109N	
75110DC	SN75110J	
75110PC	SN75110N	

FAIRCHILD (Cont.)

Fairchild	AMD Direct Replacement	AMD Functional Replacement
9600DC	9600DC	
9600DM	9600DM	
9600FM	9600FM	
9600PC	9600PC	
9601DC	9601DC	
9601DM	9601DM	
9601FM	9601FM	
9601PC	9601PC	
9602DC	9602DC	
9602DM	9602DM	
9602FM	9602FM	
9602PC	9602PC	
96L02DC	96L02DC	
96L02DM	96L02DM	
96L02FM	96L02FM	
96L02PC	96L02PC	
96S02DC		AM26S02DC
96S02PC		AM26S02PC
9614DC	9614DC	
9614DM	9614DM	
9614FM	9614FM	
9614PC	9614PC	
9615DC	9615DC	
9615DM	9615DM	
9615FM	9615FM	
9615PC	9615PC	
9616DC	9616DC	
9616DM	9616DM	
9616EDC	9616EDC	
9616EPC	9616EPC	
9616FM	9616FM	
9616PC	9616PC	
9617DC	9617DC	
9617PC	9617PC	
9634PC		AM26LS31PC
9634DC		AM26LS31DC
9634DM		AM26LS31DM
9635PC		AM26LS33PC
9635DC		AM26LS33DC
9635DM		AM26LS33DM
9636PC		AM26LS30PC
9636DC		AM26LS30DC
9636DM		AM26LS30DM
9637PC		AM26LS32PC
9637DC		AM26LS32DC
9637DM		AM26LS32DM
9638PC		AM26LS32PC
9638DC		AM26LS32DC
9638DM		AM26LS32DM
9640DC	AM26S10DC	
9640DM	AM26S10DM	
9640PC	AM26S10PC	
9641DC	AM26S11DC	
9641DM	AM26S11DM	
9641PC	AM26S11PC	
9642PC		AM26S12APC
9642DC		AM26S12ADC
9642DM		AM26S12ADM

INTEL

M D8228

Temperature Range — Package Type — Device Type

Intel	AMD Direct Replacement	AMD Functional Replacement
D3212	D3212	
MD3212	MD3212	
P3212	P3212	
D3216	D3216	N8T28F
MD3216	MD3216	S8T28F
P3216	P3216	N8T28B
D3226	D3226	N8T26F
MD3226	MD3226	S8T26F
P3226	P3226	N8T26B
D8212	D8212	
MD8212	AM8212DM	
P8212	AM8212PC	
D8216	D8216	N8T28F
MD8216	MD8216	S8T28F
P8216	P8216	N8T28B
D8224	D8224	
MD8224	AM8224DM	
P8224	AM8224PC	
D8226	D8226	N8T26F
	MD8226	MD8226
S8T26F	P8226	P8226
N8T26B	D8228	D8228
MD8228	AM8228DM	
P8228	AM8228PC	
D8238	D8238	
MD8238	AM8238DM	
P8238	AM8238PC	
D8286	DP8304BJ	
P3287	DP8304BN	
D8287	DP8303BJ	
P8287	DP8303BN	

MOTOROLA

MC 14 88 L

Mfg.'s Ident. — Temperature Range — Device Type — Package Type

Motorola	AMD Direct Replacement	AMD Functional Replacement
MC1408L6	AM1408L6	
MC1408L7	AM1408L7	
MC1408L8	AM1408L8	
MC1458G	AM1458H	
MC1488L	MC1488L	
MC1488P	AM1488PC	
MC1489L	MC1489L	
MC1489P	AM1489PC	
MC1489AL	MC1489AL	
MC1489AP	AM1489APC	
MC1508L8	AM1508L8	
MC1558G	AM1558H	
MC1723CG	723HC	
MC1723CL	723DC	
MC1723G	723HM	
MC1723L	723DM	
MC1733CG	733HC	
MC1733CL	733DC	

MOTOROLA (Cont.)

Motorola	AMD Direct Replacement	AMD Functional Replacement
MC1733F	733FM	
MC1733G	733HM	
MC1733L	733DM	
MC1741CG	741HC	
MC1741CL	741DC	
MC1741F	741FM	
MC1741G	741HM	
MC1741L	741DM	
MC1747CG	747HC	
MC1747CL	747DC	
MC1747G	747HM	
MC1747L	747DM	
MC1748CG	748HC	
MC1748G	748HM	
MC26S10L	AM26S10DC	
MC26S10P	AM26S10PC	
MC3438L		AM26S12ADC
MC3438P		AM26S12APC
MC3443L		AM26S10DC
MC3443P		AM26S10PC
MC3448AL	MC3448AL	
MC3448AP	MC3448AP	
MC3456L	NE556F	
MC3456P	NE556A	
MC3486L		AM26LS31DC
MC3486P		AM26LS31PC
MC3487L		AM26LS32DC
MC3487P		AM26LS32PC
MC3556L	SE556F	
MC55107L	SN55107BJ	
MC55108L	SN55108BJ	
MC55109L	SN55109J	
MC55110L	SN55110J	
MC5524L	SN5524J	
MC5525L	SN5525J	
MC55325L	SN55325J	
MC75107L	SN75107BJ	
MC75107P	SN75107BN	
MC75108L	SN75108BJ	
MC75108P	SN75108BN	
MC75109L	SN75109J	
MC75109P	SN75109N	
MC75110L	SN75110J	
MC75110P	SN75110N	
MC8T26L	N8T26F	
MC8T26P	N8T26B	
MC8601L	9601DC	
MC8601P	9601PC	
MC8602L	9602DC	AM2602DC
MC8602P	9602PC	AM2602PC
MC9601L	9601DM	
MC9602L	9602DM	AM2602DM
MLM101AG	LM101AH	
MLM105G	LM105H	
MLM107G	LM107H	
MLM110G	LM110H	
MLM111F	LM111F	
MLM111G	LM111H	
MLM111L	LM111D	
MLM201AG	LM210AH	
MLM205G	LM205H	
MLM207G	LM207H	
MLM210G	LM210H	
MLM211G	LM211H	

MOTOROLA (Cont.)

Motorola	AMD Direct Replacement	AMD Functional Replacement
MLM211L	LM211D	
MLM301AG	LM301AH	
MLM301API	LM301AN	
MLM305G	LM305H	
MLM307G	LM307H	
MLM310G	LM310H	
MLM311G	LM311H	
MLM211PI	LM311N	
MLM311L	LM311D	
MMH0026CG	MH0026CH	
MMH0026CL	MMH0026CL	
MMH0026CPI	MH0026CN	
MMH0026G	MH0026H	
MMH0026L	MMH0026L	

NATIONAL

DS 78 20 J

Mfg.'s Ident. — Temperature Range — Device Type — Package Type

National	AMD Functional Replacement	AMD Direct Replacement
DM54123J	SN54123J	
DM54123W	SN54123W	
DM54L123J		AM26L123DM
DM54L123W		AM26L123FM
DM71LS95J	DM71LS95J	SN54LS241J
DM71LS96J	DM71LS96J	SN54LS240J
DM71LS97J	DM71LS97J	SN54LS244J
DM71LS98J	DM71LS98J	SN54LS240J
DM74L123J		AM26L123DC
DM74L123N		AM26L123PC
DM74123J	SN74123J	AM26123DC
DM74123N	SN74123N	AM26123PC
DM81LS95J	DM81LS95J	SN74LS240J
DM81LS95N	DM81LS95N	SN74LS240N
DM81LS96J	DM81LS96J	SN74LS241J
DM81LS96N	DM81LS96N	SN74LS241N
DM81LS97J	DM81LS97J	SN74LS241J
DM81LS97N	DM81LS97N	SN74LS241N
DM81LS98J	DM81LS98J	SN74LS240J
DM81LS98N	DM81LS98N	SN74LS240N
DM8601J	9601DC	
DM8601N	9601PC	
DM8602J	9602DC	AM2602DC
DM8602N	9602PC	AM2602PC
DM9601J	9601DM	
DM9601W	9601FM	
DM9602J	9602DM	AM2602DM
DM9602W	9602FM	AM2602FM
DP7303BJ	DP7304BJ	
DP8303BJ	DP8303BJ	
DP8304BJ	DP8304BJ	
DS0026CG	MH0026CG	
DS0026CH	MH0026CH	
DS0026CJ	MMH0026CL	
DS0026CN	MH0026CN	
DS0026F	DS0026F	
DS0026G	MH0026G	
DS0026H	MH0026H	
DS0026J	MMH0026L	

NATIONAL (Cont.)

National	AMD Direct Replacement	AMD Functional Replacement
DS0056CG	DS0056CG	
DS0056CH	DS0056CH	
DS0056CJ	DS0056CJ	
DS0056CN	DS0056CN	
DS0056G	DS0056G	
DS0056H	DS0056H	
DS0056J	DS0056J	
DS1488J	MC1488L	
DS1488N	AM1488PC	
DS1489J	MC1489L	
DS1489N	AM1489L	
DS1489AJ	MC1489AL	
DS1489AN	AM1489APC	
DS1691J	AM26LS30DM	
DS1692J	DS1692J	
DS3691J	AM26LS30DC	
DS3691N	AM26LS30PC	
DS3692J	DS3692J	
DS3692N	DS3692J	
DS3692N	DS3692N	
DS7820J	DM7820J	
DS7820AJ	DM7820AJ	
DS7830J	DM7830J	
DS7831J	DM7831J	
DS7832J	DM7832J	
DS7835J		S8T26F
DS7838J	DS7838J	AM26S12ADM
DS8820J	DM8820J	
DS8820N	DM8820N	
DS8820AJ	DM8820AJ	
DS8820AN	DM8820AN	
DS8830J	DM8830J	
DS8830N	DM8830N	
DS8831J	DM8831J	
DS8831N	DM8831N	
DS8832J	DM8832J	
DS8832N	DM8832N	
DS8835J		N8T26F
DS8835N		N8T26B
DS8838J	DS8838J	AM26S12ADC
DS8838N	DS8838N	AM26S12APC
DS55107J	SN55107BJ	
DS55108J	SN55108BJ	
DS55109J	SN55109J	
DS55110J	SN55110J	
DS75107J	SN75107BJ	
DS75107N	SN75107BN	
DS75108J	SN75108BJ	
DS75108N	SN75108BN	
DS75109J	SN75109J	
DS75109N	SN75109N	
DS75110J	SN75110J	
DS75110N	SN75110N	
LF155H	LF155H	
LF155AH	LF155AH	
LF156H	LF156H	
LF156AH	LF156AH	
LF157H	LF157H	
LF157AH	LF157AH	
LF198H	LF198H	
LF255H	LF255H	
LF256H	LF256H	
LF257H	LF257H	
LF298H	LF298H	

NATIONAL (Cont.)

National	AMD Direct Replacement	AMD Functional Replacement
LF355H	LF355H	
LF355N	LF355N	
LF355AH	LF355AH	
LF356H	LF356H	
LF356N	LF356N	
LF356AH	LF356AH	
LF357H	LF357H	
LF357N	LF357N	
LF357AH	LF357AH	
LF398H	LF398H	
LH2101AD, J	LH2101AD	
LF2101AF	LH2101AF	
LF2111D, J	LH2111D	
LH2111F	LH2111F	
LH2201AD, J	LH2201AD	
LH2201AF	LH2201AF	
LH2211D, J	LH2211D	
LH2211F	LH2211F	
LH2301AD, J	LH2301AD	
LH2311D, J	LH2311D	
LM101D, J	LM101D	
LM101F	LM101F	
LM101H	LM101H	
LM101AD, J	LM101AD	
LM101AF	LM101AF	
LM101AH	LM101AH	
LM102D, J	LM102D	
LM102F	LM102F	
LM102H	LM102H	
LM105F	LM105F	
LM105H	LM105H	
LM106F	LM106F	
LM106H	LM106H	
LM107D, J	LM107D	
LM107F	LM107F	
LM107H	LM107H	
LM108D, J	LM108D	
LM108F	LM108F	
LM108H	LM108H	
LM108AD, J	LM108AD	
LM108AF	LM108AF	
LM108AH	LM108AH	
LM110D, J	LM110D	
LM110F	LM110F	
LM110H	LM110H	
LM111D, J	LM111D	
LM111F	LM111F	
LM111H	LM111H	
LM112D, J	LM112D	
LM112F	LM112F	
LM112H	LM112H	
LM118D, J	LM118D	
LM118F	LM118F	
LM118H	LM118H	
LM119D, J	LM119D	
LM119F	LM119F	
LM119H	LM119H	
LM124D, J	LM124D	
LM124F	LM124F	
LM139D, J	LM139D	
LM139AD, J	LM139AD	
LM139F	LM139F	
LM139AF	LM139AF	
LM148D	LM148D	

NATIONAL (Cont.)

National	AMD Direct Replacement	AMD Functional Replacement
LM149D	LM149D	
LM201H	LM201H	
LM201AD, J	LM201AD	
LM201AF	LM201AF	
LM201AH	LM201AH	
LM202H	LM202H	
LM205H	LM205H	
LM206H	LM206H	
LM207D, J	LM207D	
LM207F	LM207F	
LM207H	LM207H	
LM208AD, J	LM208AD	
LM208AF	LM208AF	
LM208AH	LM208AH	
LM208D, J	LM208D	
LM208F	LM208F	
LM208H	LM208H	
LM210D, J	LM210D	
LM210H	LM210H	
LM211D, J	LM211D	
LM211F	LM211F	
LM211H	LM211H	
LM212D, J	LM212D	
LM212F	LM212F	
LM212H	LM212H	
LM216D, J	LM216AD	
LM216AF	LM216AF	
LM216AH	LM216AH	
LM216D, J	LM216D	
LM216F	LM216F	
LM216H	LM216H	
LM218D, J	LM218D	
LM218F	LM218F	
LM218H	LM218H	
LM219D, J	LM219D	
LM219F	LM219F	
LM219H	LM219H	
LM224D, J	LM224D	
LM239D, J	LM239D	
LM239AD, J	LM239D	
LM248D	LM248D	
LM249D	LM249D	
LM301AD, J	LM301AD	
LM301AF	LM301AF	
LM301AH	LM301AH	
LM301AN	LM301AN	
LM302F	LM302F	
LM302H	LM302H	
LM305F	LM305F	
LM305H	LM305H	
LM305AH	LM305AH	
LM306F	LM306F	
LM306H	LM306H	
LM307D, J	LM307D	
LM307F	LM307F	
LM307H	LM307H	
LM308AD, J	LM308AD	
LM308AF	LM308AF	
LM308AH	LM308AH	
LM308AN	LM308AN	
LM308D, J	LM308D	
LM308F	LM308F	
LM308H	LM308H	
LM308N	LM308N	

NATIONAL (Cont.)

National	AMD Direct Replacement	AMD Functional Replacement
LM310D, J	LM310D	
LM310F	LM310F	
LM310H	LM310H	
LM310N	LM310N	
LM311D, J	LM311D	
LM311F	LM311F	
LM311N	LM311N	
LM312D, J	LM312D	
LM312F	LM312F	
LM312H	LM312H	
LM316AD, J	LM316AD	
LM316AF	LM316AF	
LM316AH	LM316AH	
LM316D, J	LM316D	
LM316F	LM316F	
LM316H	LM316H	
LM318D, J	LM318D	
LM318F	LM318F	
LM318H	LM318H	
LM318N	LM318N	
LM319H	LM319H	
LM319D, J	LM319D	
LM319N	LM319N	
LM324D, J	LM324D	
LM324N	LM324N	
LM339D, J	LM339D	
LM339AD, J	LM339AD	
LM339N	LM339N	
LM339AN	LM339AN	
LM348D	LM348D	
LM348N	LM348N	
LM349D	LM349D	
LM349N	LM349N	
LM723D, J	723DM	
LM723H	723HM	
LM723CD, J	723DC	
LM723CH	723HC	
LM725H	725HM	
LM725CH	725HC	
LM725CN	725CN	
LM725D, J	725DM	
LM725CD, J	725DC	
LM733D, J	733DM	
LM733H	733HM	
LM733CD, J	733DC	
LM733CH	733HC	
LM741D, J	741DM	
LM741F	741FM	
LM741H	741HM	
LM741CD, J	741DC	
LM741CF	741FC	
LM741CH	741HC	
LM747D, J	747DM	
LM747H	747HM	
LM747F	747FM	
LM747CD, J	747DC	
LM747CP	747PC	
LM747CH	747HC	
LM747CN	747PC	
LM478H	748HM	
LM748CH	748HC	
LM748CN	748PC	
LM1458H	AM1458H	
LM1558H	AM1558H	

SIGNETICS

NE — Temperature Range; 555 — Device Type; V — Package Type

Signetics	AMD Direct Replacement	AMD Functional Replacement
LM101F	LM101D	
LM101T	LM101H	
LM101AF	LM101AD	
LM101AT	LM101AH	
LM107F	LM107D	
LM107T	LM107H	
LM108F	LM108D	
LM108T	LM108H	
LM108AF	LM108AD	
LM108AT	LM108AH	
LM111F	LM111D	
LM111T	LM111H	
LM119H	LM119H	
LM119D	LM119D	
LM124F	LM124D	
LM139F	LM139D	
LM201T	LM301H	
LM201AF	LM201AD	
LM201AT	LM201AH	
LM201AV	LM201AN	
LM207F	LM207D	
LM207T	LM207H	
LM208F	LM208D	
LM208T	LM208H	
LM208AF	LM208AD	
LM208AT	LM208AH	
LM211F	LM211D	
LM211T	LM211H	
LM219H	LM219H	
LM219D	LM219D	
LM224F	LM224D	
LM239F	LM239D	
LM301AT	LM301AH	
LM301AV	LM301AN	
LM307F	LM307D	
LM307T	LM307H	
LM308F	LM308D	
LM308T	LM308H	
LM308V	LM308N	
LM308AF	LM308AD	
LM308AT	LM308AH	
LM311F	LM311D	
LM311T	LM311H	
LM311V	LM311N	
LM319H	LM319H	
LM319D	LM319D	
LM319A	LM319N	
LM324A	LM324N	
LM324F	LM324D	
LM339A	LM339N	
LM339F	LM339D	
MC1488F	MC1488L	
MC1489F	MC1489L	
MC1489AF	MC1489AL	
NE529K		AM686HC
NE592K	AM592HC	
N74123B	SN74123N	
N74123F	SN74123J	
N74221B	SN74221N	
N74221F	SN74221J	

SIGNETICS (Cont.)

Signetics	AMD Direct Replacement	AMD Functional Replacement
N8T22A	9601PC	
N8T22F	9601DC	
N8T26B	N8T26B	
N8T26F	N8T26F	
N8T26AB	N8T26AB	
N8T26AF	N8T26AF	
N8T28B	N8T28B	
N8T28F	N8T28F	
N8T38B		DS8838N
N8T38F		DS8838J
N9602B	9602PC	
N9602F	9602DC	
SE529K		AM686HM
SE555T	SE555T	
SE556F	SE556F	
SE592A	AM592PC	
SE592K	AM592HM	
S54123F	SN54123J	
S54221F	SN54221J	
S9602F	9602DM	
S8T26F	S8T26F	
S8T26AF	S8T26AF	
S8T28F	S8T28F	
S8T38F		DS7838J
μA723CF	723DC	
μA723CL	723HC	
μ723F	723DM	
μA723L	723HM	
μA733CA	733PC	
μA733CF	733DC	
μA733CK	733HC	
μA733F	733DM	
μA733K	733HM	
μA741CF	741DC	
μA741CT	741HC	
μA741F	741DM	
μA741T	741HM	
μA747CA	747PC	
μA747CF	747DC	
μA747CK	747HC	
μA747F	747DM	
μA747K	747HM	
μA748CT	748HC	
μA748F	748DM	
μA748T	748HM	

TEXAS INSTRUMENTS

SN	75	110	N
Mfg.'s Ident.	Temperature Range	Device Type	Package Type

Texas Instruments	AMD Direct Replacement	AMD Functional Replacement
SN52101AJ	LM101AD	
SN52101AL	LM101AH	
SN52101AZ	LM101AF	
SN52105L	LM105H	
SN52106FA	LM106F	
SN52106L	LM106H	
SN52107J	LM107D	
SN52107L	LM107H	

TEXAS INSTRUMENTS (Cont.)

Texas Instruments	AMD Direct Replacement	AMD Functional Replacement
SN52107Z	LM107F	
SN52108AFA	LM108AF	
SN52108AJA	LM108AD	
SN52108AL	LM108AH	
SN52108FA	LM108F	
SN52108JA	LM108D	
SN52108L	LM108H	
SN52111FA	LM111F	
SN52111J	LM111D	
SN52111L	LM111H	
SN52118FA	LM118F	
SN52118JA	LM118D	
SN52118L	LM118H	
SN52723J	723DM	
SN52723L	723HM	
SN52733FA	733FM	
SN52733J	733DM	
SN52733L	733HM	
SN52741FA	741FM	
SN52741JA	741DM	
SN52741L	741HM	
SN52747FA	747FM	
SN52747JA	747DM	
SN52747L	747HM	
SN52748FA	748FM	
SN52748JA	748DM	
SN52748L	748HM	
SN54L123J		AM26L123DM
SN54L123W		AM26L123FM
SN54LS123J	SN54LS123L	AM25LS123AM
SN54LS123W	SN54LS123W	AM25LS123FM
SN54LS240J	SN54LS240J	AM25LS240DM
SN54LS241J	SN54LS241J	AM25LS241DM
SN54LS242J	SN54LS242J	AM25LS242DM
SN54LS243J	SN54LS243J	AM25LS243DM
SN54LS244J	SN54LS244J	AM25LS244DM
SN54S240J	SN54S240J	
SN54S241J	SN54S241J	
SN54123J	SN54123J	AM26123DM
SN54123W	SN54123W	AM26123DM
SN54221J	SN54221J	
SN54221W	SN54221W	
SN55107AJ	SN55107BJ	
SN55107BJ	SN55107BJ	
SN55108AJ	SN55108BJ	
SN55108BJ	SN55108BJ	
SN55109J	SN55109J	
SN55110J	SN55110J	
SN55114J	9614DM	
SN55114W	9614FM	
SN55115J	9615DM	
SN55115W	9615DM	
SN55182J	DM7820AJ	
SN55182W	DM7820AW	
SN55183J	DM7830J	
SN55183W	DM7830W	
SN55369J	MMH0026L	
SN72301AJ	LM301AD	
SN72301AL	LM301AH	
SN72305L	LM305H	
SN72306L	LM306H	
SN72307J	LM307D	
SN72307L	LM307H	
SN72308AJA	LM308AD	

TEXAS INSTRUMENTS (Cont.)

Texas Instruments	AMD Direct Replacement	AMD Functional Replacement
SN72308AL	LM308AH	
SN72308JA	LM308D	
SN72308L	LM308H	
SN72311J	LM311D	
SN72311L	LM311H	
SN72318JA	LM318D	
SN72318L	LM318H	
SN72723J	723DC	
SN72723L	723HC	
SN72733J	733DC	
SN72733L	733HC	
SN72741JA	741DC	
SN72741L	741HC	
SN72747JA	747DC	
SN72747L	747HC	
SN72748JA	748DC	
SN72748L	748HC	
SN74L123J		AM26L123DC
SN74L123N		AM26L123PC
SN74LS123J	SN74LS123J	AM25LS123DC
SN74LS123N	SN74LS123N	AM25LS123PC
SN74LS240J	SN74LS240J	AM25LS240DC
SN74LS240N	SN74LS240N	AM25LS240PC
SN74LS241J	SN74LS241J	AM25LS241DC
SN74LS241N	SN74LS241N	AM25LS241PC
SN74LS242J	SN74LS242J	AM25LS242DC
SN74LS242N	SN74LS242N	AM25LS242PC
SN74LS243J	SN74LS243J	AM25LS243DC
SN74LS243N	SN74LS243N	AM25LS243PC
SN74LS244J	SN74LS244J	AM25LS244DC
SN74LS244N	SN74LS244N	AM25LS244PC
SN74LS424J	D8224	
SN74LS424N	P8224	
SN74S240J	SN74S240J	
SN74S240N	SN74S240N	
SN74S241J	SN74S241J	

TEXAS INSTRUMENTS (Cont.)

Texas Instruments	AMD Direct Replacement	AMD Functional Replacement
SN74S241N	SN74S241N	
SN74S412J	D8212	
SN74S412	P8212	
SN74123J	SN74123J	AM26123DC
SN74123N	SN74123N	AM26123PC
SN74221J	SN74221J	
SN74221N	SN74221N	
SN75107AJ	SN74107BJ	
SN75107AN	SN75107BN	
SN75107BJ	SN75107BJ	
SN75107BN	SN75107BN	
SN75108AJ	SN75108BJ	
SN75108AN	SN75108BN	
SN752108BJ	SN75108BJ	
SN75108BN	SN75108BN	
SN75109J	SN75109J	
SN75109N	SN75109N	
SN75110J	SN75110J	
SN75110N	SN75110N	
SN75114J	9614DC	
SN75114N	9614PC	
SN75115J	9615DC	
SN75115	9615PC	
SN75182J	DM8820AJ	
SN75182N	DM8820AN	
SN75183J	DM8830J	
SN75183N	DM8830N	
SN75188J	MC1488L	
SN75188N	AM1488PC	
SN75189J	MC1489L	
SN75189N	AM1489PC	
SN75189AJ	MC1489AL	
SN75189AN	AM1489APC	
SN75369J	MMH0026CL	
SN75369P	MH0026CN	

DICE POLICY

Advanced Micro Devices, interface and linear products are all available in dice form.

ELECTRICAL CHARACTERISTICS

Each die is electrically tested to the commercial or military grade DC parameters to guardbanded limits at 25°C to guarantee operation over the temperature range.

QUALITY ASSURANCE

All dice are 100% visually inspected to the requirements of MIL-STD-883A, Method 2010.2, condition B.

All dice are glass passivated with only the bonding pads exposed to provide scratch protection. All dice are provided without gold backing.

SHIPPING PACKAGES/ORDER INFORMATION

All dice are packaged in containers with individual compartments which prevent damage to the die during shipping.

Minimum order for AMD dice is 10 pcs.

SPECIAL CHIP PROCESSING

If there is a need for additional testing or processing, contact AMD for detailed information.

See following pages on ordering information for detail ordering number.

ORDERING INFORMATION

DEVICE NUMBER	ORDER NUMBER 0°C to +70°C				ORDER NUMBER −55°C to +125°C			
	Metal Can	Hermetic DIP	Molded DIP	Dice	Metal Can	Hermetic DIP	Flat Pak	Dice
Am592	AM592HC	AM592DC	AM592PC	AM592XC	AM592HM	AM592DM		AM592XM
Am685*	AM685HL	AM685DL		AM685XL	AM685HM	AM685DM·		AM685XM
Am686	AM686HC	AM686DC		AM686XC	AM686HM	AM686DM		AM686XM
Am687*		AM687DL		AM687XL		AM687DM		AM687XM
Am1500		AM1500DC				AM1500DM	AM1500FM	
*						AM1500DL	AM1500FL	
Am1501		AM1501DC				AM1501DM	AM1501FM	
*						AM1501DL	AM15091FL	
Am1508		AM1408L8				AM1508L8		
		AM1408L7						
		AM1408L6						
Am1558	AM1458H				AM1558H			
Am25 Series								
Am2502		AM2502DC	AM2502PC	AM2502XC		AM2502DM	AM2502FM	AM2502XM
Am2503		AM2503DC	AM2503PC	AM2503XC		AM2503DM	AM2503FM	AM2503XM
Am2504		AM2504DC	AM2504PC	AM2504XC		AM2504DM	AM2504FM	AM2504XM
Am25L02		AM25L02DC	AM25L02PC	AM25L02XC		AM25L02DM	AM25L02FM	AM25L02XM
Am25L03		AM25L03DC	AM25L03PC	AM25L03XC		AM25L03DM	AM25L03FM	AM25L03XM
Am25L04		AM25L04DC	AM25L04PC	AM25L04XC		AM25L04DM	AM25L04FM	AM25L04XM
Am25LS240		AM25LS240DC	AM25LS240PC	AM25LS240XC		AM25LS240DM	AM25LS240FM	AM25LS240XM
Am25LS241		AM25LS241DC	AM25LS241PC	AM25LS241XC		AM25LS241DM	AM25LS241FM	AM25LS241XM
Am25LS242		AM25LS242DC	AM25LS242PC	AM25LS242XC		AM25LS242DM	AM25LS242FM	AM25LS242XM
Am25LS243		AM25LS243DC	AM25LS243PC	AM25LS243XC		AM25LS243DM	AM25LS243FM	AM25LS243XM
Am25LS244		AM25LS244DC	AM25LS244PC	AM25LS244XC		AM25LS244DM	AM25LS244FM	AM25LS244XM
Am26 Series								
Am2600		AM2600DC	AM2600PC	AM2600XC		AM2600DM	AM2600FM	AM2600XM
Am2602		AM2602DC	AM2602PC	AM2602XC		AM2602DM	AM2602FM	AM2602XM
Am2614		AM2614DC	AM2614PC	AM2614XC		AM2614DM	AM2614FM	AM2614XM
Am2615		AM2615DC	AM2615PC	AM2615XC		AM2615DM	AM2615FM	AM2615XM
Am2616		AM2616DC	AM2616PC	AM2616XC		AM2616DM	AM2616FM	AM2616XM
Am2617		AM2617DC	AM2617PC	AM2617XC		AM2617DM	AM2617FM	AM2617XM
Am26123		AM26123DC	AM26123PC	AM26123XC		AM26123DM	AM26123FM	AM26123XM
Am26LS29		AM26LS29DC	AM26LS29PC	AM26LS29XC		AM26LS29DM	AM26LS29FM	AM26LS29XM
Am26LS30		AM26LS30DC	AM26LS30PC	AM26LS30XC		AM26LS30DM	AM26LS30FM	AM26LS30XM
Am26LS31		AM26LS31DC	AM26LS31PC	AM26LS31XC		AM26LS31DM	AM26LS31FM	AM26LS31XM
Am26LS32		AM26LS32DC	AM26LS32PC	AM26LS32XC		AM26LS32DM	AM26LS32FM	AM26LS32XM
Am26LS33		AM26LS33DC	AM26LS33PC	AM26LS33XC		AM26LS33DM	AM26LS33FM	AM26LS33XM
Am26L02		AM26L02DC	AM26L02PC	AM26L02XC		AM26L02DM	AM26L02FM	AM26L02XM
Am26L123		AM26L123DC	AM26L123PC	AM26L123XC		AM26L123DM	AM26L123FM	AM26L123XM
Am26S02		AM26S02DC	AM26S02PC	AM26S02XC		AM26S02DM	AM26S02FM	AM26S02XM
Am26S10		AM26S10DC	AM26S10PC	AM26S10XC		AM26S10DM	AM26S10FM	AM26S10XM
Am26S11		AM26S11DC	AM26S11PC	AM26S11XC		AM26S11DM	AM26S11FM	AM26S11XM
Am26S12		AM26S12DC	AM26S12PC	AM26S12XC		AM26S12DM	AM26S12FM	AM26S12XM
Am26S12A		AM26S12ADC	AM26S12APC	AM26S12AXC		AM26S12ADM	AM26S12AFM	AM26S12AXM
Am29 Series								
Am2905		AM2905DC	AM2905PC	AM2905XC		AM2905DM	AM2905FM	AM2905XM
Am2906		AM2906DC	AM2906PC	AM2906XC		AM2906DM	AM2906FM	AM2906XM
Am2907		AM2907DC	AM2907PC	AM2907XC		AM2907DM	AM2907FM	AM2907XM
Am2908		AM2908DC	AM2908PC	AM2908XC		AM2908DM	AM2908FM	AM2908XM
Am2915A		AM2915ADC	AM2915APC	AM2915AXC		AM2915ADM	AM2915AFM	AM2915AXM
Am2916A		AM2916ADC	AM2916APC	AM2916AXC		AM2916ADM	AM2916AFM	Am2916AXM
Am2917A		AM2917ADC	AM2917APC	AM2917AXC		AM2917ADM	AM2917AFM	AM2917AXM
Am32XX Series								
Am3212		D3212	P3212	AM8212XC		MD3212		
Am3216		D3126	P3216	AM8212XC		MD3216		
Am3226		D3226	P3226	AM8226XC		MD3226		
Am6070		AM6070DC	AM6070PC	6070XC		AM6070DM	Am6071	
Am6072								
Am6073								
Am6080		AM6080DC	AM6080PC	6080XC		AM6080DM		
Am6081		AM6081DC	6081PC	6081XC		AM6081DM		
*		AMDAC-08EQ				AMDAC-08AQ		
DAC-08		AMDAC-08CQ				AMDAC-08Q		
DM, DP or DS Series								
DS0056 (8 pin)	DS0056CH		DS0056CN	AM0056CX	DS0056H			AM0056X
DS0056 (12 pin)	DS0056CG				DS0056G			
DS0056 (14 pin)		DS0056J				DS0056J		
DS16/3692		DS3692J	DS3692N			DS1692J	DS1692W	
DM71/81LS95		DM81LS95N	DM81LS95J	AM81LS95X		DM71LS95J	DM71LS95W	AM71LS95X
DM71/81LS96		DM81LS96N	DM81LS96J	AM81LS96X		DM71LS96J	DM71LS96W	AM71LS96X
DM71/81LS97		DM81LS97N	DM81LS97J	AM81LS97X		DM71LS97J	DM71LS97W	AM71LS97X
DM71/81LS98		DM81LS98N	DM81LS98J	AM81LS98X		DM71LS98J	DM71LS98W	AM71LS98X
DM78/8820		DM8820J	DM8820N	AM8820X		DM7820J	DM7820W	AM7820X
DM78/8820A		DM8820AJ	DM8820AN	AM8820AX		DM7820AJ	DM7820AW	AM7820AX
DM78/8830		DM8830J	DM8830N	AM8830X		DM7830J	DM7830W	AM7830X
DM78/8831		DM8831J	DM8831N	AM8831X		DM7831J	DM7831W	AM7831X
DM78/8832		DM8832J	DM8832N	AM8832X		DM7832J	DM7832W	AM7832X
†DM73/8303B		DP8303BJ	DP8303BN	AM8303BX		DP7303BJ	DP7303BW	AM7303BX
DP73/8304B		DP8304BJ	DP8304BN	AM8304BX		DP7304BJ	DP7304BW	AM7304BX
DS78/8838		DS8838J	DS8838N			DS7838J	DS7838W	

ORDERING INFORMATION (Cont.)

DEVICE NUMBER	ORDER NUMBER 0°C to +70°C				ORDER NUMBER −55°C to +125°C			
	Metal Can	Hermetic DIP	Molded DIP	Dice	Metal Can	Hermetic DIP	Flat Pak	Dice
LH2101A		LH2301AD			LH2101AD	LH2101AF		
LM101	LM301H	LM301D	LM301N	LD301	LM101H	LM101D	LM101F	LD101
•			LM201N		LM201H	LM201D	LM201F	
LM101A	LM301AH	LM301AD	LM301AN	LD301A	LM101AH	LM101AD	LM101AF	LD101A
•			LM201AN		LM201AH	LM201AD	LM201AF	
LM102	LM302H	LM302D		LD302	LM102H	LM102D	LM102F	LD102
•					LM202H	LM202D	LM202F	
LM105	LM305H			LD305	LM105H			LD105
•	LM305AH				LM205H			
LM106	LM306H	LM306D		LD306	LM106H		LM106F	LD106
•					LM206H		LM206F	
LM107	LM307H	LM307D		LD307	LM107H	LM107D	LM107F	LD107
•					LM207H	LM207D	LM207F	
LM108	LM308H	LM308D	LM308N	LD308	LM108H	LM108D	LM108F	LD108
•					LM208H	LM208D	LM208F	
LM108A	LM308AH	LM308AD	LM308AN	LD308A	LM108AH	LM108AD	LM108AF	LD108A
•					LM208AH	LM208AD	LM208AF	
LM110	LM310H	LM310D	LM310N	LD310	LM110H	LM110D	LM110F	LD110
•					LM210H	LM210D	LM210F	
LM111	LM311H	LM311D	LM311N	LD311	LM111H	LM111D	LM111F	LD111
•					LM211H	LM211D	LM211F	
LM112	LM312H	M312D		LD312	LM112H	LM112D	LM112F	LD112
•					LM212H	LM212D	LM212F	
LM118	LM318H	LM318D	LM318N	LD318	LM118H	LM118D	LM118F	LD118
•					LM218H	LM218D	LM218F	
LM119	LM319H	LM319D	LM319N	LD319	LM119H	LM119D	LM119F	LD119
•					LM219H	LM219D	LM219F	
LM124		LM324D	LM324N	LD324		LM124D	LM124F	LD124
•						LM224D	LM224F	
LM124A		LM324AD	LM324AN	LD324A		LM124AD	LM124AF	LD124A
•					LM224AD	LM224AF		
LM139		LM339D	LM339N	LD339		LM139D	LM139F	LD139
•						LM239D	LM239F	
LM139A		LM339AD	LM339AN	LD339A		LM139AD	LM139AF	LD139A
•						LM239AD	LM239AF	
LM148		LM348D	LM348N	LD348		LM148D		LD148
•					LM248D			
LM149		LM349D	LM349N	LD349		LM149D		LD149
•						LM249D		
LF155	LF355H		LF355N	LD355	LF155H			LD155
•					LF225H			
LF155A	LF355AH			LD355A	LF155AH			LD155A
•								
LF156	LF356H		LF356N	LD356	LF156H			LD156
•					LF256H			
LF16A	LF356AH			LD356A	LF156AH			LD156A
•								
LF157	LF357H		LF357N	LD357	LF157H			LD157
•					LF257H			
LF157A	LF357AH			LD357A	LF157AH			LD157A
•								
LF198	LF398H			LD398	LF198H			LD198
•					LF298H			
LM216	LM316H	LM316D		LD316				
•					LM216H	LM216D	LM216F	LD216
LM216A	LM316AH	LM316AD		LD316A				
•					LM216AH	LM216AD	LM216AF	LD216A
MC1488		MC1488L	AM1488PC	AM1488XC				
MC1489		MC1489L	AM1489PC	AM1489XC				
MC1489A		MC1489AL	AM1489APC	AM1489AXC				
MC3448A		MC3448AL	MC3448APC	AM3448X				
MH0026 (8 pin)	MH0026CH		MH0026CN	AM0026CX	MH0026H			AM0026X
MH0026 (12 pin)	MH0026CG				MH0026G			
MH0026 (14 pin)		MMH0026CL				MMH0026L	DS0026F	

ORDERING INFORMATION (Cont.)

DEVICE NUMBER	ORDER NUMBER 0°C to +70°C				ORDER NUMBER −55°C to +125°C			
	Metal Can	Hermetic DIP	Molded DIP	Dice	Metal Can	Hermetic DIP	Flat Pak	Dice
SN54/74 Series								
SN54/74123		SN74123J	SN74123N	AM74123X		SN54123J	SN54123W	AM54123X
SN54/74221		SN74221J	SN74221N	Am74221X		SN54221J	SN54221W	AM54221X
SN54/74LS240		SN74LS240J	SN74LS240N	AM74LS240X		SN54LS240J	SN54LS240W	AM54LS240X
SN54/74LS241		SN74LS241J	SN74LS241N	AM74LS241X		SN54LS241J	SN54LS241W	AM54LS241X
SN54/74LS242		SN74LS242J	SN74LS242N	AM74LS242X		SN54LS242J	SN54LS242W	AM54LS242X
SN54/74LS243		SN74LS243J	SN74LS243N	AM74LS243X		SN54LS243J	SN54LS243W	AM54LS243X
SN54/74LS244		SN74LS244J	SN74LS244N	AM74LS244X		SN54LS244J	SN54LS244W	AM54LS244X
SN54/74S240		SN74S240J	SN74S240N	AM74S240X		SN54S240J		AM54S240X
SN54/74S241		SN74S241J	SN74S241N	AM74S241X		SN54S241J		AM54S241X
†SN54/74S242		SN74S242J	SN74S242N	AM74S242X		SN54S242J		AM54S242X
SN54/74S243		SN74S243J	SN74S243N	AM74S243X		SN54S243J		AM54S243X
SN54/74S244		SN74S244J	SN74S244N	AM74S244X		SN54S244J		AM54S244X
SN55/75 Series								
SN55/75107B		SN75107BJ	SN75107BN	AM75107BX		SN55107BJ		AM55107BX
SN55/75108B		SN75108BJ	SN75108BN	AM75108BX		SN55108BJ		AM55108BX
SN55/75109		SN75109J	SN75109N	AM75109X		SN55109J		AM55109X
SN55/75110		SN75110J	SN75110N	AM75110X		SN55110J		AM55110X
715	715HC	715DC		715XC	715HM	715DM		715XM
723	723HC	723DC	723PC	723XC	723HM	723DM		723XM
SSS725	SSS725CJ	SSS725CP			SSS725J	SSS725P		
733	733HC	733DC		733XC	733HM	733DM	733FM	733XM
741	741HC	741DC	741XC	741HM	741DM	741FM	741XM	
741A	741EHC	741EDC			741AHM	741ADM	741AFM	
SSS741	SSS741CJ				SSS741J			
747	747HC	747DC	747PC	747XC	747HM	747DM	747FM	747XM
747A	747EHC	747EDC			747AHM	747ADM	747AFM	
SSS747	SSS747CK	SSS747CP			SSS747K	SSS747P	SSS747M	
748	748HC	748DC	748PC	748XC	748HM	748DM	748FM	748XM
8XXX Series								
8T26		N8T26F	N8T26B	AM8T26X		S8T26F		AM8T26X
8T26A		N8T26AF	N8T26AB	AM8T26AX		S8T26AF		AM8T26AX
8T28		N8T28F	N8T28B	AM8T28X		S8T28F		AM8T28X
8212		D8212	P8212	AM8212XC		AM8212DM		
8216		D8216	P8216	AM8216XC		AM8216DM		
8224		D8224	AM8224PC	AM8224XC		AM8224DM		
Am8224-4		AM8224-4DC						
8226		D8226	AM8226PC	AM8226XC		AM8226DM		
8228		D8228	AM8228PC	AM8228XC		AM8226DM		
8238		D8238	AM8238PC	AM8238XC		AM8238DM		
Am8238-4		AM8238-4DC	AM8238-4PC					
96 Series								
9600		9600DC	9600PC	AM9600XC		9600DM	9600FM	AM9600XM
9601		9601DC	9601PC	AM9601XC		9601DM	9601FM	AM9601XM
9602		9602DC	9602PC	AM9602XC		9602DM	9602FM	AM9602XM
9614		9614DD	9614PC	AM9614XC		9614DM	9614FM	AM9614XM
9615		9615DC	9615PC	AM9615XC		9615DM	9615FM	AM9615XM
9616		9616DC	9616PC	AM9616XC		9616DM		
9617		9617DC	9617PC	AM9617XC		9617DM		AM9617XM
96L02		96L02DC	96L02PC	AM96L02XC		96L02DM	96L02FM	AM96L02XM

PRODUCT ASSURANCE
MIL-M-38510 • MIL-STD-883

The product assurance program at Advanced Micro Devices defines manufacturing flow, establishes standards and controls, and confirms the product quality at critical points. Standardization under this program assures that all products meet military and government agency specifications for reliable ground applications. Further screening for users desiring flight hardware and other higher reliability classes is simplified because starting product meets all initial requirements for high-reliability parts.

The quality standards and screening methods of this program are equally valuable for commercial parts where equipment must perform reliably with minimum field service.

Two military documents provide the foundation for this program. They are:

MIL-M-38510 – General Specification for Microcircuits
MIL-STD-883 – Test Methods and Procedures for Microelectronics

MIL-M-38510 describes design, processing and assembly workmanship guidelines for military and space-grade integrated circuits. All circuits manufactured by Advanced Micro Devices for full temperature range (−55°C to +125°C) operation meet these quality requirements of MIL-M-38510.

MIL-STD-883 defines detail testing and inspection methods for integrated circuits. Three of the methods are quality and processing standards directly related to product assurance:

Test Method 2010 defines the visual inspection of integrated circuits before sealing. By confirming fabrication and assembly quality, inspection to this standard assures the user of reliable circuits in long-term field applications. Standard inspection at Advanced Micro Devices includes all the requirements of the latest revision of Method 2010, condition B.

Test Method 5004 defines three reliability classes of parts. All must receive certain basic inspection, preconditioning and screening stresses. The classes are:

Class C – Used where replacement can be readily accomplished. Screening steps are given in the AMD processing flow chart.

Class B – Used where maintenance is difficult or expensive and where reliability is vital. Devices are upgraded from Class C to Class B by 160-hour burn-in at 125°C followed by more extensive electrical measurements. All other screening requirements are the same.

Class S – Used where replacement is extremely difficult and reliability is imperative. Class S screening selects extra reliability parts by expanded visual and X-ray inspection, further burn-in, and tighter sampling inspection.

All hermetically sealed integrated circuits (military and commercial) manufactured by Advanced Micro Devices are screened to MIL-STD-883, Class C. Molded integrated circuits receive Class C screening except that centrifuge and hermeticity steps are omitted.

Optional extended processing to MIL-STD-883, Class B is available for all AMD integrated circuits. Parts procured to this screening are marked with a "−B" following the standard part number, except that linear 100, 200 or 300 series are suffixed "/883B".

Test Method 5005 defines qualification and quality conformance procedures. Subgroups, tests and quality levels are given for Group A (electrical), Group B (mechanical quality related to the user's assembly environment), Group C (die related tests) and Group D (package related tests). Group A tests are always performed; Group B, C and D may be specified by the user.

MANUFACTURING, SCREENING AND INSPECTION FOR INTEGRATED CIRCUITS

All integrated circuits are screened to MIL-STD-883, Method 5004, Class C; quality conformance inspection where required is performed to Class B quality levels on either Class B or Class C product.

All full-temperature-range (−55°C to +125°C) circuits are manufactured to the workmanship requirements of MIL-M-38510.

The flow chart identifies processing steps as they relate to MIL-STD-883 and MIL-M-38510.

STANDARD PROCESSING CLASS C Steps 1 Through 25

HERMETIC PACKAGE PROCESS

MOLDED PACKAGE PROCESS

1 **INSPECTION**

Purchased or fabricated starting materials are inspected for conformance to specified requirements. Inspection follows written procedures, and records are analyzed for supplier quality negotiations.

2 **WAFER FABRICATION**

Repeated masking, etching and diffusion processes produce finished dice in wafer form.

3 **IN-PROCESS INSPECTION**

Each wafer is inspected prior to irreversible process steps.

4 **FINISHED WAFER INSPECTION**

Sample wafers from each finished diffusion lot are inspected to confirm lot quality before release for test and assembly.

5 **WAFER ELECTRICAL TEST**

Electrical probe test of every die. A computer-controlled system measures static and dynamic parameters and identifies dice that do not meet electrical requirements.

6 **DIE SEPARATION**

Wafers are separated into individual dice and electrical rejects are removed.

7 **VISUAL INSPECTION**

Separated dice are inspected and selected at high magnification.

8 **QUALITY INSPECTION**

Decisions at the 100% inspection are reviewed through periodic random sampling, confirming product quality and revealing any need for operator retraining.

9 **DIE ATTACH**

10 **QUALITY INSPECTION**

Strength of die attachment, position of die and visual quality of eutectic wetting are confirmed periodically by inspecting random samples and push-testing the attached dice.

11 **WIRE BOND**

Hermetic: Aluminum wires, ultrasonic bonding.
Molded: Gold wires, thermocompression bonding.

12 **QUALITY INSPECTION**

Weld strength, bond size and position, wire dress and general workmanship are confirmed periodically by comparing random samples with assembly instructions and quality standards. Bond strength is plotted on statistical control charts, providing early warning of process drifts.

13 **INTERNAL VISUAL INSPECTION**

Assembled but unsealed units are individually inspected at low and high power.

QUALITY STANDARDS:

All devices – MIL-STD-883, Method 2010, Condition B (latest revision).
Full temperature devices – MIL-M-38510, Para. 3.7 for workmanship (rebonding limits).

14 **QUALITY INSPECTION**

Decisions at the 100% inspection are reviewed through periodic random sampling, providing confirmation of product quality and revealing any need for operator retraining.

15a **FINAL SEAL**

(Hermetic devices)

15b **ENCAPSULATE**

(Molded Devices)

16 **HIGH TEMPERATURE STORAGE**

MIL-STD-883, Method 1008, Cond. C: 150°C, 24 hr

17 **TEMPERATURE CYCLE**

MIL-STD-883, Method 1010, Cond. C: –65°C, +150°C, 10 cycles

18 **CENTRIFUGE**

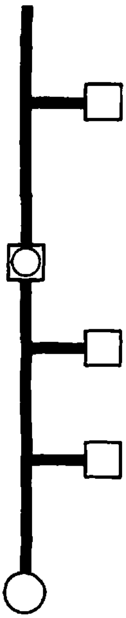
MIL-STD-883, Method 2001, Cond. E: 30,000 G

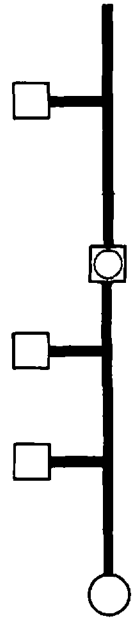
19 **SEAL (HERMETICITY) TEST**

MIL-STD-883, Method 1014, Cond. A or B: Fine Leak
MIL-STD-883, Method 1014, Cond. C2: Gross Leak

20 **ELECTRICAL TEST**

MIL-STD-883, Method 5004, Para. 3.1.12: Static, dynamic, functional tests at 25°C or in certain products at the most critical extreme temperature to assure accuracy of device selection.





21 **QUALITY GROUP A ELECTRICAL TEST (TABLE I)**

MIL-STD-883, Method 5005. See the table below. Quality levels as defined for Class B are applied to both Class B and Class C parts. Proven correlations supported by periodic reconfirmation may be used for some parameters.

22 **MARK, INSPECT, PACK FOR SHIPMENT**

23 **QUALITY INSPECTION, PRE-SHIPMENT**

Confirmation of marking, physical quality, and product identity.

24 **QUALITY INSPECTION FOR SHIPMENT RELEASE**

Confirmation of product type, count, package.
Confirmation of completion of all process requirements.
Confirmation of required documentation.

25 **SHIP TO CUSTOMER**

This AMD standard product meets screening requirements of MIL-STD-883, Class C.

GROUP A ELECTRICAL TESTS
From MIL-STD-883, Method 5005, Table I

Subgroups	LTPD (Note 1)	Initial Sample Size
Subgroup 1 – Static tests at 25°C	5	45
Subgroup 2 – Static tests at maximum rated operating temperature	7	32
Subgroup 3 – Static tests at minimum rated operating temperature	7	32
Subgroup 4 – Dynamic tests at 25°C – Linear devices	5	45
Subgroup 5 – Dynamic tests at maximum rated operating temperature – Linear devices	7	32
Subgroup 6 – Dynamic tests at minimum rated operating temperature – Linear devices	7	32
Subgroup 7 – Functional tests at 25°C	5	45
Subgroup 8 – Functional tests at maximum and minimum rated operating temperatures	10	22
Subgroup 9 – Switching tests at 25°C – Digital devices	7	32
Subgroup 10 – Switching tests at maximum rated operating temperature – Digital devices (Note 2)	10	10
Subgroup 11 – Switching tests at minimum rated operating temperature – Digital devices (Note 2)	10	10

1. Sampling plans are based on LTPD tables of MIL-M-38510. The smaller initial sample size, based on zero rejects allowed, has been chosen unless otherwise indicated. If necessary, the sample size will be increased once to the quantity corresponding to an acceptance number of 2. The minimum reject number in all cases is 3.
2. These subgroups are usually performed during initial device characterization only.

OPTIONAL EXTENDED PROCESSING
CLASS B
Steps 101 Through 110

Advanced Micro Devices offers several extended processing options to meet customer high-reliability requirements. These are defined in AMD document 00-003. The flow chart below outlines Option B, a 160-hr burn in. Military temperature range devices processed to this flow (in the left column) meet the screening requirements of MIL-STD-883, Class B.

MILITARY RANGE HERMETIC PACKAGES

COMMERCIAL RANGE HERMETIC OR MOLDED PACKAGES

101 **BEGINNING MATERIAL**

Standard product taken after completion of step 20 (electrical test)

102 **BURN IN**

MIL-STD-883, Method 1015: 160 hr, 125°C, or time-temperature equivalents as allowed by Method 1015.

103 **FINAL ELECTRICAL TEST**

MIL-STD-883, Method 5004.

Military: Testing subgroups as defined for Class B. Static and functional at 3 temperatures, dynamic or switching at room temperature.

Commercial: Repeat step 20.

104 **QUALITY GROUP A ELECTRICAL SAMPLE (TABLE I)**

MIL-STD-883, Method 5005 and Table I. Quality levels as defined for Class B. Temperature correlations may be used on commercial products.

105 **QUALITY CONFORMANCE TESTS, GROUPS B, C, AND D**

MIL-STD-883, Method 5005. Sample life and environmental tests if required by purchase order. Further information on specifying this is given in AMD document 00-003.

106 **DATA PREPARATION AND REVIEW**

107 **MARK, INSPECT, PACK FOR SHIPMENT**

Standard AMD parts with this burn-in option are marked with "–B" after the part number, except that linear 100, 200 or 300 series are suffixed "/883B".

108 **QUALITY INSPECTION, PRE-SHIPMENT**

Confirmation of marking, physical quality, and product identity.

109 **QUALITY INSPECTION FOR SHIPMENT RELEASE**

Final review of shipment against order.

110 **SHIP TO CUSTOMER**

Military temperature range parts meet screening requirements of MIL-STD-883, Class B.

OTHER OPTIONS

Document 00-003, "Extended Processing Options", further defines Option B as well as other screening or sampling options available or special order. Available options are listed here for reference.

Option	Description	Effect
A	Modified Class A screen (Similar to Class S screening)	Provides space-grade product, following most Class S requirements of MIL-STD-883, Method 5004.
B	160-hr operating burn in	Upgrades a part from Class C to Class B.
X	Radiographic inspection (X-ray)	Related to Option A. Provides limited internal inspection of sealed parts.
S	Scanning Electron Microscope (SEM) metal inspection	Sample inspection of metal coverage of die.
V	Preseal visual inspection to MIL-STD-883, Method 2010, Cond. A	More stringent visual inspection of assemblies and die surfaces prior to seal.
P	Particle impact noise (PIN) screen with ultrasonic detection.	Detects loose particles of approximately 0.5 mil size or larger, which could affect reliability in zero-G or high vibration applications.
Q	Quality conformance inspection (Group B, C and D life and environmental tests)	Samples from the lot are stressed and tested per Method 5005. The customer's order must state which groups are required. Group B destroys 16 devices; Group C, 92 devices; Group D, 60 devices.

Comparators – Section II

Application Notes

Am106/206/306

Voltage Comparator/Buffer

Distinctive Characteristics

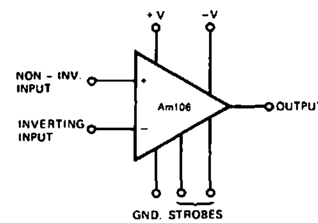
- *Functionally*, electrically, and pin-for-pin equivalent to the National LM 106/206/306
- Drives RTL, DTL or TTL directly
- Output can switch voltages up to 24 V @ 100 mA
- Fan-out of 10 with DTL or TTL
- 100% reliability assurance testing in compliance with MIL STD 883.
- Electrically tested and optically inspected die for assemblers of hybrid products.
- Available in metal can and hermetic flat package.

2

FUNCTIONAL DESCRIPTION

The Am106/206/306 are high-speed voltage comparators/buffers designed to be used in applications where high accuracy and fast response times are required. The device is useful as a pulse-height discriminator, relay or lamp driver or a line receiver.

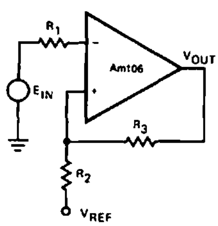
FUNCTIONAL DIAGRAM



LIC-072

APPLICATION

Level Detector With Hysteresis



LIC-073

Upper and Lower Trip Points:

$$V_{UT} = V_{REF} + \frac{R_2\,[V_{0\,MAX} - V_{REF}]}{R_2 + R_3}$$

and

$$V_{LT} = V_{REF} + \frac{R_2\,[V_{0\,MIN} - V_{REF}]}{R_2 + R_3}$$

$$\text{Hysteresis} = V_H = V_{UT} - V_{LT}$$

$$= \frac{R_2\,[V_{0\,MAX} - V_{0\,MIN}]}{R_2 + R_3}$$

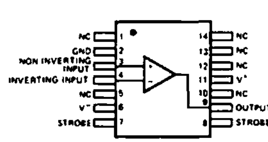
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am306	Metal Can	0°C to +70°C	LM306H
	Dice	0°C to +70°C	LD306
Am206	Metal Can	–25°C to +85°C	LM206H
Am106	Metal Can	–55°C to +125°C	LM106H
	Flat Pak	–55°C to +125°C	LM106F
	Dice	–55°C to +125°C	LD106

CONNECTION DIAGRAMS

Top Views

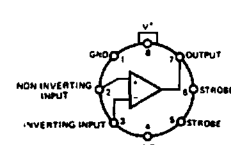
Flat Package



LIC-074

Note: Pin 6 connected to bottom of package.

Metal Can



LIC-075

Note: Pin 4 connected to case.

MAXIMUM RATINGS

Positive Supply Voltage	15 V
Negative Supply Voltage	−15 V
Output Voltage	24 V
Output to Negative Supply Voltage	30 V
Differential Input Voltage	±5 V
Input Voltage	±7 V
Power Dissipation (Note 1)	600 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	
Am106	−55°C to +125°C
Am206	−25°C to +85°C
Am306	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 60 sec)	300°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified) (Note 2)

Parameter (see definitions)	Conditions	Am306 Min	Am306 Typ	Am306 Max	Am106 Am206 Min	Am106 Am206 Typ	Am106 Am206 Max	Units
Input Offset Voltage	Note 3		1.6	5.0		0.5	2.0	mV
Input Offset Current	Note 3		1.8	5.0		0.7	3.0	μA
Input Bias Current			16	25		10	20	μA
Voltage Gain			40			40		V/mV
Response Time	Note 4		30	40		30	40	ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{sink} = 100$ mA		0.8	2.0		1.0	1.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $8\text{ V} \leq V_{OUT} \leq 24$ V		0.02	2.0		0.02	1.0	μA
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	Note 3			6.5			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$T_{A(min)} \leq T_A \leq T_{A(max)}$		5.0	20		3.0	10	μV/°C
Input Offset Current	$T_A = T_{A(max)}$		0.6	5.0		0.25	3.0	μA
	Note 3, $T_A = T_{A(min)}$		2.4	7.5		1.8	7.0	μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{A(max)}$		15	50		5.0	25	nA/°C
	$T_{A(min)} \leq T_A \leq 25°C$		24	100		15	75	nA/°C
Input Bias Current				40			45	μA
Input Voltage Range	$-7\text{ V} \geq V^- \geq -12$ V	±5.0			±5.0			V
Differential Input Voltage Range		±5.0			±5.0			V
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{sink} = 50$ mA			1.0			1.0	V
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{sink} \leq 16$ mA			0.4			0.4	V
Positive Output Level	$V_{IN} \geq 5$ mV, $I_{OUT} = 400$ μA	2.5		5.5	2.5		5.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $8\text{ V} \leq V_{OUT} \leq 24$ V			100			100	μA
Strobe Current	$V_{strobe} = 0.4$ V		1.7	3.3		1.7	3.3	mA
Strobe ON Voltage		0.9	1.4		0.9	1.4		V
Strobe OFF Voltage	$I_{sink} \leq 16$ mA		1.4	2.5		1.4	2.5	V
Positive Supply Current	$V_{IN} = -5$ mV		5.5	10		5.5	10	mA
Negative Supply Current			1.5	3.6		1.5	3.6	mA

Note 1: Derate metal can package at 6.8 mW/°C for operation at ambient temperatures above 60°C; derate flat package at 5.4 mW/°C for operation at ambient temperatures above 40°C.

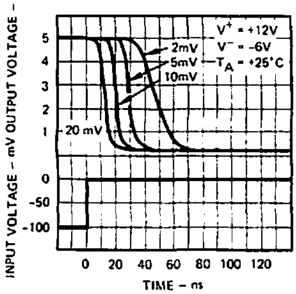
Note 2: These specifications apply for $-3\text{ V} \geq V^- \geq -12$ V, $V^+ = 12$ V and $T_A = 25°C$ unless otherwise specified.

Note 3: The offset voltages, offset currents, and bias currents given are the maximum values required to drive the output from the minimum output level up to the maximum output level. Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

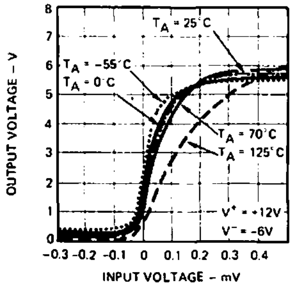
Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

PERFORMANCE CURVES

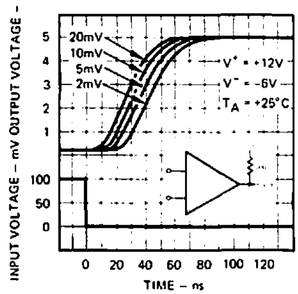
Response Time For Various Input Overdrives



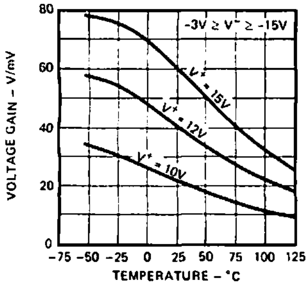
Transfer Function



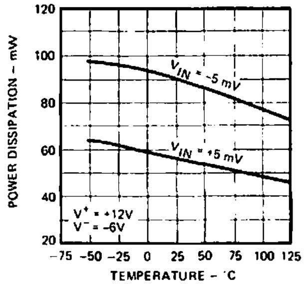
Response Time For Various Input Overdrives



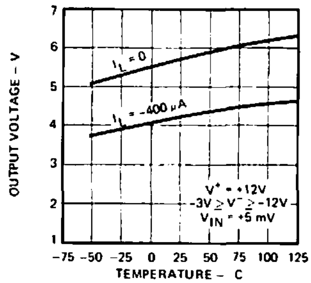
Voltage Gain



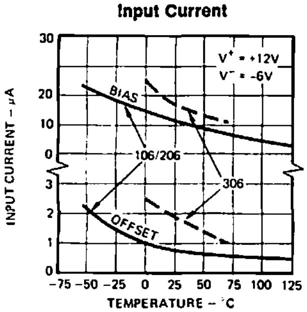
Power Consumption



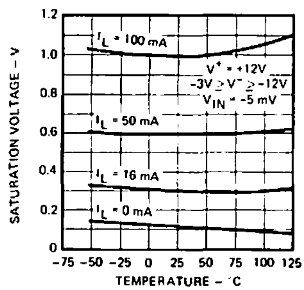
Positive Output Level



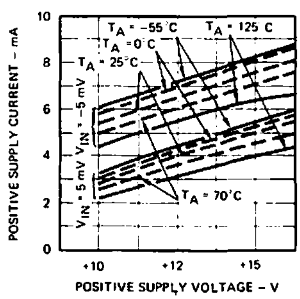
Input Current



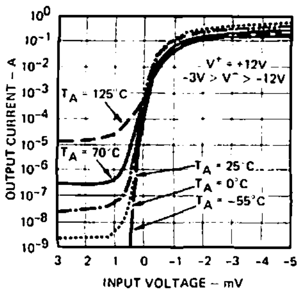
Saturation Voltage



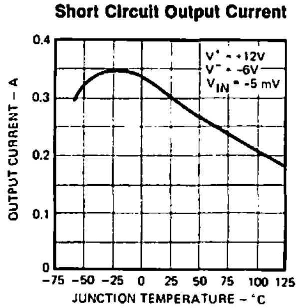
Positive Supply Current



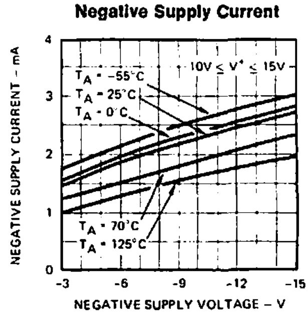
Transconductance



Short Circuit Output Current



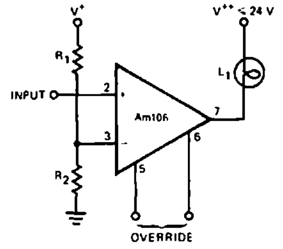
Negative Supply Current



LIC-076

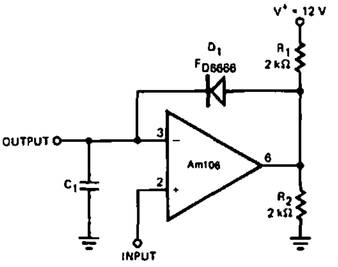
ADDITIONAL APPLICATIONS

Level Detector and Lamp Driver



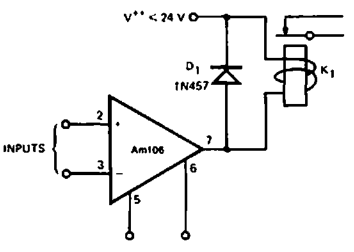
LIC-077

Fast Response Peak Detector



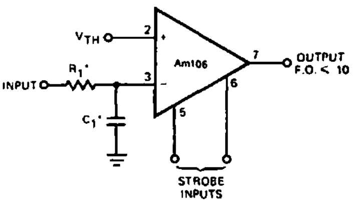
LIC-078

Relay Driver



LIC-079

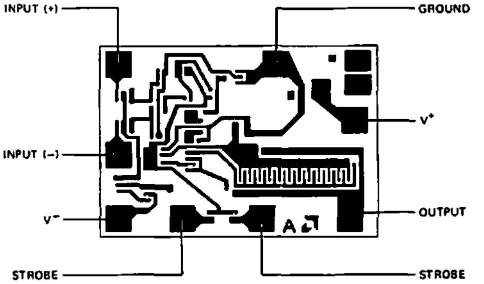
Adjustable Threshold Line Receiver



LIC-080

*Optional for response time control

Metallization and Pad Layout



33 x 46 Mils

Am111/211/311

Precision Voltage Comparator

Distinctive Characteristics

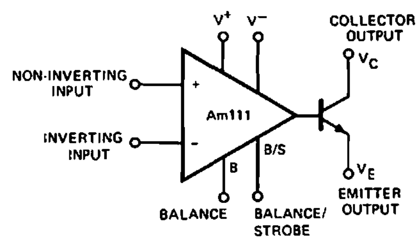
- The Am111/211/311 are functionally, electrically, and pin-for-pin equivalent to the National LM 111/211/311
- Output Drive – 50V and 50mA
- Input Bias Current – 150nA max.
- Input Offset Voltage – 4mV max.
- Differential Input Voltage Range – ±30V
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected die for assemblers of hybrid products
- Mixing privileges for obtaining price discounts. Refer to price list.
- Available in Metal Can, Hermetic Dual-In-Line or hermetic Flat Packages

2

FUNCTIONAL DESCRIPTION

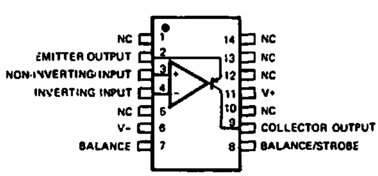
The Am111/211/311 are voltage comparators featuring low input currents, high differential and common mode voltage ranges, wide supply voltage range, and outputs compatible with all bipolar and MOS circuitry. The inputs and outputs can be isolated from system ground, and the output can drive loads refered to ground or either supply. Strobing and offset balancing are available and the outputs can be wire ORed.

FUNCTIONAL DIAGRAM



LIC-081

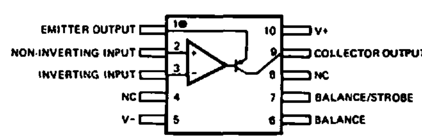
CONNECTION DIAGRAM
Top View
Dual-In-Line
Am111/211/311



Pin 6 is connected to bottom of package.

LIC-082

CONNECTION DIAGRAM
Top View
Flat Package
Am111/211/311



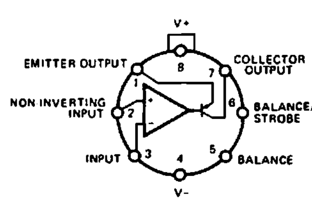
Pin 5 is connected to bottom of package.

LIC-083

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am311	TO-99	0°C to +70°C	LM311H
	Hermetic DIP	0°C to +70°C	LM311D
	Mini-DIP	0°C to +70°C	LM311N
	Dice	0°C to +70°C	LD311
Am211	TO-99	–25°C to +85°C	LM211H
	Hermetic DIP	–25°C to +85°C	LM211D
Am111	TO-99	–55°C to +125°C	LM111H
	Hermetic DIP	–55°C to +125°C	LM111D
	Flat Pak	–55°C to +125°C	LM111F
	Dice	–55°C to +125°C	LD111

CONNECTION DIAGRAM
Top View
Metal Can
Am111/211/311



Pin 4 is connected to case.

LIC-084

MAXIMUM RATINGS

Voltage from V^+ to V^-	36V
Voltage from Collector Output to V^-	
Am111/211	50V
Am311	40V
Voltage from Emitter Output to V^-	30V
Voltage between Inputs	±30V
Voltage from Inputs to V^-	+30V, –0V
Voltage from Inputs to V^+	–30V
Power Dissipation (Note 1)	500mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	
Am111	–55°C to +125°C
Am211	–25°C to +85°C
Am311	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 2)

Parameters (see definitions)	Test Conditions	Am311 Min.	Am311 Typ.	Am311 Max.	Am111 Am211 Min.	Am111 Am211 Typ.	Am111 Am211 Max.	Units
Input Offset Voltage (Note 3)			2.0	7.5		0.7	3.0	mV
Input Offset Current (Note 3)			6.0	50.0		4.0	10.0	nA
Input Bias Current (Note 3)			100	250		60	100	nA
Response Time (Note 4)	R_L = 500 Ω to +5 V, V_E = 0		200			200		ns
Supply Current Positive (Note 5)			3.9	7.5		3.9	6.0	mA
Negative (Note 5)			2.6	5.0		2.6	4.5	mA
Voltage Gain			200			200		V/mV
Saturation Voltage	$V_{IN} \leq -5$ mV, I_C = 50 mA					0.75	1.5	Volts
	$V_{IN} \leq -10$ mV, I_C = 50 mA		0.75	1.5				Volts
Output Leakage Current	$V_{IN} \geq +5$ mV, V_C to V_E = 50 V					0.2	10.0	nA
	$V_{IN} \geq +10$ mV, V_C to V_E = 40 V		0.2	50.0				nA
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage (Note 3)				10.0			4.0	mV
Input Offset Current (Note 3)				70.0			20.0	nA
Input Bias Current (Note 3)				300			150	nA
Saturation Voltage	$V_{IN} \leq -6$ mV, I_C = 8 mA					0.23	0.40	Volts
	$V_{IN} \leq -10$ mV, I_C = 8 mA		0.23	0.40				Volts
Output Leakage Current	$V_{IN} \geq +6$ mV, V_C to V_E = 50 V					0.1	0.5	μA
Input Voltage Range		±13	±14		±13	±14		Volts
Supply Current Positive (Note 5)	T_A = 125°C					2.7	4.5	mA
Negative (Note 5)	T_A = 125°C					1.8	3.5	mA

Notes: 1. For the Am111/211/311, derate Metal Can package at 6.8mW/°C for operation at ambient temperatures above 75°C, the Dual In-Line at 9mW/°C for operation at ambient temperatures above 95°C, and the Flat Packages at 5.4mW/°C for operation at ambient temperatures above 57°C.

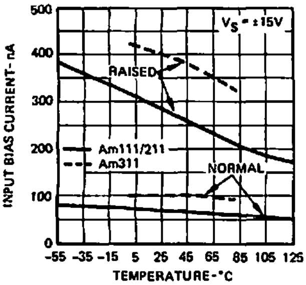
2. Unless otherwise specified, these specifications apply for V^+ = +15V, $V-$ = –15V, V_E = –15V, and R_L at collector output = 7.5kΩ to +15V.

3. The offset voltage, offset current and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a 7.5kΩ load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

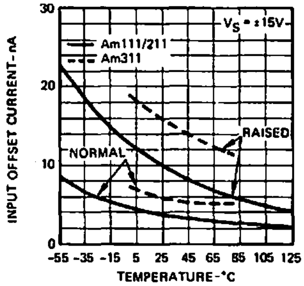
4. The response time specified (see definitions) is for a 100mV input step with 5mV overdrive.

PERFORMANCE CURVES

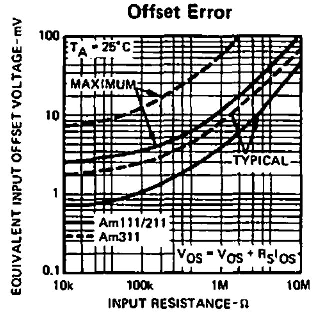
Input Bias Current



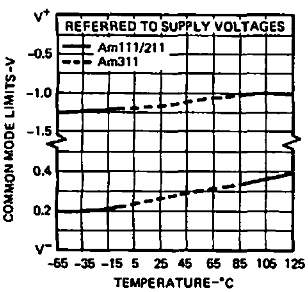
Input Offset Current



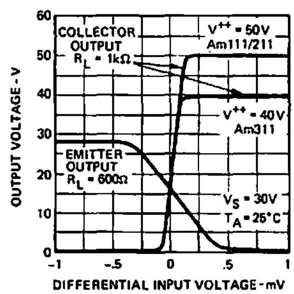
Offset Error



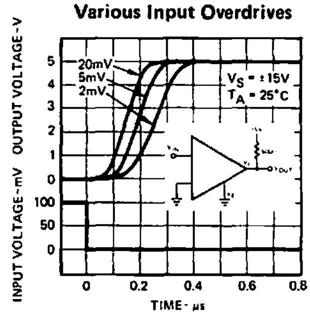
Common-Mode Limits



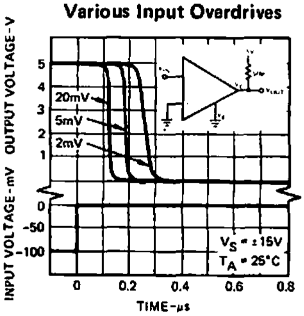
Transfer Function



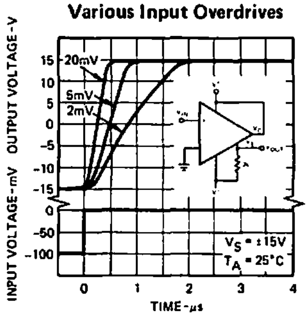
Response Time For Various Input Overdrives



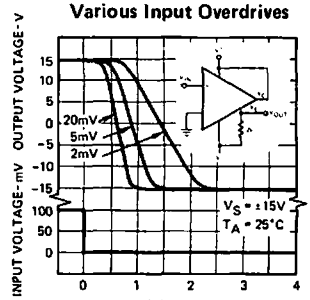
Response Time For Various Input Overdrives



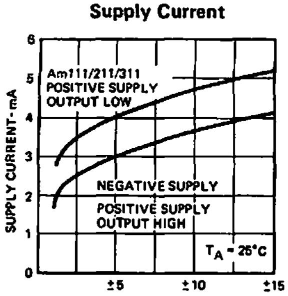
Response Time For Various Input Overdrives



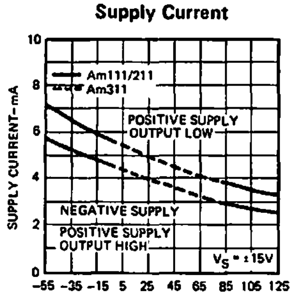
Response Time For Various Input Overdrives



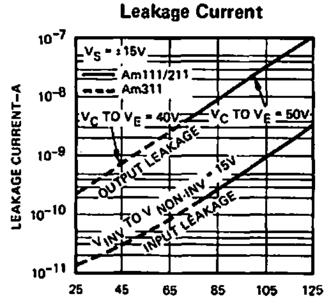
Supply Current



Supply Current



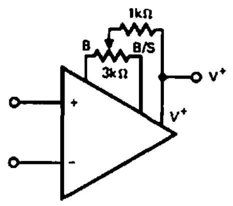
Leakage Current



LIC-085

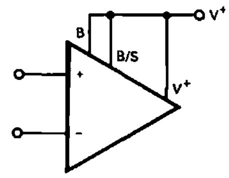
APPLICATIONS

Offset Balancing



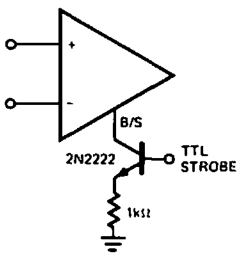
LIC-086

Increasing Input Stage Current*



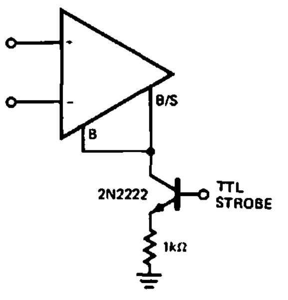
LIC-087

Strobing



LIC-088

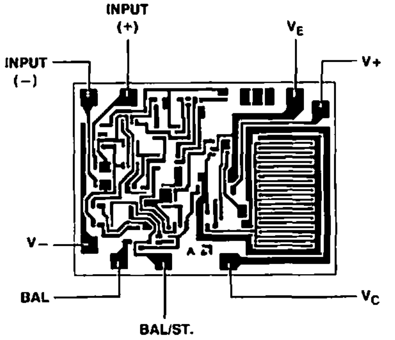
Strobing OFF both Input and Output Stages**



LIC-089

*Increases input bias current and common mode slew rate by a factor of 3.
**Typical input current = 50pA with inputs strobed OFF.

Metallization and Pad Layout



48 x 65 Mils

Am119/219/319

Dual Comparator

Distinctive Characteristics

- The Am119/219/319 are functionally, electrically, and pin-for-pin equivalent to the National LM119/219/319.
- Two independent comparators.
- Operates from single 5V supply.
- Output drive – 35V and 25mA.
- Input bias current – 1μA max. (1.2μA for Am319)
- Response time 80ns typical at ±15V.
- Minimum fan out of 2 each side.
- Inputs and outputs isolated from system ground.
- High common mode slew rate.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected die for assemblers of hybrid products.
- Available in Metal Can, Hermetic Dual-In-Line, Hermetic Flatpack or Molded DIP packages.

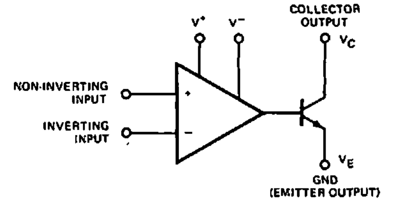
2

FUNCTIONAL DESCRIPTION

The Am119/219/319 are dual high-speed voltage comparators designed to operate over a wide range of voltage supplies down to a single 5V supply and ground. They have higher gain and lower input bias currents than devices such as the μA710. The uncommitted collector of the output stage facilitates RTL, DTL and TTL interfacing, and driving lamps and relays at currents up to 25mA. The device is specified for operation from power supplies up to ±15V and features faster response than the Am111 at the expense of higher power dissipation.

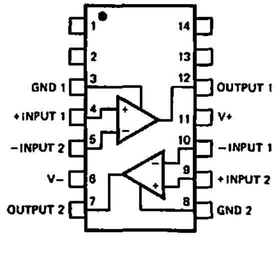
The Am119 performance is specified over the temperature range –55°C to 125°C, the Am219 performance is specified over the temperature range –25°C to 85°C and the Am319 performance is specified over the temperature range 0°C to 70°C.

FUNCTIONAL DIAGRAM
(One Comparator)



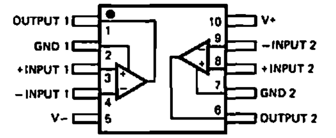
LIC-091

CONNECTION DIAGRAM
Top View
Dual In-Line



Pin 6 connected to bottom of package. LIC-090

CONNECTION DIAGRAM
Top View
Flat Package

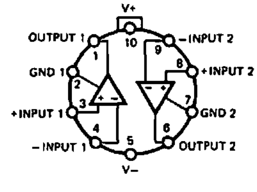


Pin 5 connected to bottom of package. LIC-092

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am319	TO-99	0°C to +70°C	LM319H
	DIP	0°C to +70°C	LM319D
	Molded DIP	0°C to +70°C	LM319N
	Dice	0°C to +70°C	LD319
Am219	TO-99	–25°C to +85°C	LM219H
	DIP	–25°C to +85°C	LM219D
	Flat Pak	–25°C to +85°C	LM219F
Am119	TO-99	–55°C to +125°C	LM119H
	DIP	–55°C to +125°C	LM119D
	Flat Pak	–55°C to +125°C	LM119F
	Dice	–55°C to +125°C	LD119

CONNECTION DIAGRAM
Top View
Metal Can



Pin 5 connected to case. LIC-093

MAXIMUM RATINGS (Above which the useful life may be impaired)

Voltage from V^+ to V^-	36V
Voltage from Collector Output to V^-	36V
Voltage from Ground to V^+	18V
Voltage from Ground to V^-	25V
Differential Input Voltage	±5.0V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500mW
Output Short Circuit Duration	10s
Operating Temperature Range	
Am119	−55°C to +125°C
Am219	−25°C to +85°C
Am319	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

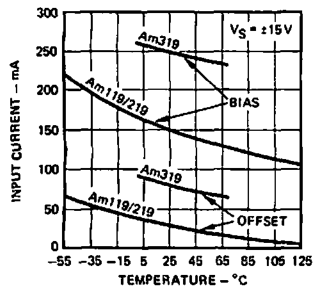
ELECTRICAL CHARACTERISTICS (T_A = 25°C, Unless Otherwise Noted) (Note 3)

Parameters (See definitions)		Conditions		Am319 Min.	Am319 Typ.	Am319 Max.	Am119/219 Min.	Am119/219 Typ.	Am119/219 Max.	Units
Input Offset Voltage (Note 4)		$R_S \leq 5k$			2.0	8.0		0.7	4.0	mV
Input Offset Current (Note 4)					80	200		30	75	nA
Input Bias Current					250	1000		150	500	nA
Response Time (Note 5)					80			80		ns
Supply Current	Positive	$V^+ = 5.0V, V^- = 0$			4.3			4.3		mA
		$V_S = \pm15V$			8.0	12.5		8.0	11.5	
	Negative	$V_S = \pm15V$			3.0	5.0		3.0	4.5	
Voltage Gain				8.0	40		10	40		
Saturation Voltage		$V_{in} \leq -5.0mV, I_C = 25mA$						0.75	1.5	Volts
		$V_{in} \leq -10mV, I_C = 25mA$			0.75	1.5				
Output Leakage Current		$V_{in} \geq +5.0mV, V_C$ to $V_E = 35V$						0.2	2.0	µA
		$V_{in} \geq +10mV, V_C$ to $V_E = 35V$			0.2	10				
The Following Specifications Apply Over The Operating Temperature Ranges										
Input Offset Voltage (Note 4)		$R_S \leq 5k$				10			7.0	mV
Input Offset Current (Note 4)						300			100	nA
Input Bias Current						1200			1000	nA
Saturation Voltage		$V_{in} \leq -8.0mV, I_C = 3.2mA$	$T_A \geq 0°C$					0.23	0.4	Volts
			$T_A \leq 0°C$						0.6	
		$V_{in} \leq -12mV, I_C = 3.2mA$			0.3	0.4				
Output Leakage Current		$V_{in} \geq +8.0mV, V_C$ to $V_E = 35V$						1.0	10	µA
Input Voltage Range		$V_S = \pm15V$			±13			±13		Volts
		$V^+ = 5.0V, V^- = 0$		1.0		3.0	1.0		3.0	

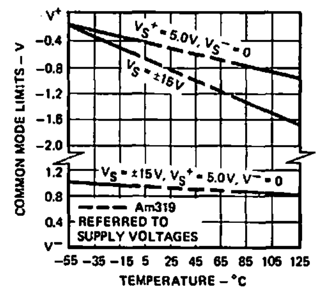
Notes:
1. For supply voltages less than ± 15V the absolute maximum rating is equal to the supply voltage.
2. Derate Metal Can package at 6.8mW/°C for operation at ambient temperatures above 75°C, the Dual-In-Line at 9mW/°C for operation at temperatures above 55°C, and the Flat Package at 5.4mW/°C for operation at temperatures above 57°C.
3. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ± 15V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within 1 volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified is for a 100mV input step with 5mV overdrive.

TYPICAL PERFORMANCE CURVES

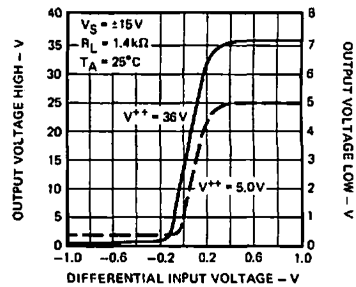
Input Currents



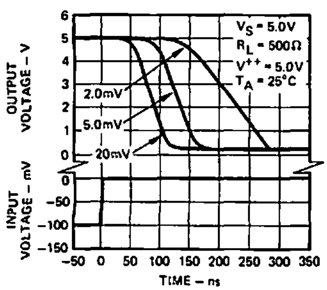
Common Mode Limits



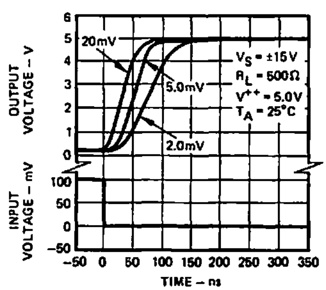
Transfer Function



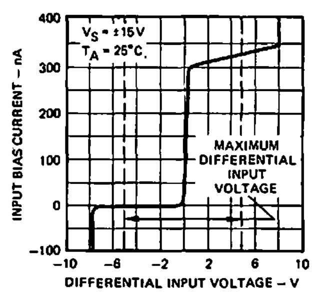
Response Time for Various Input Overdrives



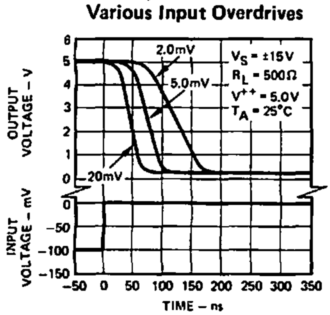
Response Time for Various Input Overdrives



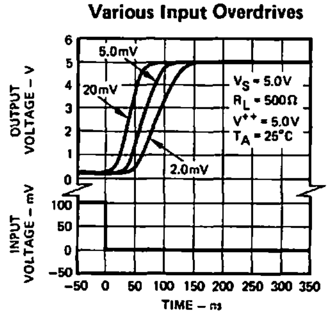
Input Characteristics



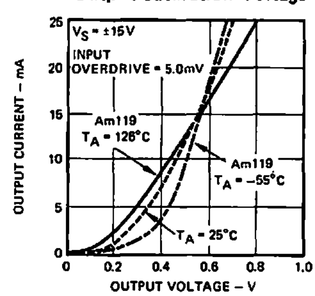
Response Time for Various Input Overdrives



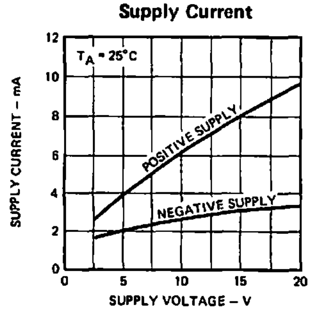
Response Time for Various Input Overdrives



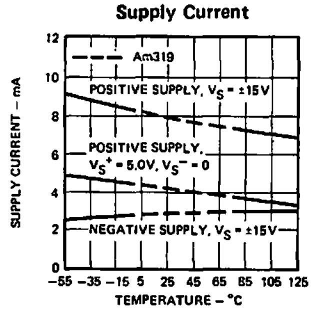
Output Saturation Voltage



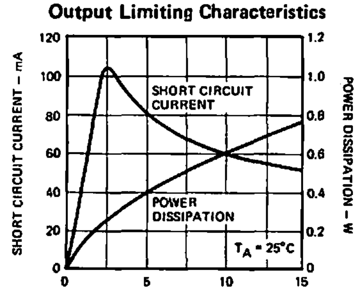
Supply Current



Supply Current



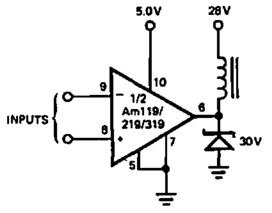
Output Limiting Characteristics



LIC-094

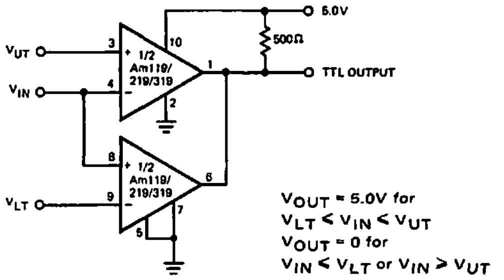
APPLICATIONS

Relay Driver



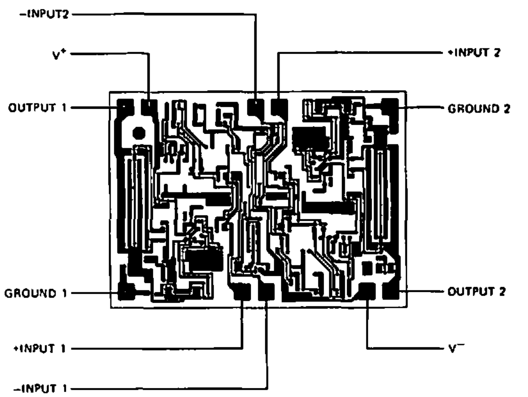
LIC-095

Window Detector



LIC-096

Metallization and Pad Layout



57 x 78 Mils

Am139/239/339 • Am139A/239A/339A

Low Offset Voltage Quad Comparators

Distinctive Characteristics

- Four high precision comparators
- Reduced VOS drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Wide single supply voltage range or dual supplies
  $2.0 V_{DC}$ to $36 V_{DC}$
  $\pm 1.0 V_{DC}$ to $\pm 18 V_{DC}$
- Very low supply current drain (0.8mA)—independent of supply voltage (1.0mW/comparator) makes these comparators suitable for battery operation.
- Low input bias current – 35nA
- Low input offset current – 3.0nA and offset voltage – 2.0mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage
  1.0mV at 5.0μA
  60mV at 1.0mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

2

FUNCTIONAL DESCRIPTION

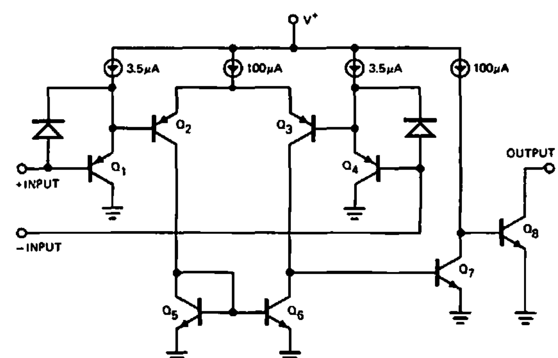
The Am139, Am239, Am339, Am339A, Am239A and Am339A quad comparators are functionally, electrically and pin-for-pin equivalent to the National LM139, LM239, LM339, LM339A, LM239A and LM339A. This series of precision comparators consists of four independent voltage comparators which were specifically designed to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators have a unique characteristic in that the input common-mode voltage range includes ground even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The Am139/A series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the Am139/A will directly interface with MOS logic – where the lower power drain of the Am139/A is a distinct advantage over standard comparators.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am339	DIP	0°C to 70°C	LM339D
	Molded DIP	0°C to 70°C	LM339N
	Dice	0°C to 70°C	LD339
Am239	DIP	–25°C to +85°C	LM239D
Am139	DIP	–55°C to +125°C	LM139D
	Flat Pack	–55°C to +125°C	LM139F
	Dice	–55°C to +125°C	LD139
Am339A	DIP	0°C to 70°C	LM339AD
	Molded DIP	0°C to 70°C	LM339AN
	Dice	0°C to 70°C	LD339A
Am239A	DIP	–25°C to +85°C	LM239AD
Am139A	DIP	–55°C to +125°C	LM139AD
	Flat Pack	–55°C to +125°C	LM139AF
	Dice	–55°C to +125°C	LD139A

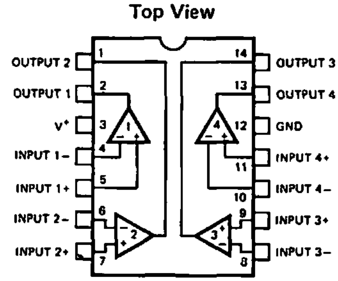
SCHEMATIC DIAGRAM



LIC-097

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

LIC-098

MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage, V+	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Power Dissipation (Note 1)	
Ceramic Dip	900 mW
Plastic Dip	570 mW
Flat Pack	800 mW

Output Short Circuit to GND (Note 2)	Continuous
Input Current (V_{in} −0.3 V_{DC}) (Note 3)	50 mA
Operating Temperature Range	
Am339/A	0°C to +70°C
Am239/A	−25°C to +85°C
Am139/A	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS
(V^+ = +5.0V_{DC}) (Note 4)

Parameters	Test Conditions	Am239 Am339 Min.	Typ.	Max.	Am139 Min.	Typ.	Max.	Am239A Am339A Min.	Typ.	Max.	Am139A Min.	Typ.	Max.	Units
Input Offset Voltage	T_A = +25°C (Note 9)		±2.0	±5.0		±2.0	±5.0		±1.0	±2.0		±1.0	±2.0	mV_{DC}
Input Bias Current (Note 5)	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, T_A = +25°C		25	250		25	100		25	250		25	100	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, T_A = +25°C		±5.0	±50		±3.0	±25		±5.0	±50		±3.0	±25	nA_{DC}
Input Common-Mode Voltage Range (Note 6)	T_A = +25°C	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V_{DC}
Supply Current	R_L = ∞ on all Comparators T_A = +25°C		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0	mA_{DC}
Voltage Gain	R_L > 15kΩ, T_A = +25°C, V^+ = 15 V_{DC} (To Support Large V_o Swing)		200			200		50	200		50	200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = +1.4V_{DC}, V_{R_L} = 5.0V_{DC}, R_L = 5.1kΩ and T_A = +25°C		300			300			300			300		ns
Response Time (Note 7)	V_{R_L} = 5.0 V_{DC} and R_L = 5.1 kΩ T_A = +25°C		1.3			1.3			1.3			1.3		μs
Output Sink Current	$V_{IN(-)}$ > +1.0 V_{DC}, $V_{IN(+)}$ = 0, and V_o < +1.5 V_{DC}, T_A = +25°C	6.0	16		6.0	16		6.0	16		6.0	16		mA_{DC}
Saturation Voltage	$V_{IN(-)}$ > +1.0 V_{DC}, $V_{IN(+)}$ = 0, and I_{sink} < 4.0 mA, T_A = +25°C		250	400		250	400		250	400		250	400	mV_{DC}
Output Leakage Current	$V_{IN(+)}$ > +1.0 V_{DC}, $V_{IN(-)}$ = 0 and V_o = 5.0 V_{DC}, T_A = +25°C		0.1			0.1			0.1			0.1		nA_{DC}
Input Offset Voltage	(Note 9)			9.0			9.0			4.0			4.0	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±150			±100			±150			±100	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			400			300			400			300	nA_{DC}
Input Common-Mode Voltage Range		0		V^+−2.0	0		V^+−2.0	0		V^+−2.0	0		V^+−2.0	V_{DC}
Saturation Voltage	$V_{IN(-)}$ > +1.0 V_{DC}, $V_{IN(+)}$ = 0 and I_{sink} < 4.0 mA			700			700			700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)}$ > +1.0 V_{DC}, $V_{IN(-)}$ = 0 and V_o = 30 V_{DC}			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage (Note 8)	Keep all V_{IN}'s > 0 V_{DC} (or V− if used)			36			36			V^+			V^+	V_{DC}

Note 1: For high temperature operation, the Am339/A must be derated based on a +125°C maximum junction temperature and a thermal resistance of +175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The Am239/A and Am139/A must be derated based on a +150°C maximum junction temperature. The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small (Pd ≤ 100 mW), provided the output transistors are allowed to saturate.

2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.

3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal outputs states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC}.

4: These specifications apply for V^+ = +5.0 V_{DC} and −55°C ≤ T_A ≤ +125°C, unless otherwise stated. With the Am239/A all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C and the Am339/A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C.

5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+−1.5 V, but either or both inputs can go to +30 V_{DC} without damage.

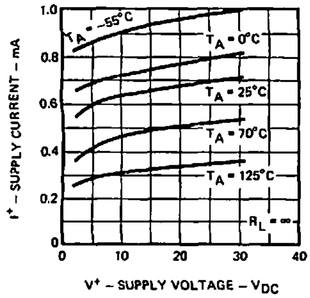
7: The response time specified is for a 100mV input step with 5.0mV overdrive. 300ns can be achieved with larger overdrive signals, see typical performance characteristics section.

8: If the voltage applied to any input exceeds V^+, all four comparator outputs will go to the high voltage level. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply, if used).

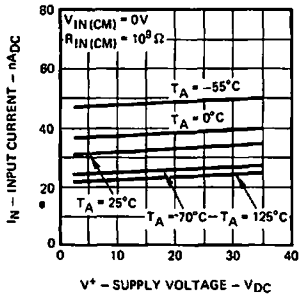
9: At output switch point, $V_O \cong 1.4V_{DC}$, R_S = 0Ω with V^+ from 5.0 V_{DC}; and over the full input common mode range (0 V_{DC} to V^+ -1.5V_{DC}).

TYPICAL PERFORMANCE CHARACTERISTICS

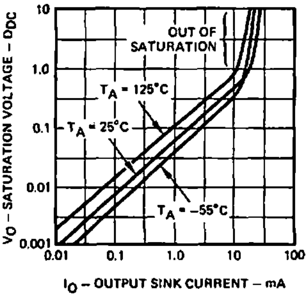
Supply Current



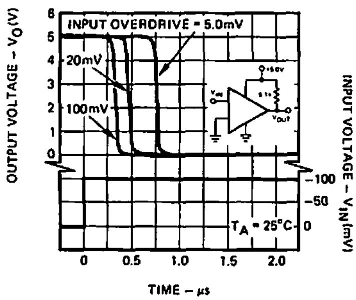
Input Current



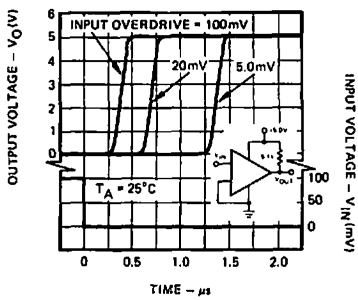
Output Saturation Voltage



Response Time for Various Input Overdrives Negative Transition



Response Time for Various Input Overdrives Positive Transition



LIC-099

APPLICATION HINTS

The Am139/A is a high gain, wide bandwidth device; which like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. The oscillation shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board-layout is helpful as it reduces stray input-output coupling. Lowering the input resistors to <10kΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the I/C card attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

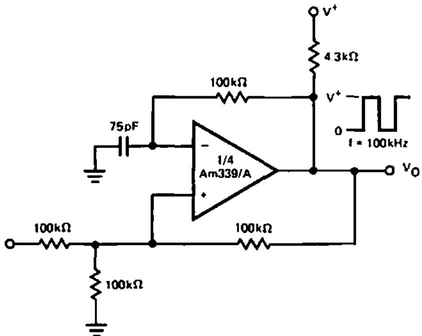
The bias network of the Am139/A establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from $2V_{DC}$ to $30\ V_{DC}$.

It is not normally necessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3V_{DC}$ (at 25°C). An input clamp diode and input resistor can be used as shown in the applications section.

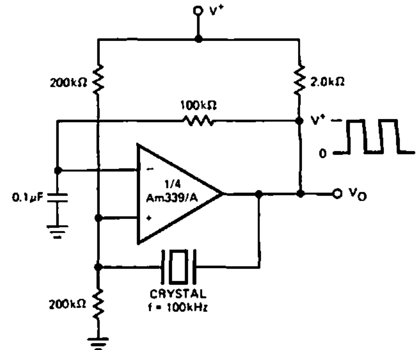
The output of the Am139/A is the uncommitted collector of a grounded-emitter NPN output transistor. Several collectors can be tied together to provide an output OR'ing function. An output "pull-up" resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the Am139/A package. The output can also be used as a simple SPST switch to ground (when a "pull-up" resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{sat} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp very nearly to ground level for small load currents.

TYPICAL APPLICATIONS
($V^+ = 5.0V_{DC}$)



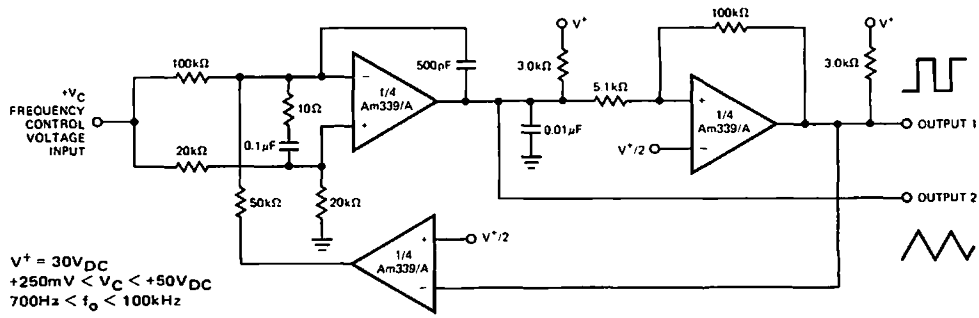
LIC-100

Squarewave Oscillator



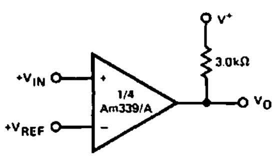
Crystal Controlled Oscillator

LIC-101



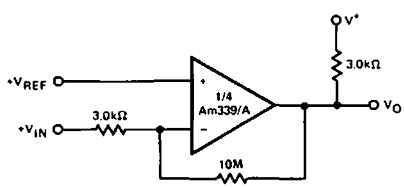
Two-Decade High-Frequency VCO

LIC-102



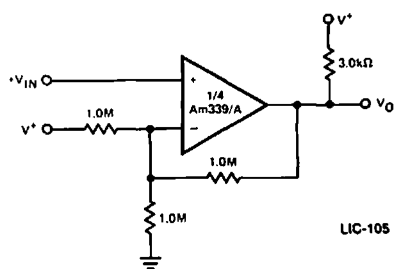
LIC-103

Basic Comparator



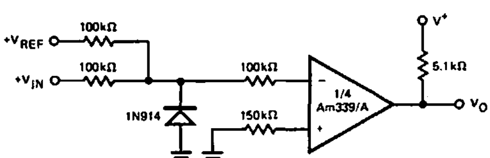
LIC-104

Non-Inverting Comparator with Hysteresis



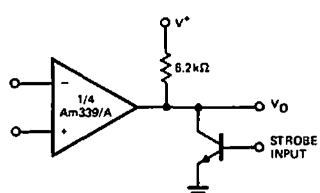
LIC-105

Inverting Comparator with Hysteresis



LIC-106

Comparing Input Voltages of Opposite Polarity



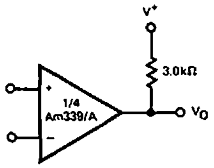
LIC-107

*Or logic gate without pull-up resistor.

Output Strobing

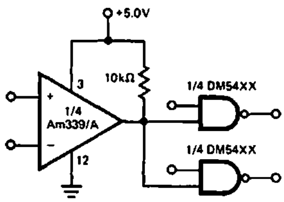
TYPICAL APPLICATIONS (Cont.)

($V^+ = 5.0V_{DC}$)



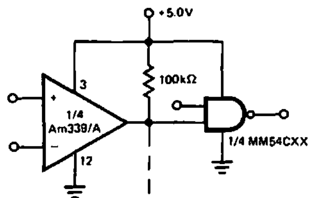
LIC-108

Basic Comparator



LIC-109

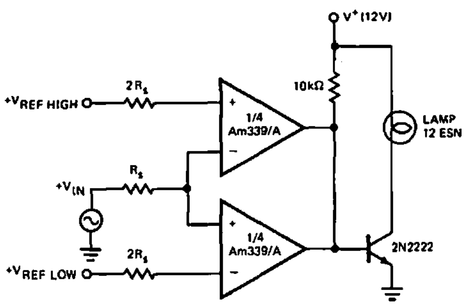
Driving TTL



LIC-110

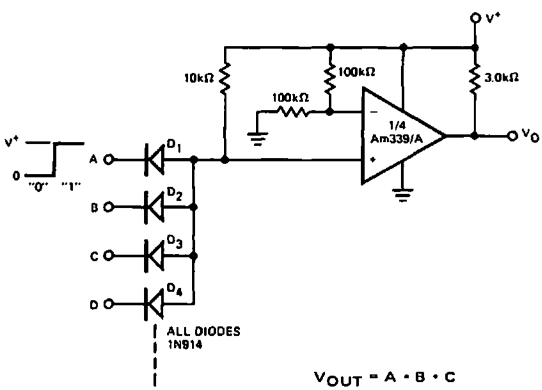
Driving CMOS

($V^+ = 15V_{DC}$)



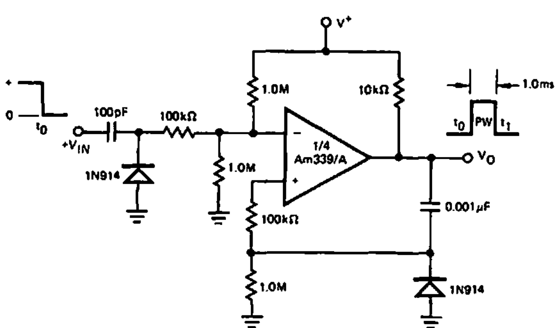
LIC-111

Limit Comparator



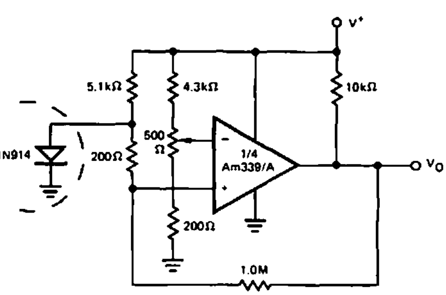
LIC-112

Large Fan-In AND Gate



LIC-113

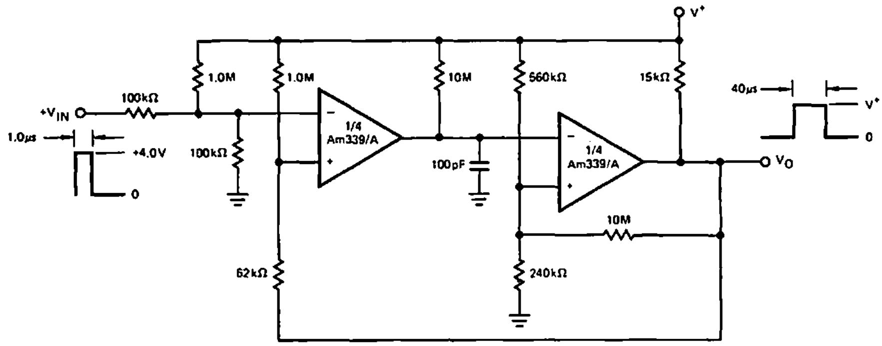
One-Shot Multivibrator



LIC-114

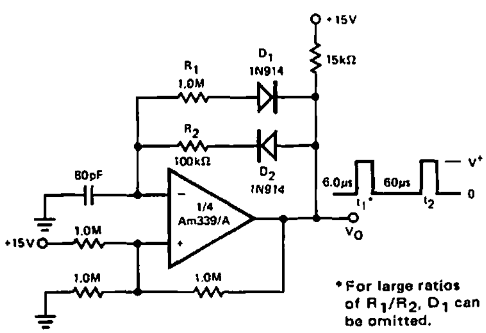
Remote Temperature Sensing

TYPICAL APPLICATIONS (Cont.)
($V^+ = 15V_{DC}$)



LIC-115

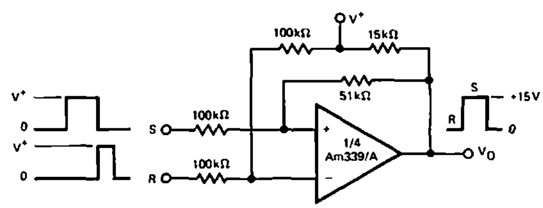
One-Shot Multivibrator with Input Lock Out



*For large ratios of R_1/R_2, D_1 can be omitted.

LIC-116

Pulse Generator



LIC-117

Bi-Stable Multivibrator

Am685

Voltage Comparator

Distinctive Characteristics:

- 6.5ns MAXIMUM PROPAGATION DELAY AT 5mV OVERDRIVE
- 3.0ns Latch setup time
- Complementary ECL outputs
- 50Ω line driving capability
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically and optically inspected dice for assemblers of hybrid products
- Available in metal can and hermetic dual-in-line packages

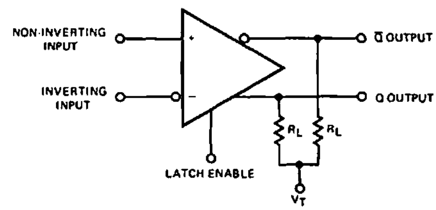
2

FUNCTIONAL DESCRIPTION

The Am685 is a fast voltage comparator manufactured with an advanced bipolar NPN, Schottky diode high-frequency process that makes possible very short propagation delays (6.5 ns) without sacrificing the excellent matching characteristics hitherto associated only with slow, high-performance linear IC's. The circuit has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50Ω transmission lines. The low input offset and high resolution make this comparator especially suitable for high-speed precision analog-to-digital processing.

A latch function is provided to allow the comparator to be used in a sample-hold mode. If the Latch Enable input is HIGH, the comparator functions normally. When the Latch Enable is driven LOW, the comparator outputs are locked in their existing logical states. If the latch function is not used, the Latch Enable must be connected to ground.

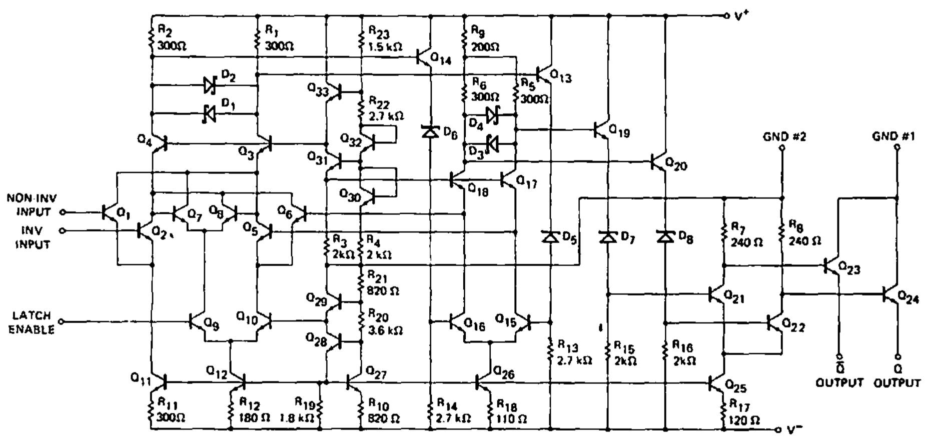
FUNCTIONAL DIAGRAM



LIC-118

The outputs are open emitters, therefore external pull-down resistors are required. These resistors may be in the range of 50–200Ω connected to −2.0 V, or 200–2000Ω connected to −5.2 V.

CIRCUIT DIAGRAM



LIC-119

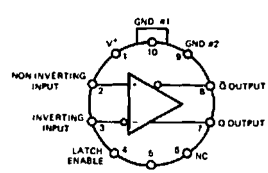
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am685	Metal Can	−30°C to +85°C	Am685HL
	DIP	−30°C to +85°C	Am685DL
Am685	Metal Can	−55°C to +125°C	Am685HM
	DIP	−55°C to +125°C	Am685DM
Am685	Dice	−30°C to +85°C	Am685XL
	Dice	−55°C to +125°C	Am685XM

CONNECTION DIAGRAMS

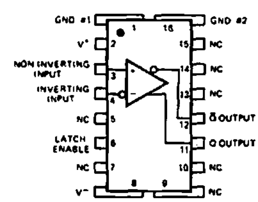
Top Views

Metal Can



LIC-120

Dual-In-Line



Note 1: On metal package, pin 5 is connected to case. On DIP, pin 8 is connected to case.

LIC-121

MAXIMUM RATINGS (Above which the useful life may be impaired)

Positive Supply Voltage	+7 V
Negative Supply Voltage	−7 V
Input Voltage	±4 V
Differential Input Voltage	±6 V
Output Current	30 mA
Power Dissipation (Note 2)	500 mW

Operating Temperature Range	
Am685-L	−30°C to +85°C
Am685-M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 Sec.)	300°C
Minimum Operating Voltage (V^+ to V^-)	9.7V

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

DC Characteristics

Symbol	Parameter (see definitions)	Conditions (Note 3)	Am685-L Min.	Am685-L Max.	Am685-M Min.	Am685-M Max.	Units
V_{OS}	Input Offset Voltage	$R_S < 100\,\Omega$, $T_A = 25°C$	−2.0	+2.0	−2.0	+2.0	mV
		$R_S < 100\,\Omega$	−2.5	+2.5	−3.0	+3.0	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S < 100\,\Omega$	−10	+10	−10	+10	μV/°C
I_{OS}	Input Offset Current	$T_A = 25°C$	−1.0	+1.0	−1.0	+1.0	μA
			−1.3	+1.3	−1.6	+1.6	μA
I_B	Input Bias Current	$T_A = 25°C$		10		10	μA
				13		16	μA
R_{IN}	Input Resistance	$T_A = 25°C$	6.0		6.0		kΩ
C_{IN}	Input Capacitance	$T_A = 25°C$		3.0		3.0	pF
V_{CM}	Input Voltage Range		−3.3	+3.3	−3.3	+3.3	V
CMRR	Common Mode Rejection Ratio	$R_S < 100\,\Omega$, $-3.3 < V_{CM} < +3.3\,V$	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S < 100\Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output HIGH Voltage	$T_A = 25°C$	−0.960	−0.810	−0.960	−0.810	V
		$T_A = T_{A(min.)}$	−1.060	−0.890	−1.100	−0.920	V
		$T_A = T_{A(max.)}$	−0.890	−0.700	−0.850	−0.620	V
V_{OL}	Output LOW Voltage	$T_A = 25°C$	−1.850	−1.650	−1.850	−1.650	V
		$T_A = T_{A(min.)}$	−1.890	−1.675	−1.910	−1.690	V
		$T_A = T_{A(max.)}$	−1.825	−1.625	−1.810	−1.575	V
I^+	Positive Supply Current			22		22	mA
I^-	Negative Supply Current			26		26	mA
P_{DISS}	Power Dissipation			300		300	mW

Switching Characteristics ($V_{in} = 100\,mV$, $V_{od} = 5\,mV$)

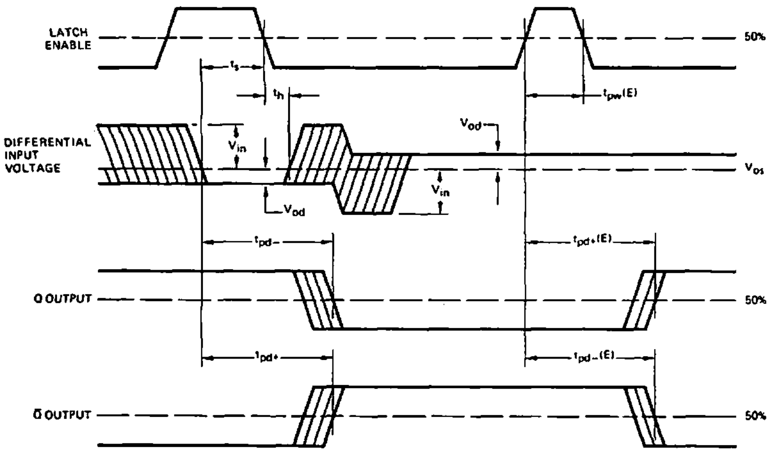
Symbol	Parameter	Conditions	Am685-L Min.	Am685-L Max.	Am685-M Min.	Am685-M Max.	Units
t_{pd+}	Input to Output HIGH	$T_{A(min.)} < T_A < 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
t_{pd-}	Input to Output LOW	$T_{A(min.)} < T_A < 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
$t_{pd+}(E)$	Latch Enable to Output HIGH (Note 4)	$T_{A(min.)} < T_A < 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
$t_{pd-}(E)$	Latch Enable to Output LOW (Note 4)	$T_{A(min.)} < T_A < 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
t_s	Minimum Set-up Time (Note 4)	$T_{A(min.)} < T_A < 25°C$		3.0		3.0	ns
		$T_A = T_{A(max.)}$		4.0		6.0	ns
t_h	Minimum Hold Time (Note 4)	$T_{A(min)} < T_A < T_{A(max.)}$		1.0		1.0	ns
$t_{pw}(E)$	Minimum Latch Enable Pulse Width (Note 4)	$T_{A(min.)} < T_A < 25°C$		3.0		3.0	ns
		$T_A = T_{A(max.)}$		4.0		5.0	ns

NOTES: 2: For the metal can package, derate at 6.8 mW/°C for operation at ambient temperatures above +100°C; for the dual-in-line package, derate at 9 mW/°C for operation at ambient temperatures above +105°C.

3: Unless otherwise specified $V^+ = 6.0V$, $V^- = -5.2V$, $V_T = -2.0V$, and $R_L = 50\Omega$; all switching characteristics are for a 100 mV input step with 5 mV overdrive. The specifications given for V_{os}, I_{os}, I_B, CMRR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltages. The Am685 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

4: Owing to the difficult and critical nature of switching measurements involving the latch, these parameters can not be tested in production. Engineering data indicates that at least 95% of the units will meet the specifications given.

TIMING DIAGRAM



LIC-122

KEY TO TIMING DIAGRAM

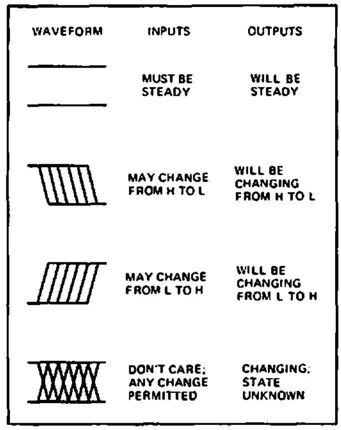


Figure 1

The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_s will be detected and held; those occurring after t_h will not be detected. Changes between t_s and t_h may or may not be detected.

DEFINITION OF TERMS

V_{OS} **INPUT OFFSET VOLTAGE** – That voltage which must be applied between the two input terminals through two equal resistances to obtain zero voltage between the two outputs.

$\Delta V_{OS}/\Delta T$ **AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE** – The ratio of the change in input offset voltage over the operating temperature range to the temperature range.

I_{OS} **INPUT OFFSET CURRENT** – The difference between the currents into the two input terminals when there is zero voltage between the two outputs.

I_B **INPUT BIAS CURRENT** – The average of the two input currents.

R_{IN} **INPUT RESISTANCE** – The resistance looking into either input terminal with the other grounded.

C_{IN} **INPUT CAPACITANCE** – The capacitance looking into either input terminal with the other grounded.

V_{CM} **INPUT VOLTAGE RANGE** – The range of voltages on the input terminals for which the offset and propagation delay specifications apply.

CMRR **COMMON MODE REJECTION RATIO** – The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

SVRR **SUPPLY VOLTAGE REJECTION RATIO** – The ratio of the change in input offset voltage to the change in power supply voltages producing it.

V_{OH} **OUTPUT HIGH VOLTAGE** – The logic HIGH output voltage with an external pull-down resistor returned to a negative supply.

V_{OL} **OUTPUT LOW VOLTAGE** – The logic LOW output voltage with an external pull-down resistor returned to a negative supply.

I^+ **POSITIVE SUPPLY CURRENT** – The current required from the positive supply to operate the comparator.

I^- **NEGATIVE SUPPLY CURRENT** – The current required from the negative supply to operate the comparator.

P_{DISS} **POWER DISSIPATION** – The power dissipated by the comparator with both outputs terminated in 50Ω to -2.0V.

SWITCHING TERMS (refer to Fig. 1)

t_{pd+} **INPUT TO OUTPUT HIGH DELAY** – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pd-} **INPUT TO OUTPUT LOW DELAY** – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{pd+(E)}$ **LATCH ENABLE TO OUTPUT HIGH DELAY** – The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{pd-(E)}$ **LATCH ENABLE TO OUTPUT LOW DELAY** – The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

t_s **MINIMUM SET-UP TIME** – The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h **MINIMUM HOLD TIME** – The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

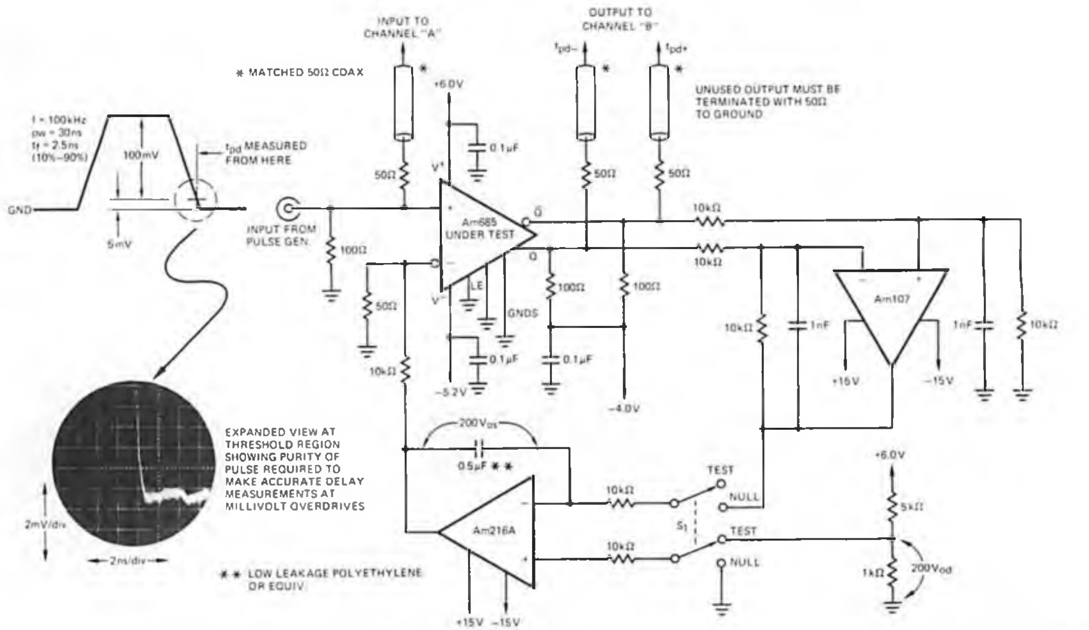
$t_{pw(E)}$ **MINIMUM LATCH ENABLE PULSE WIDTH** – The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an input signal change.

OTHER SYMBOLS

T_A Ambient temperature
R_S Input source resistance
V_S Supply voltages
V^+ Positive supply voltage
V^- Negative supply voltage
V_T Output load terminating voltage
R_L Output load resistance
V_{in} Input pulse amplitude
V_{od} Input overdrive
f Frequency

MEASUREMENT OF PROPAGATION DELAY

A voltage comparator must be able to respond to input signal levels ranging from a few millivolts to several volts, ideally with little variation in propagation delay. The most difficult condition is where the comparator has been driven hard into one state by a large signal, and the next input signal is just barely enough to make it switch to the other state. This forces the input stage of the circuit to swing from a full off (or on) state to a point somewhere near the center of its linear range, thus exercising both its large- and small-signal responses. If the comparator is fast for this condition, it should be as fast or faster for almost any other condition. The unofficial industry standard input signal is a 100mV step with an overdrive of 5mV (the overdrive is the voltage in excess of that needed to bring the output to the center of its dynamic range). The 100mV is more than enough to fully turn on the input stage, but not so large to make measurement a problem. Large pulses would require exceptionally good control on waveform purity, since only a few tenths of a percent of overshoot or ripple would be enough to affect the value of the overdrive and, for sensitive comparators, result in false switching. The propagation delay is measured from the time the input signal crosses the input threshold voltage (i.e., the offset voltage) to the 50% point of either output. This definition ensures that each unit is measured under equal conditions, and also makes the measurement relatively independent of the input rise and fall times.



LIC-123

Figure 2

The test circuit of Figure 2 provides a means of automatically nulling out the offset voltage and applying the overdrive. With S1 in the "NULL" position, the feedback loop around the Am685 via the two operational amplifiers corrects for the offset of the circuit including any dc shift in the ground level of the input signal. When switched to "TEST", the offset is held on the storage capacitor of the Am216A and the overdrive is added at the Am216A non-inverting input. The duty cycle of the signal is made low so that the presence of the input pulse during nulling will not disturb the offset. A solid ground plane is used for the test jig, and capacitors bypass the supply voltages. All power and signal leads are kept as short as possible. The Am685 input and output run directly into the 50Ω inputs of the sampling scope via equal lengths of 50Ω coaxial cable. For the conditions shown in the figure, t_{pd+} is measured at the $\bar{Q}$ output and t_{pd-} at the Q output. If it is desired to measure the opposite output polarities, the polarities of the input signal and overdrive must be reversed.

THERMAL CONSIDERATIONS

To achieve the high speed of the Am685, a certain amount of power must be dissipated as heat. This increases the temperature of the die relative to the ambient temperature. In order to be compatible with ECL III and ECL 10,000, which normally use air flow as a means of package cooling, the Am685 characteristics are specified when the device has an air flow across the package of 500 linear feet per minute or greater. Thus, even though different ECL circuits on a printed circuit board may have different power dissipations, all will have the same input and output levels, etc., provided each sees the same air flow and air temperature. This eases design, since the only change in characteristics between devices is due to the increase in ambient temperature of the air passing over the devices. If the Am685 is operated without air flow, the change in electrical characteristics due to the increased die temperature must be taken into account.

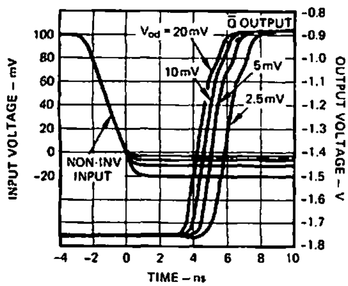
INTERCONNECTION TECHNIQUES

All high-speed ECL circuits require that special precautions be taken for optimum system performance. The Am685 is particularly critical because it features very high gain (60dB) at very high frequencies (100MHz). A ground plane must be provided for a good, low inductance, ground current return path. The impedance at the inputs should be as low as possible and lead lengths as short as practical. It is preferable to solder the device directly to the printed circuit board instead of using a socket. Open wiring on the outputs should be limited to less than one inch, since severe ringing occurs beyond this length. For longer lengths, the printed-circuit interconnections become microstrip transmission lines when backed up by a ground plane, with a characteristic impedance of 50 to 150Ω. Reflections will occur unless the line is terminated in its characteristic impedance. The termination resistors normally go to −2.0V, but a Thevenin equivalent to V⁻ can be used at some increase in power. Best results are usually obtained with the terminating resistor at the end of the driven line. The lower impedance lines are more suitable for driving capacitive loads. The supply voltages should be well decoupled with RF capacitors connected to the ground plane as close to the device supply pins as possible.

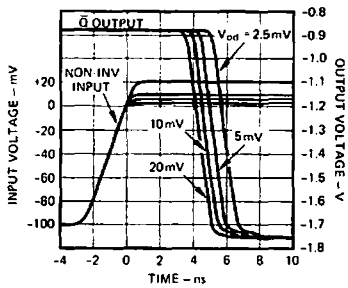
PERFORMANCE CURVES

(Unless otherwise specified, standard conditions for all curves are $T_A = 25°C$, $V^+ = 6.0V$, $V^- = -5.2V$, $V_T = -2.0V$, $R_L = 50\Omega$, and switching characteristics are for $V_{in} = 100mV$, $V_{od} = 5mV$.)

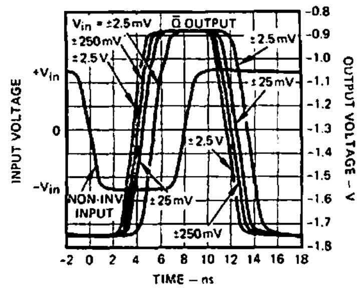
Response for Various Input Overdrives



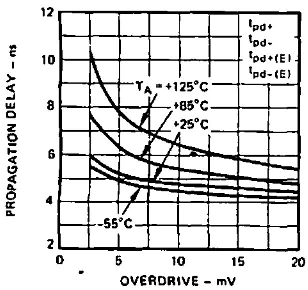
Response for Various Input Overdrives



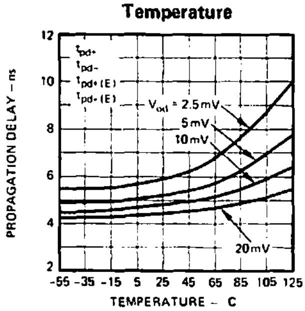
Response for Various Input Signal Levels



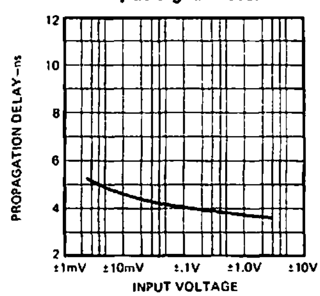
Propagation Delays as a Function of Input Overdrive



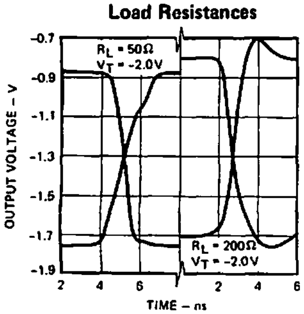
Propagation Delays as a Function of Temperature



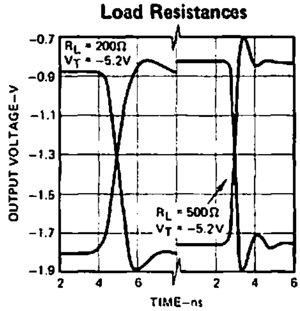
Propagation Delay as a Function of Input Signal Level



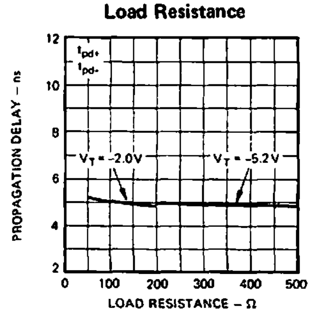
Response for Various Load Resistances



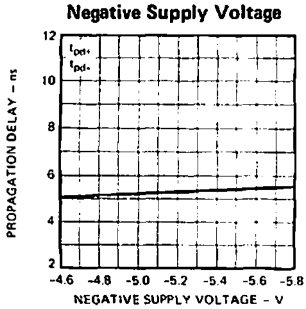
Response for Various Load Resistances



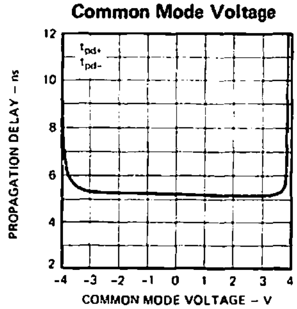
Propagation Delays as a Function of Load Resistance



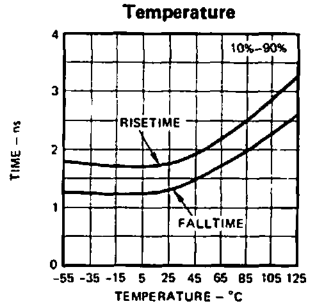
Propagation Delays as a Function of Negative Supply Voltage



Propagation Delays as a Function of Common Mode Voltage



Output Rise and Fall Times as a Function of Temperature

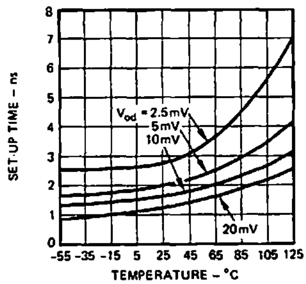


LIC-124

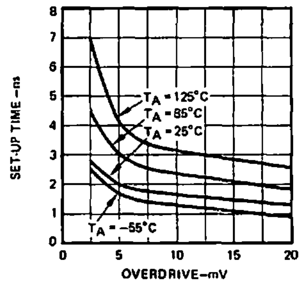
PERFORMANCE CURVES (Cont.)

(Unless otherwise specified, standard conditions for all curves are $T_A = 25°C$, $V^+ = 6.0V$, $V^- = -5.2V$, $V_T = -2.0V$, $R_L = 50\Omega$, and switching characteristics are for $V_{in} = 100mV$, $V_{od} = 5mV$.)

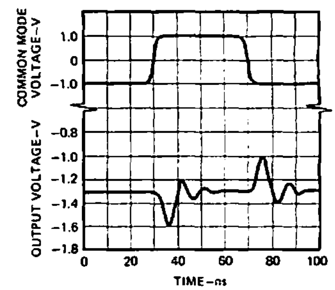
Set-up Time as a Function of Temperature



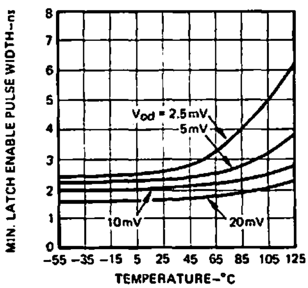
Set-up Time as a Function of Input Overdrive



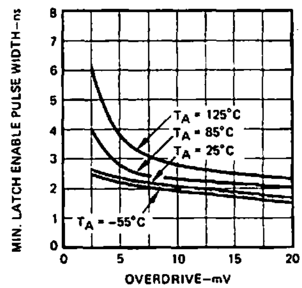
Common Mode Pulse Response



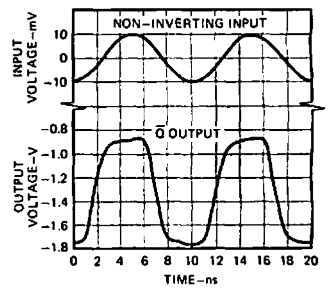
Min. Latch Enable Pulse Width as a Function of Temperature



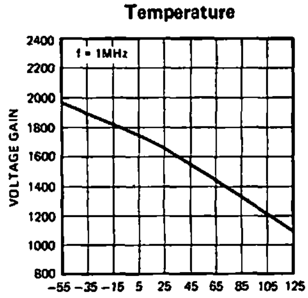
Min. Latch Enable Pulse Width as a Function of Input Overdrive



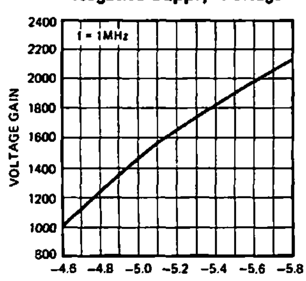
Response to 100MHz Sine Wave



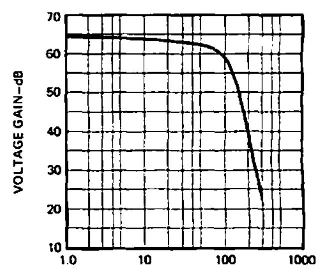
Voltage Gain as a Function of Temperature



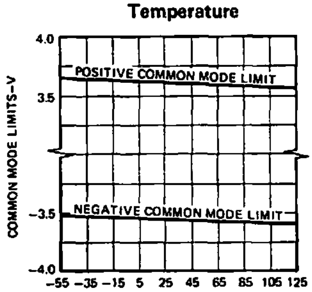
Voltage Gain as a Function of Negative Supply Voltage



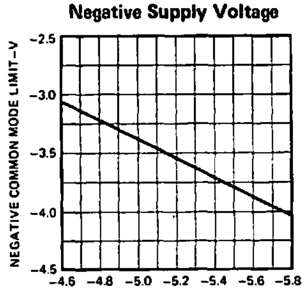
Voltage Gain as a Function of Frequency



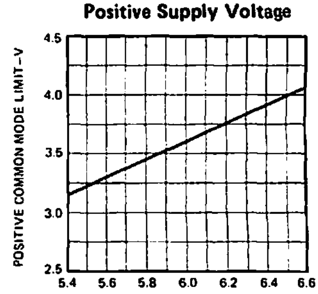
Common Mode Limits as a Function of Temperature



Negative Common Mode Limit as a Function of Negative Supply Voltage



Positive Common Mode Limit as a Function of Positive Supply Voltage

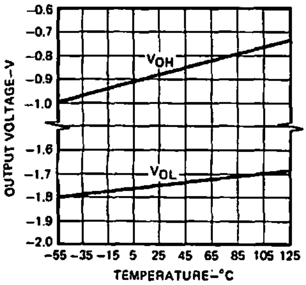


LIC-125

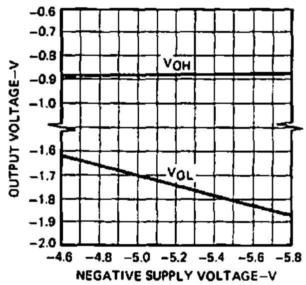
PERFORMANCE CURVES (Cont.)

(Unless otherwise specified, standard conditions for all curves are $T_A = 25°C$, $V^+ = 6.0V$, $V^- = -5.2V$, $V_T = -2.0V$, $R_L = 50\Omega$, and switching characteristics are for $V_{in} = 100mV$, $V_{od} = 5mV$.)

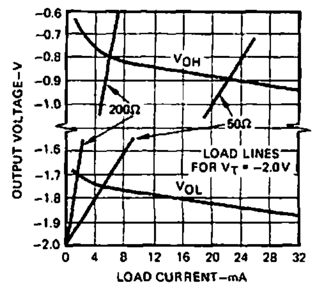
Output Levels as a Function of Temperature



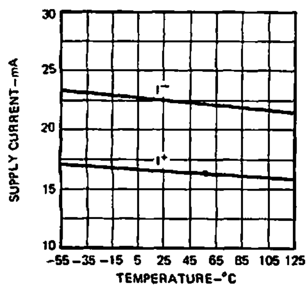
Output Levels As A Function Of Negative Supply Voltage



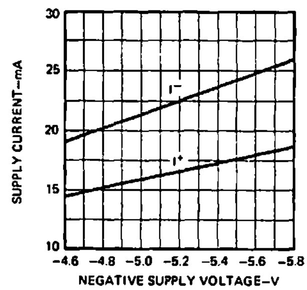
Output Levels As A Function Of DC Loading



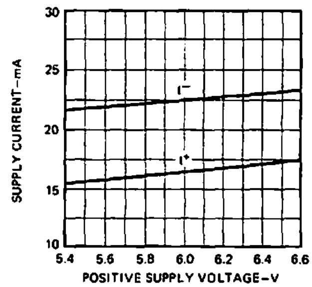
Supply Currents As A Function Of Temperature



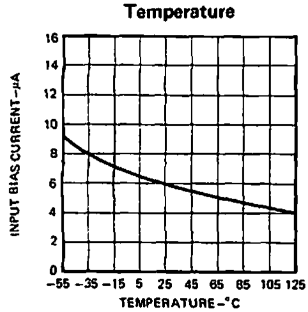
Supply Currents As A Function Of Negative Supply Voltage



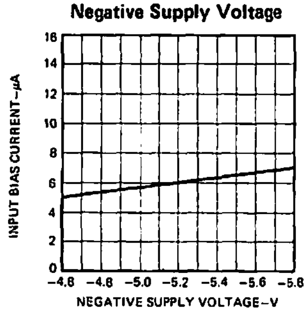
Supply Currents As A Function Of Positive Supply Voltage



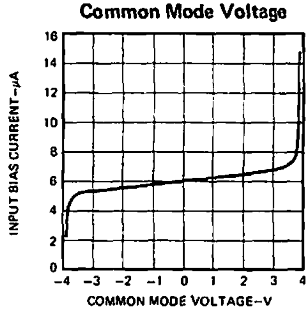
Input Bias Current As A Function Of Temperature



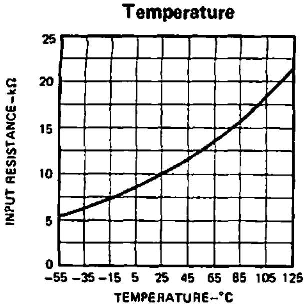
Input Bias Current As A Function Of Negative Supply Voltage



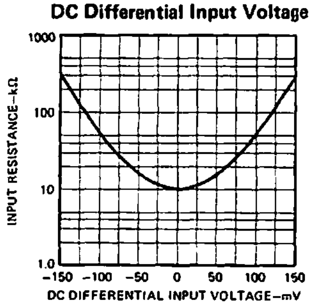
Input Bias Current As A Function Of Common Mode Voltage



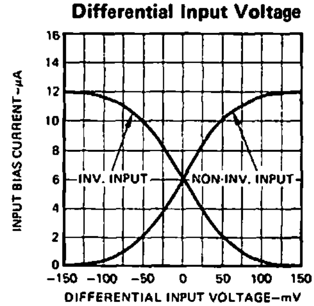
Input Resistance As A Function Of Temperature



Input Resistance As A Function Of DC Differential Input Voltage



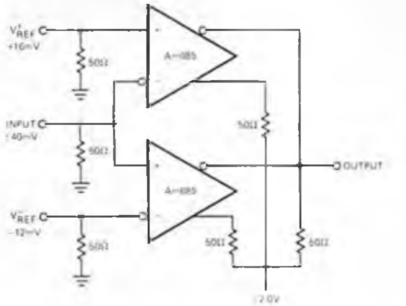
Input Current As A Function Of Differential Input Voltage

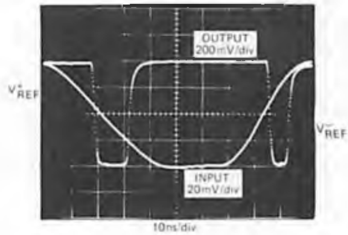


LIC-126

TYPICAL APPLICATIONS
($T_A = 25°C$)

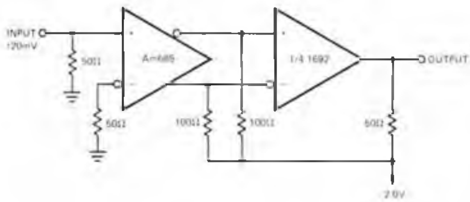
High-Speed Window Detector

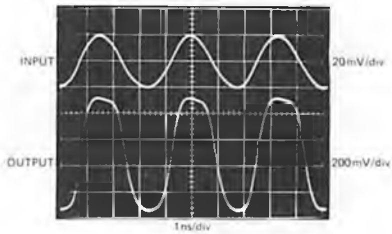




LIC-127

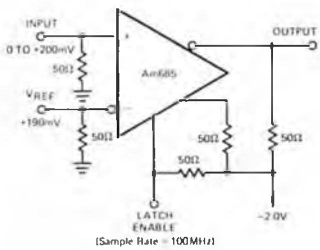
300MHz Line Receiver

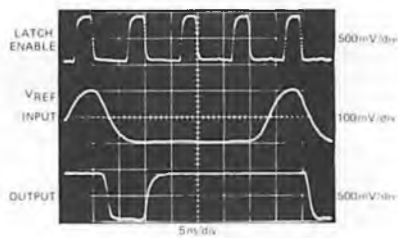




LIC-128

High-Speed Sampling

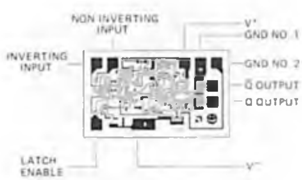




LIC-129

Metallization and Pad Layout

32 x 54 Mils



Am686

Voltage Comparator

Distinctive Characteristics

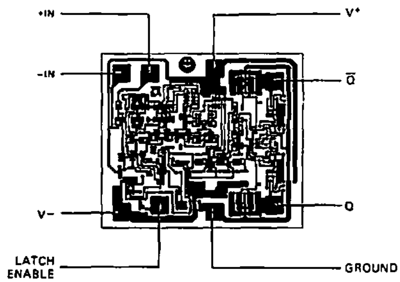
- 12ns MAXIMUM PROPAGATION DELAY AT 5mV OVERDRIVE
- *Complementary* Schottky TTL outputs
- Fanout of 5
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically and optically inspected dice for assemblers of hybrid products.
- Available in metal can and hermetic dual-in-line packages.

FUNCTIONAL DESCRIPTION

The Am686 is a fast voltage comparator manufactured with an advanced bipolar NPN, Schottky diode high-frequency process that makes possible very short propagation delays without sacrificing the excellent matching characteristics hitherto associated only with slow, high-performance linear IC's. The circuit has differential analog inputs and complementary logic outputs compatible with Schottky TTL. The output current capability is adequate for driving 5 standard Schottky inputs. The low input offset and high resolution make this comparator especially suitable for high-speed precision *analog-to-digital* processing.

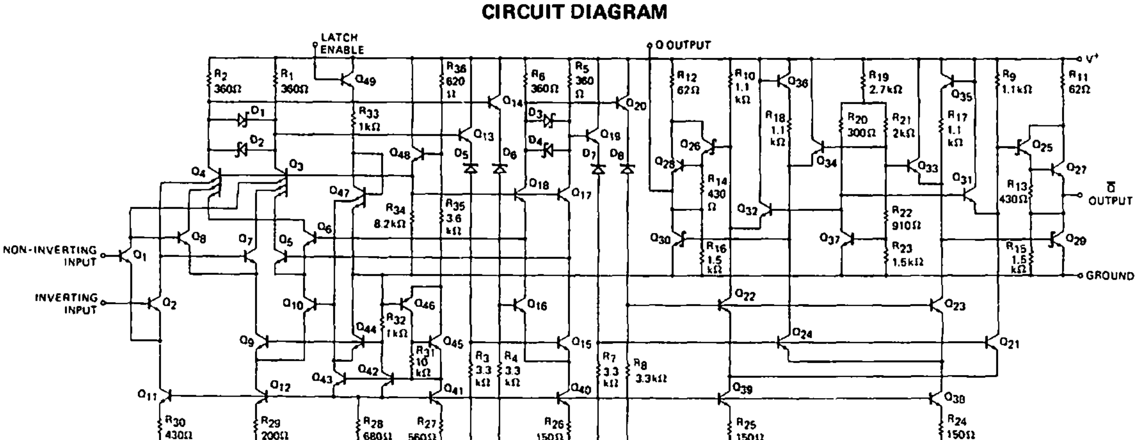
A latch function is provided to allow the comparator to be used in a sample-hold mode. If the Latch Enable input is LOW, the comparator functions normally. When the Latch Enable is driven HIGH, the comparator outputs are locked in their existing logical states. If the latch function is not used, the Latch Enable may be left open or connected to ground.

Metallization and Pad Layout



46 X 53 Mils

CIRCUIT DIAGRAM



LIC-130

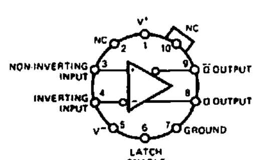
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am686	Metal Can	0°C to 70°C	Am686HC
	DIP	0°C to 70°C	Am686DC
Am686	Metal Can	−55°C to +125°C	Am686HM
	DIP	−55°C to +125°C	Am686DM
Am686	Dice	0°C to 70°C	Am686XC
	Dice	−55°C to +125°C	Am686XM

CONNECTION DIAGRAMS

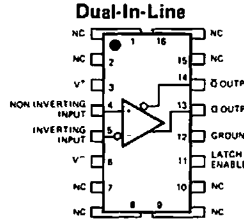
Top Views

Metal Can



LIC-131

Dual-In-Line



Note 1: On metal package, pin 6 is connected to case. On DIP, pin 6 is connected to case.

LIC-132

MAXIMUM RATINGS (Above which the useful life may be impaired)

Positive Supply Voltage	+7V
Negative Supply Voltage	−7V
Input Voltage	±4V
Differential Input Voltage	±6V
Power Dissipation (Note 2)	600mW
Lead Temperature (Soldering, 60 sec.)	300°C
Storage Temperature Range	−65°C to +150°C

Operating Temperature Range	
Am686-C	0°C to +70°C
Am686-M	−55°C to +125°C
Operating Supply Voltage Range	
Am686-C	V^+ = +5.0V ±5%, V^- = −6.0V ±5%
Am686-M	V^+ = +5.0V ±10%, V^- = −6.0V ±10%
Minimum Operating Voltage (V^+ to V^-)	9.7V

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

DC Characteristics

Symbol	Parameter	Conditions (Note 3)	Am686-C	Am686-M	Units
V_{OS}	Input Offset Voltage	R_S < 100Ω, T_A = 25°C	3.0	2.0	mV MAX.
		R_S < 100Ω	3.5	3.0	mV MAX.
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	R_S < 100Ω	10	10	μV/°C MAX.
I_{OS}	Input Offset Current	25°C < T_A < T_A (max.)	1.0	1.0	μA MAX.
		T_A = T_A (min.)	1.3	1.6	μA MAX.
I_B	Input Bias Current	25°C < T_A < T_A (max.)	10	10	μA MAX.
		T_A = T_A (min.)	13	16	μA MAX.
V_{CM}	Input Voltage Range		+2.7, −3.3	+2.7, −3.3	V MIN.
CMRR	Common Mode Rejection Ratio	R_S < 100Ω, −3.3V < V_{CM} < +2.7V	80	80	dB MIN.
SVRR	Supply Voltage Rejection Ratio	R_S < 100Ω	70	70	dB MIN.
V_{OH}	Output HIGH voltage	I_L = −1.0mA, V_S = V_S (min.)	2.7	2.5	V MIN.
V_{OL}	Output LOW Voltage	I_L = 10mA, V_S = V_S (max.)	0.5	0.5	V MAX.
I^+	Positive Supply Current		42	40	mA MAX.
I^-	Negative Supply Current		34	32	mA MAX.
P_{DISS}	Power Dissipation		415	400	mW MAX.

Switching Characteristics (V^+ = +5.0V, V^- = −6.0V, V_{in} = 100mV, V_{od} = 5.0mV, C_L = 15pF) (Note 4)

t_{pd+}	Propagation Delay, Input to Output HIGH	T_A (min.) < T_A < 25°C	12	12	ns MAX.
		T_A = T_A (max.)	15	15	ns MAX.
t_{pd-}	Propagation Delay, Input to Output LOW	T_A (min.) < T_A < 25°C	12	12	ns MAX.
		T_A = T_A (max.)	15	15	ns MAX.
Δt_{pd}	Difference in Propagation Delay between Outputs	T_A = 25°C	2.0	2.0	ns MAX.

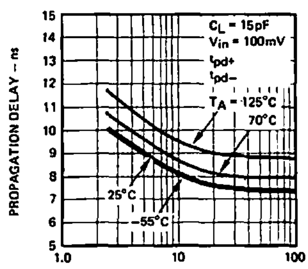
Notes: 2. For the metal can package, derate at 6.8mW/°C for operation at ambient temperatures above +95°C; for the dual-in-line package, derate at 9mW/°C for operation at ambient temperatures above 115°C.

3. Unless otherwise specified, V^+ = +5.0V, V^- = −6.0V and the Latch Enable input is at V_{OL}. The switching characteristics are for a 100mV input step with 5.0mV overdrive.

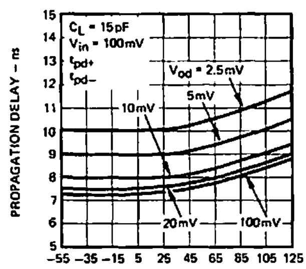
4. The outputs of the Am686 are unstable when biased into their linear range. In order to prevent oscillation, the rate-of-change of the input signal as it passes through the threshold of the comparator must be at least 1V/μs. For slower input signals, a small amount of external positive feedback may be applied around the comparator to give a few millivolts of hysteresis.

PERFORMANCE CURVES

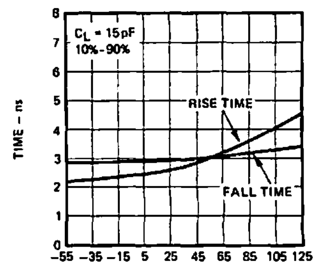
Propagation Delays as a Function of Input Overdrive



Propagation Delays as a Function of Temperature



Output Rise and Fall Times as a Function of Temperature



LIC-133

Am687·Am687A

Dual Voltage Comparators

Distinctive Characteristics

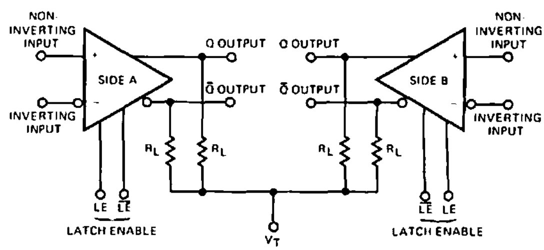
- 8.0ns MAXIMUM PROPAGATION DELAY AT 5mV OVERDRIVE
- Complementary ECL outputs
- 50Ω line driving capability
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically and optically inspected dice for assemblers of hybrid products.
- Available in the hermetic dual-in-line package.

FUNCTIONAL DESCRIPTION

The Am687 and Am687A are fast dual voltage comparators constructed on a single silicon chip with an advanced high-frequency process. The circuits feature very short propagation delays as well as excellent matching characteristics. Each comparator has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50Ω transmission lines. The low input offsets and short delays make these comparators especially suitable for high-speed precision analog-to-digital processing.

The comparators are similar to the Am685 high-speed comparator but have been designed to operate from a 5V positive supply (instead of 6V), dissipating less power than two Am685's. Separate latch functions are provided to allow each comparator to be independently used in a sample-hold mode. The Latch Enable inputs are intended to be driven from the complementary outputs of a standard ECL gate. If LE is HIGH and $\overline{LE}$ is LOW, the comparator functions normally. When LE is driven LOW and $\overline{LE}$ is driven HIGH, the comparator outputs are locked in their existing logical states. If the latch function is not used, LE must be connected to ground.

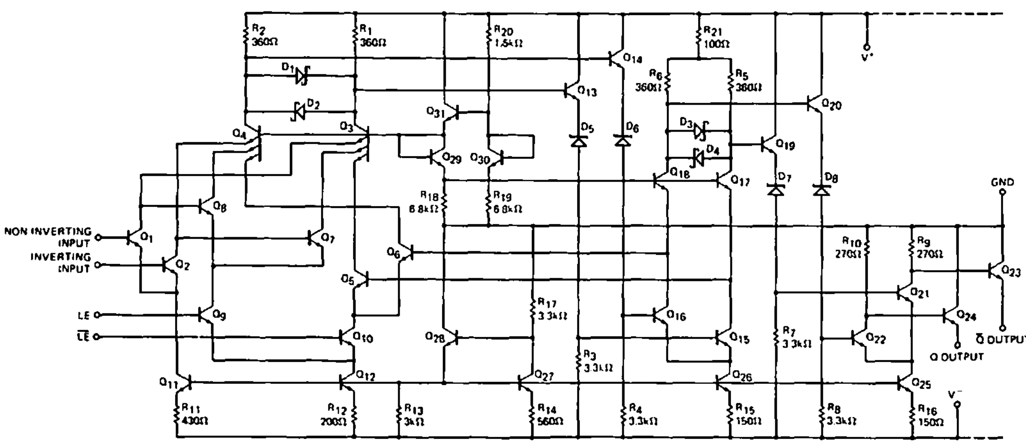
FUNCTIONAL DIAGRAM



LIC-134

The outputs are open emitters; therefore external pull-down resistors are required. These resistors may be in the range of 50-200Ω connected to −2.0V, or 200-2000Ω connected to −5.2V.

CIRCUIT DIAGRAM (Each Comparator)

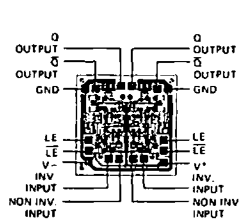


LIC-135

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am687A	DIP	−30°C to +85°C	AM687ADL
Am687A	DIP	−55°C to +125°C	AM687ADM
Am687	DIP	−30°C to +85°C	AM687DL
Am687	DIP	−55°C to +125°C	AM687DM
Am687	Dice	−30°C to +85°C	AM687XL
Am687	Dice	−55°C to +125°C	AM687XM

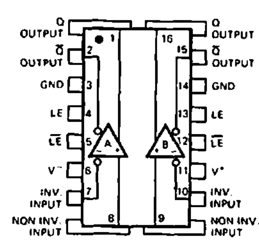
METALLIZATION AND PAD LAYOUT



DIE SIZE 0.056" X 0.056"

CONNECTION DIAGRAM

Top View



LIC-136

Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Positive Supply Voltage	+7 V
Negative Supply Voltage	–7 V
Input Voltage	±4 V
Differential Input Voltage	±6 V
Output Current	30 mA
Power Dissipation (Note 2)	600 mW

Operating Temperature Range	
Am687-L, Am687A-L	–30°C to +85°C
Am687-M, Am687A-M	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 Sec.)	300°C
Minimum Operating Voltage (V^+ to V^-)	9.7 V

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless otherwise specified)

DC Characteristics

Symbol	Parameter	Conditions (Note 3)	Am687A-L / Am687-L Min.	Am687A-L / Am687-L Max.	Am687A-M / Am687-M Min.	Am687A-M / Am687-M Max.	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\,\Omega$, $T_A = 25°C$	-3.0	+3.0	-2.0	+2.0	mV
		$R_S \leq 100\,\Omega$	-3.5	+3.5	-3.0	+3.0	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\,\Omega$	-10	+10	-10	+10	μV/°C
I_{OS}	Input Offset Current	$25°C \leq T_A \leq T_{A(max.)}$	-1.0	+1.0	-1.0	+1.0	μA
		$T_A = T_{A(min.)}$	-1.3	+1.3	-1.6	+1.6	μA
I_B	Input Bias Current	$25°C \leq T_A \leq T_{A(max.)}$		10		10	μA
		$T_A = T_{A(min.)}$		13		16	μA
V_{CM}	Input Voltage Range		-3.3	+2.7	-3.3	+2.7	V
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\,\Omega$, $-3.3 \leq V_{CM} \leq +2.7$ V	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\,\Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output HIGH Voltage	$T_A = 25°C$	-0.960	-0.810	-0.960	-0.810	V
		$T_A = T_{A(min.)}$	-1.060	-0.890	-1.100	-0.920	V
		$T_A = T_{A(max.)}$	-0.890	-0.700	-0.850	-0.620	V
V_{OL}	Output LOW Voltage	$T_A = 25°C$	-1.850	-1.650	-1.850	-1.650	V
		$T_A = T_{A(min.)}$	-1.890	-1.675	-1.910	-1.690	V
		$T_A = T_{A(max.)}$	-1.825	-1.625	-1.810	-1.575	V
I^+	Positive Supply Current			35		32	mA
I^-	Negative Supply Current			48		44	mA
P_{DISS}	Power Dissipation			485		450	mW

Switching Characteristics (V_{in} = 100 mV, V_{od} = 5 mV)

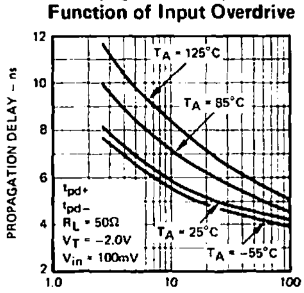
Symbol	Parameter	Conditions	L Min.	L Max.	M Min.	M Max.	Units
t_{pd+}, t_{pd-}	Propagation Delay, Am687A	$T_{A(min.)} \leq T_A \leq 25°C$		8.0		8.0	ns
		$T_A = T_{A(max.)}$		10		12.5	ns
t_{pd+}, t_{pd-}	Propagation Delay, Am687	$T_{A(min.)} \leq T_A \leq 25°C$		10		10	ns
		$T_A = T_{A(max.)}$		14		20	ns
t_s	Minimum Latch Set-up Time	$T_A = 25°C$		4.0		4.0	ns

Notes: 2. Derate at 9mW/°C for operation at ambient temperatures above +115°C.

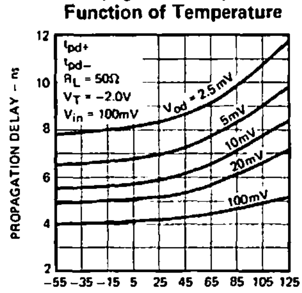
3. Unless otherwise specified V^+ = +5.0V, V^- = –5.2V, V_T = –2.0V, and R_L = 50Ω; all switching characteristics are for a 100mV input step wi[th] 5mV overdrive. The specifications given for V_{os}, I_{os}, I_B, CMRR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltage. The Am687 and Am687A are designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

PERFORMANCE CURVES

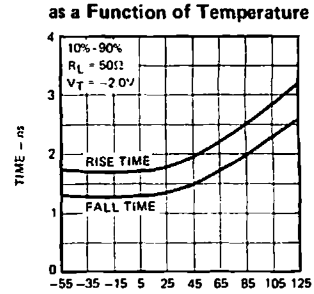
Propagation Delays as a Function of Input Overdrive



Propagation Delays as a Function of Temperature



Output Rise and Fall Times as a Function of Temperature



LIC-137

Am1500

Dual Precision Voltage Comparator

Distinctive Characteristics

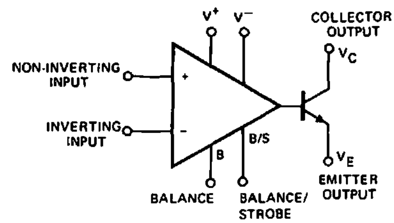
- The Am1500 is functionally, electrically, and pin-for-pin equivalent to the National LH2111
- The Am1500 is a dual 111, but requires 25% less power than two 111 comparators
- Output Drive – 50V and 50mA
- Input Bias Current – 150nA max.
- Input Offset Voltage – 4.0mV max.
- Differential Input Voltage Range – ±30V
- 100% reliability assurance testing in compliance with MIL-STD-883
- Available in Hermetic Dual-In-Line or Hermetic Flat Packages

2

FUNCTIONAL DESCRIPTION

The Am1500 is a voltage comparator featuring low input currents, high differential and common mode voltage ranges, wide supply voltage range, and outputs compatible with all bipolar and MOS circuitry. The inputs and outputs can be isolated from system ground, and the output can drive loads referred to ground or either supply. Strobing and offset balancing are available and the outputs can be wire-ORed.

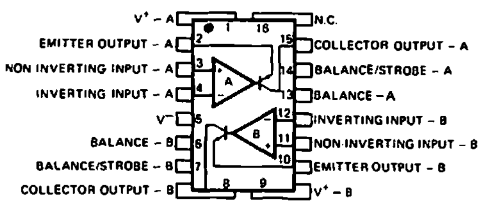
FUNCTIONAL DIAGRAM
(each half)



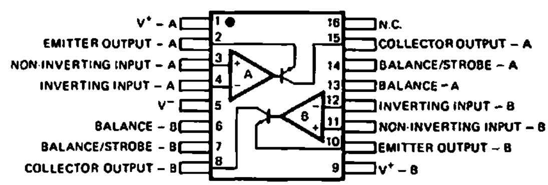
LIC-138

CONNECTION DIAGRAMS
Top Views

Dual In-Line



Flat Package



Note: Pin 1 is marked for orientation.

LIC-139

LIC-140

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am1500C	TO-99	0°C to +70°C	AM1500DC
	Hermetic DIP	0°C to +70°C	AM1500FC
Am1500L	TO-99	−25°C to +85°C	AM1500DL
	Hermetic DIP	−25°C to +85°C	AM1500FL
Am1500M	Hermetic DIP	−55°C to +125°C	AM1500DM
	Flat Pak	−55°C to +125°C	AM1500FM

MAXIMUM RATINGS

Voltage from V^+ to V^-	36V
Voltage from Collector Output to V^-	
Am1500M, L	50V
Am1500C	40V
Voltage from Emitter Output to V^-	30V
Voltage between Inputs	±30V
Voltage from Inputs to V^-	+30V, −0V
Voltage from Inputs to V^+	−30V
Power Dissipation (Note 1)	500mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	
Am1500M	−55°C to +125°C
Am1500L	−25°C to + 85°C
Am1500C	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

ELECTRICAL CHARACTERISTICS

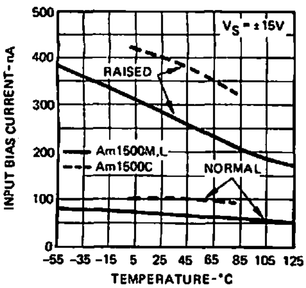
(T_A = 25°C unless otherwise specified) (Note 2)

Parameter (see definitions)	Conditions	Am1500C Min.	Am1500C Typ.	Am1500C Max.	Am1500M Am1500L Min.	Am1500M Am1500L Typ.	Am1500M Am1500L Max.	Units
Input Offset Voltage (Note 3)			2.0	7.5		0.7	3.0	mV
Input Offset Current (Note 3)			6.0	50.0		4.0	10.0	nA
Input Bias Current (Note 3)			100	250		60	100	nA
Response Time (Note 4)	R_L = 500Ω to +5V, V_E = 0		200			200		ns
Supply Current–Positive (Note 5) –Negative (Note 5)			3.9 2.6	7.5 5.0		7.0 4.8	9.5 7.5	mA
Voltage Gain			200			200		V/mV
Saturation Voltage	V_{in} < −5.0mV, I_C = 50mA V_{in} < −10mV, I_C = 50mA		 0.75	 1.5		0.75	1.5	V
Output Leakage Current	V_{in} > +5.0mV, V_C to V_E = 50V V_{in} > +10mV, V_C to V_E = 40V		 0.2	 50.0		0.2	10.0	nA
The Following Specifications Apply Over The Operating Temperature Range								
Input Offset Voltage (Note 3)				10.0			4.0	mV
Input Offset Current (Note 3)				70.0			20.0	nA
Input Bias Current (Note 3)				300			150	nA
Saturation Voltage	V_{in} < −6.0mV, I_C = 8.0mA V_{in} < −10mV, I_C = 8.0mA		 0.23	 0.40		0.23	0.40	V
Output Leakage Current	V_{in} > +6.0mV, V_C to V_E = 50V					0.1	0.5	μA
Input Voltage Range		±13	±14		±13	±14		V
Supply Current–Positive (Note 5) –Negative (Note 5)	T_A = +125°C					4.8 3.2	6.4 4.4	mA

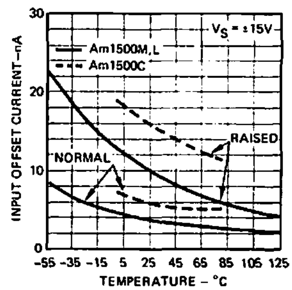
Notes:
1. For the Flat Package derate at 6.5mW/°C for operation at ambient temperatures above 83°C, and the Dual-In-Line at 9mW/°C for operation at ambient temperatures above 95°C.
2. Unless otherwise specified, these specifications apply for V^+ = +15V, V^- = −15V, V_E = −15V, and R_L at collector output = 7.5kΩ to +15V.
3. The offset voltage, offset current and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a 7.5kΩ load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
4. The response time specified (see definitions) is for a 100mV input step with 5.0mV overdrive.
5. The Am1500 supply current is the sum of the supply currents required by each side.

PERFORMANCE CURVES

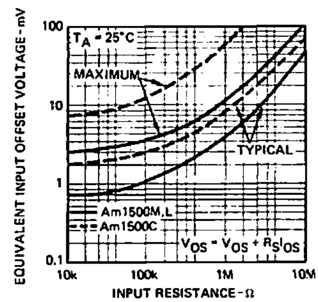
Input Bias Current



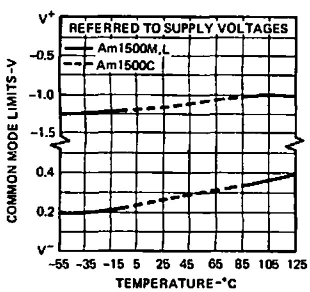
Input Offset Current



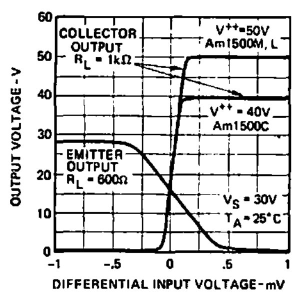
Offset Error



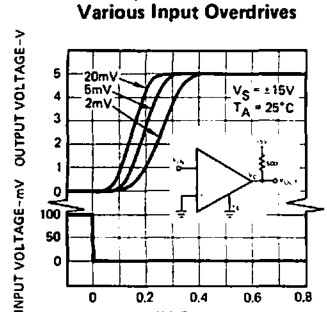
Common Mode Limits



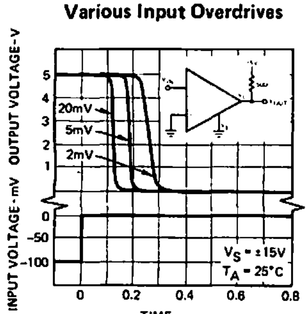
Transfer Function



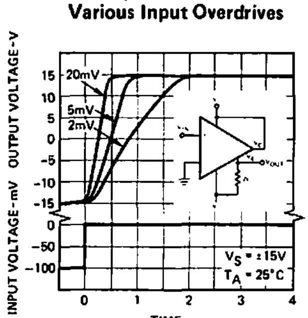
Response Time For Various Input Overdrives



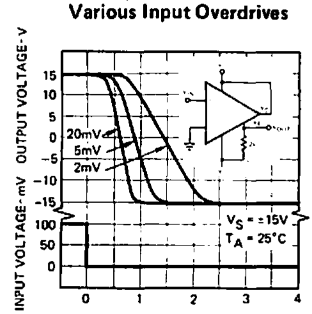
Response Time For Various Input Overdrives



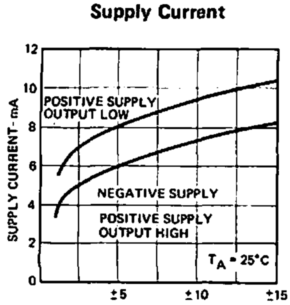
Response Time For Various Input Overdrives



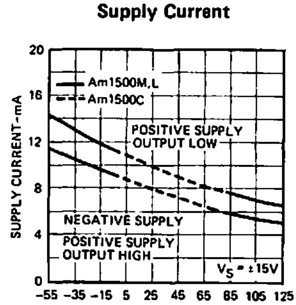
Response Time For Various Input Overdrives



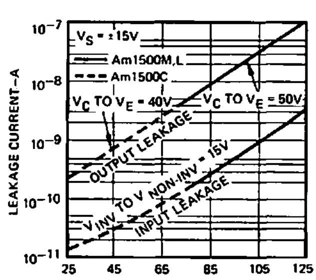
Supply Current



Supply Current



Leakage Current

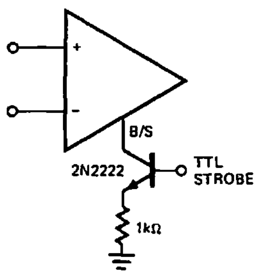


LIC-141

2

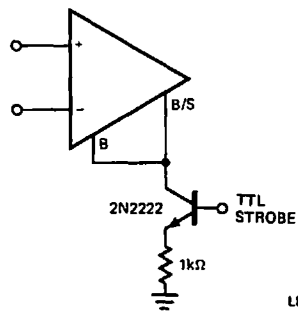
APPLICATIONS

Strobing



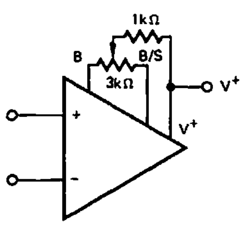
LIC-142

Strobing Off Both Input and Output Stages**



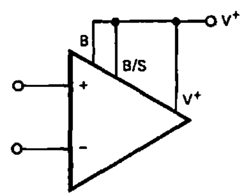
LIC-143

Offset Balancing



LIC-144

Increasing Input Stage Current*



LIC-145

*Increases input bias current and common-mode slew rate by a factor of 3.

**Typical input current = 50pA with inputs storbed OFF.

LH2111/2211/2311

Dual Precision Voltage Comparator

Distinctive Characteristics

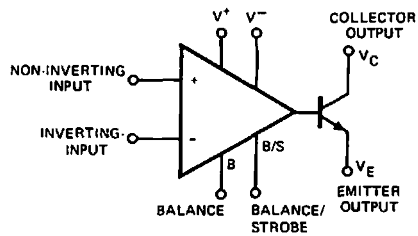
- The LH2111/2211/2311 are functionally, electrically, and pin-for-pin equivalent to the National LH2111/2211/2311
- The LH2111 is a dual 111, but requires 25% less power than two 111 comparators
- Output Drive – 50V and 50mA
- Input Bias Current – 150nA max.
- Input Offset Voltage – 4.0mV max.
- Differential Input Voltage – ±30V
- 100% reliability assurance testing in compliance with MIL-STD-883
- Available in Hermetic Dual-In-Line or Hermetic Flat Packages

2

FUNCTIONAL DESCRIPTION

The LH2111/2211/2311 are voltage comparators featuring low input currents, high differential and common mode voltage ranges, wide supply voltage range, and outputs compatible with all bipolar and MOS circuitry. The inputs and outputs can be isolated from system ground, and the output can drive loads referred to ground or either supply. Strobing and offset balancing are available and the outputs can be wire-ORed.

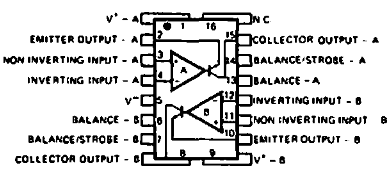
FUNCTIONAL DIAGRAM
(Each Half)



LIC-146

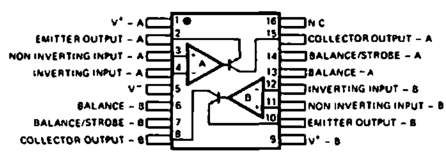
CONNECTION DIAGRAMS
Top Views

Dual-In-Line



LIC-147

Flat Package



LIC-148

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
LH2311	DIP	0°C - +70°C	LH2311D
	Flat Pak	0°C - +70°C	LH2311F
LH2211	DIP	–25°C - +85°C	LH2211D
	Flat Pak	–25°C - +85°C	LH2211F
LH2111	DIP	–55°C - +125°C	LH2111D
	Flat Pak	–55°C - +125°C	LH2111F

MAXIMUM RATINGS

Voltage from V^+ to V^-	36V
Voltage from Collector Output to V^-	
LH2111/LH2211	50V
LH2311	40V
Voltage from Emitter Output to V^-	30V
Voltage between Inputs	±30V
Voltage from Inputs to V^-	+30V, –0V
Voltage from Inputs to V^+	–30V
Power Dissipation (Note 1)	500mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	
LH2111	–55°C to +125°C
LH2211	–25°C to +85°C
LH2311	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

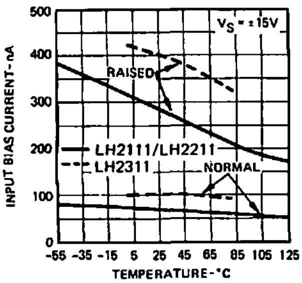
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 2)

Parameter (see definitions)	Conditions	LH2311 Min.	LH2311 Typ.	LH2311 Max.	LH2111 LH2211 Min.	LH2111 LH2211 Typ.	LH2111 LH2211 Max.	Units
Input Offset Voltage (Note 3)			2	7.5		0.7	3.0	mV
Input Offset Current (Note 3)			6.0	50.0		4.0	10.0	nA
Input Bias Current (Note 3)			100	250		60	100	nA
Response Time (Note 4)	R_L = 500Ω to +5V, V_E = 0		200			200		ns
Supply Current—Positive (Note 5)			3.9	7.5		7.0	9.5	mA
—Negative (Note 5)			2.6	5.0		4.8	7.5	mA
Voltage Gain			200			200		V/mV
Saturation Voltage	V_{IN} < –5mV, I_C = 50mA					0.75	1.5	V
	V_{IN} < –10mV, I_C = 50mA		0.75	1.5				V
Output Leakage Current	V_{IN} > +5mV, V_C to V_E = 50V					0.2	10.0	nA
	V_{IN} > +10mV, V_C to V_E = 40V		0.2	50.0				nA
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage (Note 3)				10.0			4.0	mV
Input Offset Current (Note 3)				70.0			20.0	nA
Input Bias Current (Note 3)				300			150	nA
Saturation Voltage	V_{IN} < –6mV, I_C = 8mA					0.23	0.40	V
	V_{IN} < –10mV, I_C = 8mA		0.23	0.40				V
Output Leakage Current	V_{IN} > +6mV, V_C to V_E = 50V					0.1	0.5	µA
Input Voltage Range		±13	±14		±13	±14		V
Supply Current—Positive (Note 5)	T_A = 125°C					4.8	6.4	mA
—Negative (Note 5)	T_A = 125°C					3.2	4.4	mA

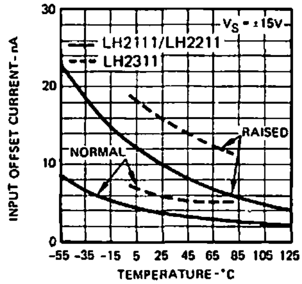
Notes: 1. For the Flat Package derate at 6.5 mW/°C for operation at ambient temperatures above 83°C, and the Dual-In-Line at 9 mW/°C for operation at ambient temperatures above 95°C.
2. Unless otherwise specified, these specifications apply for V^+ = 15V, V^- = –15V, V_E = –15V, and R_L at collector output = 7.5kΩ to +15V.
3. The offset voltage, offset current and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a 7.5kΩ load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
4. The response time specified (see definitions) is for a 100mV input step with 5mV overdrive.
5. The LH2111 supply current is the sum of the supply currents required by each side.

PERFORMANCE CURVES

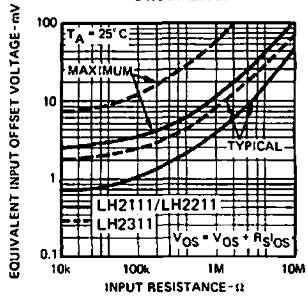
Input Bias Current



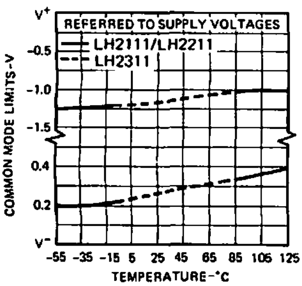
Input Offset Current



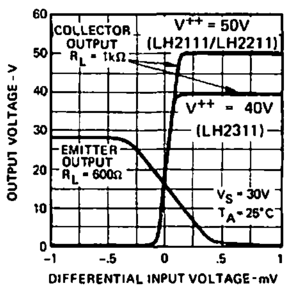
Offset Error



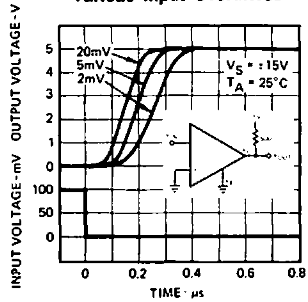
Common Mode Limits



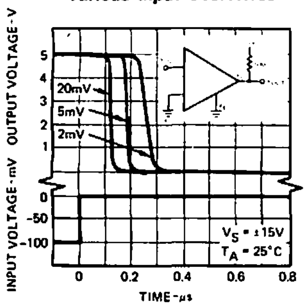
Transfer Function



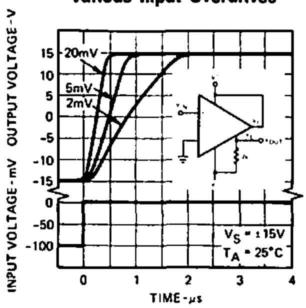
Response Time For Various Input Overdrives



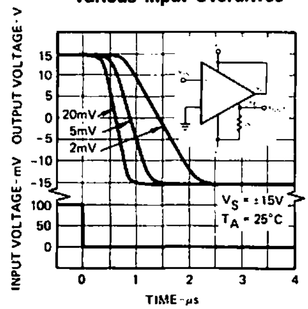
Response Time For Various Input Overdrives



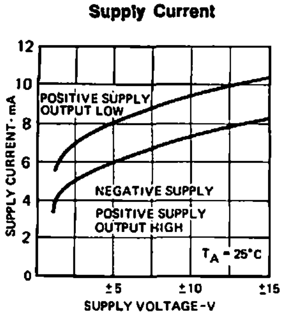
Response Time For Various Input Overdrives



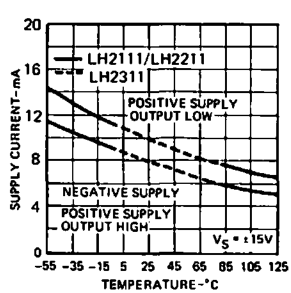
Response Time For Various Input Overdrives



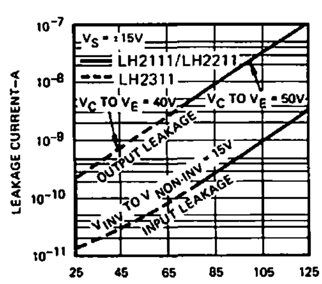
Supply Current



Supply Current



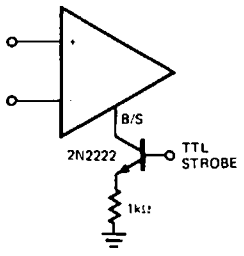
Leakage Current



LIC-149

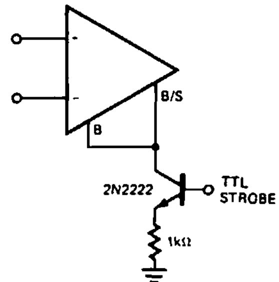
APPLICATIONS

Strobing



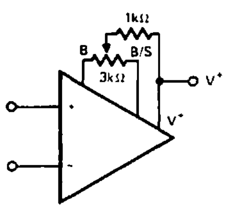
LIC-150

Strobing Off Both Input and Output Stages**



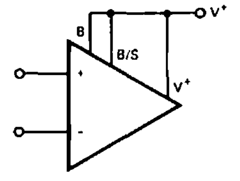
LIC-151

Offset Balancing



LIC-152

Increasing Input Stage Current*



LIC-153

*Increases input bias current and common-mode slew rate by a factor of 3.
**Typical input current = 50pA with inputs strobed OFF.

A NEW HIGH-SPEED COMPARATOR THE Am685

By Jim Giles and Alan Seales

INTRODUCTION

Modern electronic systems require more and more that operations be performed in a few nanoseconds so that the delay of the complete system, which may be very complex, be held to a minimum. There are abundant logic circuit elements available that meet this criterion: gold-doped TTL, Schottky TTL, and emitter-coupled logic (ECL), listed in descending order of propagation delay. Where it is necessary to interface from the analog world to the input of a logic system, or to detect very low-level logic signals in the presence of heavy noise, a high-speed precision comparator is needed. If such a comparator had a propagation delay less than 10ns, it could replace costly and complex circuitry that designers are now forced to use in very high-speed analog-to-digital converters, data acquisition systems, and optical isolators, as well as make possible many applications hitherto considered unfeasible. It could also be used as a sensitive line receiver or sense amplifier, in 100MHz sample and hold circuits, and in very high-frequency voltage-controlled oscillators.

The basic requirements for a high-speed precision comparator are few and well-defined: good resolution (high gain), high common-mode and differential voltage ranges, outputs compatible with standard logic levels, and, above all, very fast response to signal levels ranging from a few millivolts to several volts. The industry workhorse, the 710, has come close to meeting these requirements, and except for the most demanding applications, its 40ns propagation delay is adequate. A survey of presently available monolithic IC comparators (Table I) shows that there is really none that meets the requirements of very high-speed systems. The newer TTL-output circuits offer only marginal improvement over the 710 when measured under identical conditions of large input pulse and small overdrive, and the ECL-output comparator, although faster, has such poor resolution that it can be used only for large input signals. Advanced Micro Devices felt there was a need for a family of linear devices to fill the needs of very high-speed systems, with the first circuit being a precision comparator with less than 10ns delay.

Type No.	Logic Family	Propagation Delay	Resolution
Am111	TTL	200ns	0.012mV
μA710	TTL	40ns	1.4mV
Am106	TTL	40ns	0.06mV
μA760	TTL	25ns	0.5mV
NE527/529	TTL	25ns	0.5mV
MC1650	ECL	12ns	30mV

Table I: Propagation Delays of Available Monolithic IC Comparators (100mV Input Step, 5mV Overdrive)

DESIGN OBJECTIVES

In order to achieve the ultimate in speed, it is clear that the comparator outputs must be compatible with ECL, even though at present the majority of systems use TTL. Designers striving for the highest possible speed will already be using ECL in the critical circuit areas of their systems to squeeze the last possible nanosecond out of the overall delay. Further, an ECL circuit requires only one-third the gain of an equivalent TTL circuit for the same resolution owing to its smaller output logic swing. This means that lower impedances can be used and consequently larger bandwidth realized for the same power dissipation. Also, there is no problem interfacing the linear input stages with the digital output gate since an ECL gate is basically a non-saturating overdriven differential amplifier. Properly driving a TTL gate from a linear amplifier is more difficult, however, because it requires a large voltage swing suitably biased to track the input logic threshold with temperature, plus a large peak negative current capability to turn off the gate with minimum delay.

The usefulness and versatility of a comparator can be enhanced by adding a strobe or latch function to the circuit. A strobe simply forces the output of the comparator to one fixed state, independent of input signal conditions, whereas a latch locks the output in the logical state it was in at the instant the latch was enabled. The latch can thus perform a sample and hold function, allowing short input signals to be detected and held for further processing. If the latch is designed to operate directly upon the input stage—so the signal does not suffer any additional delays through the comparator—signals only a few nanoseconds wide can be acquired and held. A latch, therefore, provides a more useful function than a strobe for very high-speed processing.

The most difficult input signal for a comparator to respond to is a large amplitude pulse that just barely exceeds the input threshold. This forces the input stage of the comparator to swing from a full off (or on) state to a point somewhere near the center of its linear range. This exercises both the large-and small-signal responses of the stage. If the comparator has less than 10ns delay under these stringent conditions, then it should be as fast or faster for any other circumstances (see Figure 1). The industry standard measurement is with a

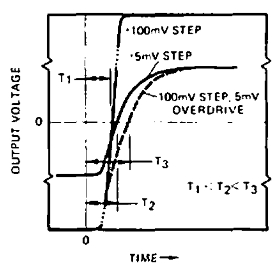


Figure 1. Response to step input signals at output of a differential amplifier

100mV input pulse and an overdrive 5mV above input threshold (this was used for the delays given in Table 1). Pulses larger than 100mV might be used, but this would multiply measurement difficulties, since only a few tenths of a percent aberration or ripple in the pulse generator waveform would be enough to seriously affect the accuracy of the small overdrive, and thus would give misleading results for the propagation delay.

To obtain satisfactory speed for all input signals and particularly for the worst case measurement conditions, the input stage of the comparator must have: 1) wide small-signal bandwidth, 2) high slew rate for large signals, 3) minimum voltage swings, and 4) high gain. The first requirement can be realized by using low-value load resistors, by making every effort in circuit design, device geometry and processing to minimize parasitic capacitances, and by using transistors with the highest f_T possible. The second item calls for high operating currents as well as minimum capacitance. The last two requirements are conflicting, since obtaining high gain normally requires a large voltage swing; therefore some means of clamping the swing must be used that does not degrade the propagation delay.

The overall gain of the complete comparator must also be high because, as illustrated in Figure 1, the propagation delay is less if each stage is well overdriven. To ensure that most of the input overdrive signal is actually used for overdriving, and not consumed in just moving the output from one state to the other, the gain error should be no more than about 10% of the input overdrive. Therefore, for a 5mV overdrive and an ECL output swing of 800mV, the minimum gain must be 1600. It is not practical to strive for much higher gain than this because the small-signal rise time begins to suffer as the stage gain increases. Addition of another stage is undesirable as this also adds delay and increases circuit complexity. It must be remembered that there is a maximum limit on power dissipation that a single integrated circuit package can handle adequately, and this consideration must influence the choice of operating currents and impedance levels throughout the design of the circuit.

With a figure for the total gain required, it is now possible to determine the number of stages and the gain per stage. Since the output stage must be ECL-compatible, its design is fixed, giving a differential-input to single-ended-output gain of about 6. This leaves a differential gain of 270 to be provided by the remainder of the comparator. This is most efficiently divided between two stages, each with a gain somewhat over 16. Both stages should be identical, since minimum overall delay time is obtained when identical stages are cascaded.

A factor not yet discussed that affects the accuracy of the comparator is its input offset voltage. Unless this is trimmed out initially, it must be added to the overdrive in determining the worse-case value of input signal for which the propagation delay specifications will be met. Even with trimming, the temperature drift of high-offset units is typically much greater than that of low-offset units. Therefore, it is desirable to have low initial offset so that trimming is not necessary, and so that the offset temperature coefficient will be good. Also affecting the offset voltage and its drift at higher source resistances are the input currents. To keep this contribution to the total offset low requires high current gains in the input transistors. Therefore, obtaining offsets in the 1–2mV range requires close attention to circuit design, mask layout, and very tight process control (equivalent to that needed for the high-performance, low-frequency operational amplifiers), but with the added kicker of f_Ts well above 1GHz.

As was mentioned, large common-mode and differential voltage ranges are desirable features of a comparator. The limits of the common-mode range in a well-designed circuit should be close to the supply voltages. Since a high-speed comparator will, of necessity, operate at fairly high current levels, the supply voltages must be low to stay within the package power dissipation limits. As a minimum, the common-mode range should be equal to or exceed the differential voltage range to take full advantage of the voltage breakdown characteristics of the input transistors. The basic differential amplifier input stage has a differential voltage breakdown in the range of 5 to 6 volts; the design goal for the common mode range should thus be at least ±3 volts.

In summary, the design objectives for a high-speed precision comparator are as follows:

1) propagation delay <10ns measured at 100mV input step, 5 mV overdrive
2) ECL-compatible outputs
3) latch capability
4) gain >1600
5) input offset voltage <±2mV
6) common-mode range >±3V

CIRCUIT DESIGN

The watchword in designing wideband circuits is simplicity – have the fewest possible active devices in the signal path, the lowest possible impedance levels, and the lowest possible capacitance. The simple, common-emitter differential amplifier can be designed to approach these ideals with one major exception: the deleterious shunting effect of the collector-to-base capacitance upon the driving source resistance is multiplied by the voltage gain of the stage (Miller effect). Even though the impedance levels will be only a few hundred ohms at most, this condition cannot be tolerated if maximum speed is to be achieved. The solution is to add an additional pair of common-base transistors to form a differential cascode amplifier (Figure 2). This circuit has all of the performance features of a common-emitter amplifier and no feedback capacitance.

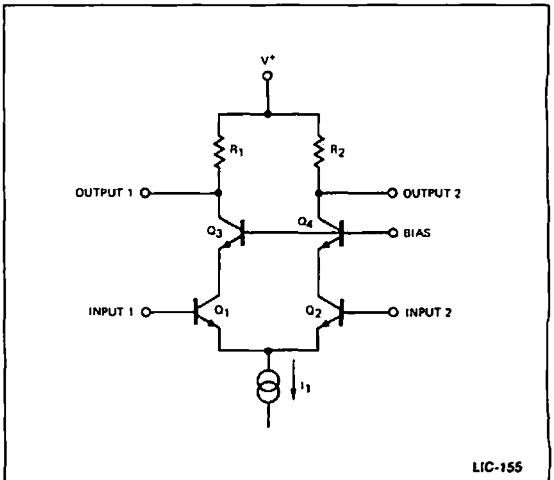


Figure 2. Differential cascode amplifier

Further advantages of the cascode will become apparent later when the latch design is discussed. The only drawback is that there are more devices in the signal path, the positive common-mode range is reduced, and circuitry has to be provided to bias the cascode transistors.

It is now necessary to provide a means of shifting the signal at the output of the cascode (which is very near the positive supply voltage) down to a lower voltage to drive the inputs of the second stage. The use of PNPs is definitely out because of their poor frequency response. This leaves three possibilities: a chain of forward-biased diodes, a programmed voltage drop across a resistor, or a zener diode. The diode chain is useful for level shifts of only a few volts at most, above that, the number of diodes gets too large, with a consequent increase in shunt capacitance and temperature coefficient. The use of a current-source/resistor combination is in the wrong direction for keeping impedance levels low. The resistors could be bypassed with capacitors, but this would offer only marginal improvement, since integrated capacitors have a large shunt component to the substrate. Besides, the addition of four capacitors (for both stages) would result in a large increase in chip area.

The zener diode is definitely superior for high-frequency applications because its shunt capacitance to ground is low, being equal to the collector-to-base capacitance of a transistor. It has no capacitance to the substrate, and its dynamic resistance is quite low. It does have the disadvantage that the level shift is limited to one voltage (6V), which restricts the range of power supply variation the circuit can tolerate. In addition it requires very tight control of the manufacturing process to maintain the matching required. For an input stage gain of 16 the zener voltages have to be matched to better than 0.25% to produce less than 1mV offset voltage at the input.

As shown in Figure 3, the zeners are buffered from the cascode collectors by emitter followers. The pulldown current through the zener-follower combination must be made large enough to discharge the node capacitance when the follower swings in the negative direction. The minimum value necessary is determined by the node capacitance, the signal swing, and the amount of delay that can be tolerated. The amount of signal swing can be reduced by adding clamping diodes across the collectors of the cascode. Regular diode-connected transistors could be used, but would add considerable collector-to-substrate capacitance across the load resistors as well as base-to-emitter capacitance between them. Schottky diodes, on the other hand, require little additional chip area, and are very fast. With clamping, some of the common-mode range lost when the cascode was added can be regained because the cascode transistors can be biased closer to the positive supply without fear of going into saturation at the extremes of the signal swing. The use of Schottky diodes, however, puts a few more gray hairs on the head of the process engineer since he has to control another set of characteristics without affecting the other parameters. The circuit values given in Figure 3 are designed for a minimum differential gain of 16, and a minimum negative-going slew rate at the output of the level-shifter of 1000V/μs.

As mentioned earlier the design of the output stage (Figure 4) can vary little from that of a standard ECL gate. The output emitter followers have to be large enough to handle loading by a 50Ω transmission line (25mA), yet small enough not to add a lot of capacitance that would slow down the response. Therefore, the transistor design must be as efficient as possible with regard to physical size and current-carrying

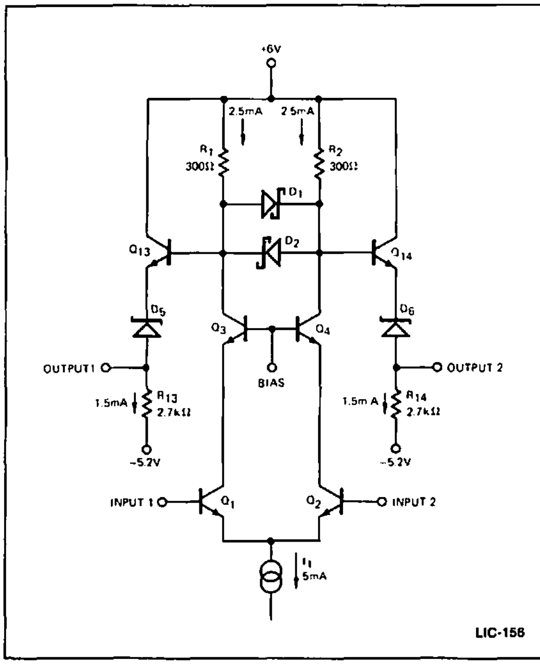


Figure 3. Basic cascode gain stage

capacity. Since the input common-mode level to the gate varies with changes in the power supplies and resistor tolerance, a current source is used to supply the emitters of the gate, rather than the usual resistor to the negative supply. The design of this current source must be such as to provide the correct logical "1" and "0" levels at the output and the proper variation with temperature and power supply changes. The propagation delays to either output of this gate will be equal, whereas they are slightly different in a standard ECL gate owing to the additional capacitive loading on the $\overline{Q}$ output caused by the multiple input transistors.

Implementation of the latch function must be accomplished without interfering with the normal comparator operation or degrading the speed in any way. It must be as close to the input as possible to permit short input signals to be acquired and held. One simple method of adding a latch to a differential

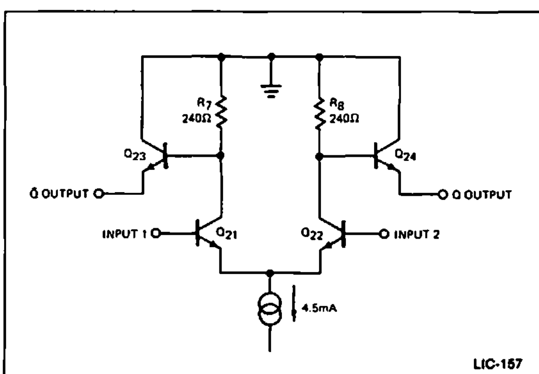


Figure 4. Output gate

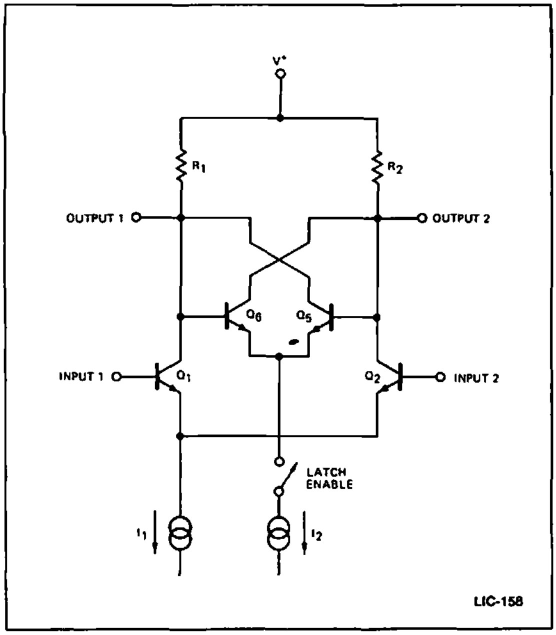


Figure 5. Simple latch circuit

amplifier is shown in Figure 5. A pair of transistors, Q_5 and Q_6, are cross-coupled at the collectors of the input transistors, Q_1 and Q_2. The current source I_2 is switched on when it is desired to enable the latch. If I_2 is greater than I_1, the positive feedback via Q_5 and Q_6 will hold the circuit in whatever state it was in when the latch was turned on.

The simple circuit of Figure 5 is not the best for speed because of the added capacitance of Q_5 and Q_6 and the fact that they can saturate unless the signal swings are very small. However, it can be adapted to the cascode stage quite nicely as illustrated in Figure 6. Drive for the positive feedback transistors is taken from the level shifters, and the collectors go to the emitters of the cascode. With this arrangement there is no significant capacitive loading on the gain stage at all. The current source is switched by another differential amplifier, Q_9–Q_{10}, referenced to the ECL logic threshold voltage. This provides the correct input levels for the Latch Enable being driven from a standard ECL gate as well as being very fast, since only currents are being switched.

The latch current source (I_2) must be about 1mA greater than the input current source (I_1) to ensure positive latching for any condition of input signal. Thus, for 5mA in the input stage, at least 6mA must be used to power the latch. This amounts to a lot of power consumed for a function that some users may never even need. However, there is a way to cut the latch standby power down to zero; this is accomplished by the addition of Q_7 and Q_8, as shown in Figure 8.

To understand the function of these transistors, first refer to Figure 7. The differential voltage appearing across the emitters of the cascode transistors is equal to the input signal (for small input signals). This is because the currents through the lower pair of transistors in the cascode are equal to the corresponding currents through the upper pair, and the transistors are matched; therefore the differences in base-emitter voltages must be equal. Thus, Q_7 and Q_8 function as if they were

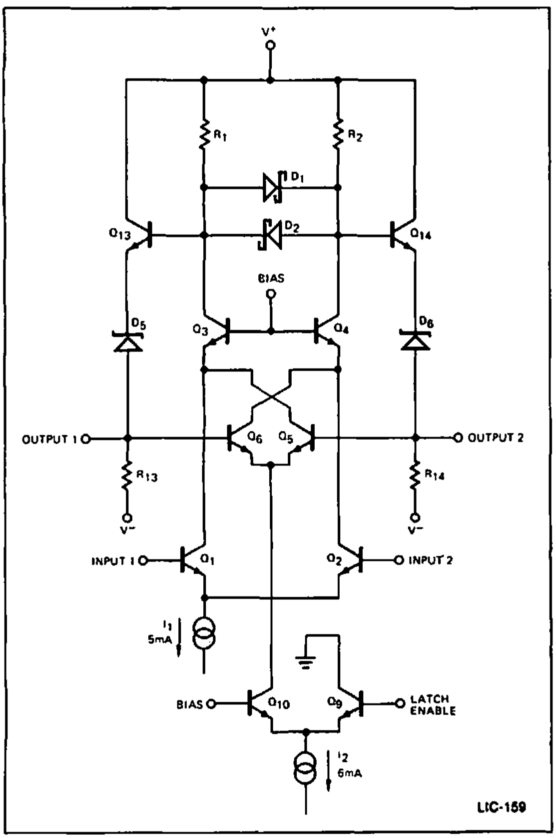


Figure 6. Cascode with latch

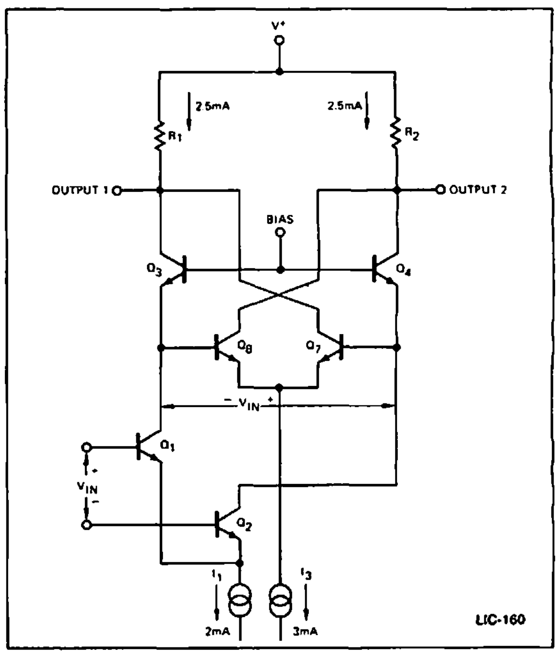


Figure 7. Cascode with "parallel" transistors

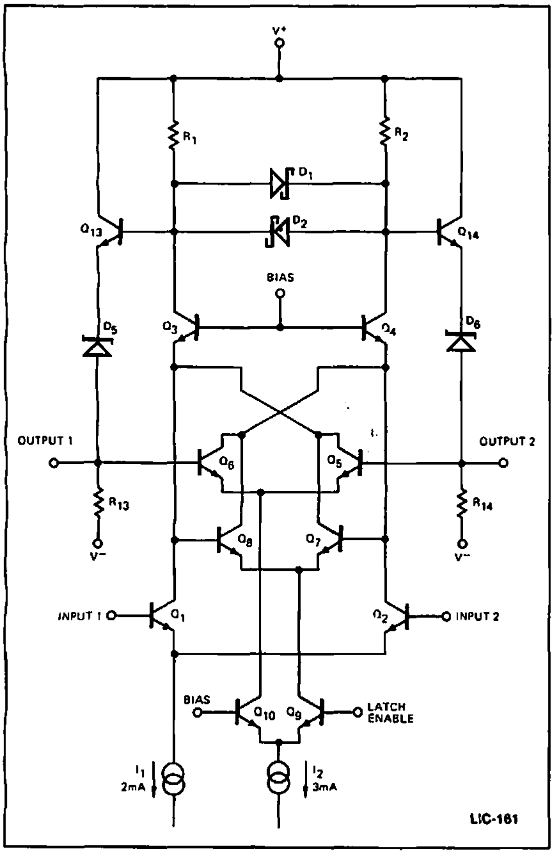


Figure 8. Complete input cascode stage with latch

simply connected in parallel with Q_1 and Q_2, as far as the net effect at the collector load resistors is concerned. To obtain the desired total stage gain, the current I_1 can be 2mA and I_3 *can be 3mA.*

Now refer to Figure 8. With the latch enable HIGH, Q_9 will be switched on and the 3mA current source will be supplied to the parallel transistors, Q_7–Q_8. The comparator functions normally, and no current is used up in the latch. When the latch enable goes LOW, I_2 will be switched through Q_{10} to the positive feedback transistors, robbing 3mA from the gain stage and giving it to the latch. The latch current is now 1mA greater than the input stage current, but the total current required is still only 5mA. As with the latch transistors, the collectors of the parallel transistors are connected to the emitters of the cascode, so no additional capacitance is added across the load resistors. This places the requirement on Q_7 and Q_8 that they maintain their high f_T at zero collector-to-base voltage.

The use of the parallel transistors has the added bonus that the input bias currents are decreased by more than a factor of two, thus reducing their influence on the offset voltage. The penalty paid is that all three pairs of junctions (Q_1–Q_2, Q_3–Q_4 and Q_7–Q_8) add equally to the input offset. Once again, the processing must be carefully controlled to keep the overall offset within the 2mV goal.

The complete circuit of the comparator is given in Figure 9. It includes some additional refinements as well as the DC biasing. The drive for the latching transistors is taken from the emitters of the second cascode rather than from the level-shifting zeners. This removes their input capacitance from the level shifter and also ensures that Q_{10} cannot saturate. A resistor (R_8) is included to center the common-mode voltage at the input to the gate within its dynamic range; this prevents saturation of the gate or its current source over the expected range of signal swing, temperature drift and supply voltage variations. A separate ground is used for the output emitter followers so that heavy loading at the output will not couple back into the remainder of the circuit. The DC bias chain for the current sources is referenced to ground and the negative supply, so the output logic levels will track those of other ECL circuits connected to the same negative supply. The current sources are designed to stay constant with temperature, which keeps the open-loop gain high at elevated temperatures (>1000 at +125°C), and thus helps to maintain good propagation delay.

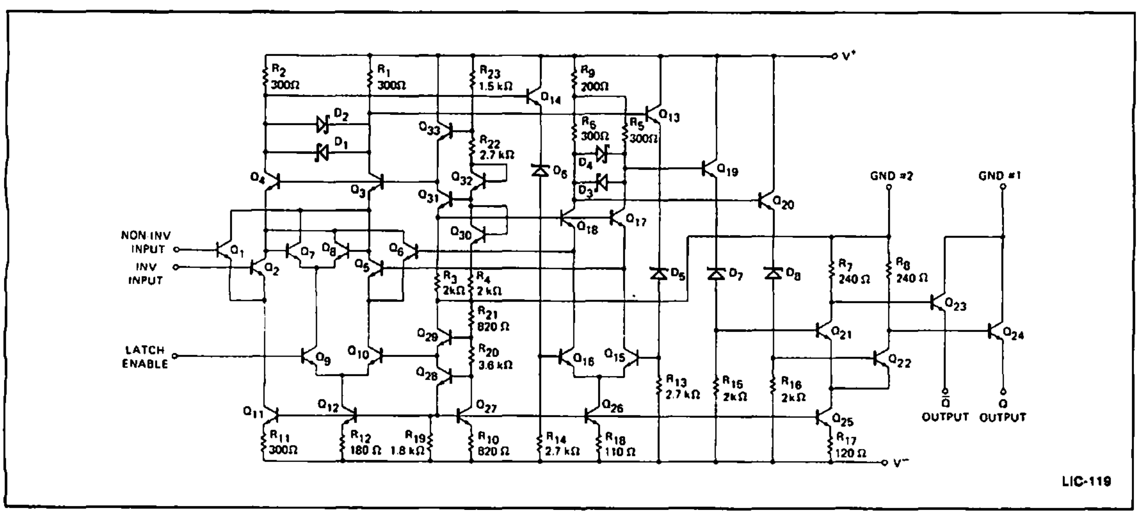


Figure 9. Complete schematic of the Am685 comparator

PROCESS TECHNOLOGY

Circuit design requirements for high speed and a latch function result in an input structure that has three pairs of transistors, the matching of which determines the offset voltage. This dictates that the matching of V_{BE} shall be extremely good between the transistors in each pair in order to meet the 2mV maximum offset voltage target. For the speeds necessary the transistor f_T has to be in the region above 1 GHz, so high-frequency performance can not be compromised. The slew rate of the input stage has to be very high for acceptable response with large input signals. This is achieved by high operating current and low stray capacitances. It is very desirable to keep both the input bias current and the input offset current very low so that the impedances in the source voltages do not introduce intolerable input voltage errors. It would be possible to use a Darlington-connected input stage to achieve these low currents, but the penalty exacted in offset voltage, offset voltage drift, and propagation delay is unacceptable, so high current-gain transistors that match extremely well are needed. The problems are thus centered on achieving very well-matched transistors with high beta and high f_T.

As previously mentioned, it is desirable in a comparator to have a wide common-mode voltage range and high power-supply rejection ratio. This is facilitated by using Schottky diodes to clamp the collector-to-collector swings in the first two stages. Schottky diodes can be fabricated simply by making a window in the oxide over the N-type epitaxial layer and using the same evaporated aluminum as is used for the interconnects (see Figure 10). The contact potential between silicon and aluminum causes a potential barrier to the flow of electrons. Making the metal positive lowers this barrier, allowing electrons to pass over it by virtue of their thermal energy. This process is essentially the same as thermionic emission. Since these electrons are majority carriers, Schottky diodes show extremely fast turn-off characteristics, desirable in this application. Why the Schottky diode is so attractive is that the forward voltage necessary to produce a given current may be several hundred millivolts less than that required to produce the same current in a p-n junction diode of about the same size. It can thus be used as a "clamp" to prevent a bipolar transistor from saturating, when connected from collector to base so as to prevent the forward voltage of the collector-base diode from rising to a level sufficient to cause appreciable current flow in the collector-base diode. This is the common application in Schottky TTL circuits.

In the ECL comparator the use is different. Here they are used back-to-back to limit the differential voltage swings between the collectors in both the first and the second stages. Connected in this way the reverse voltage seen by one Schottky diode is equal to the forward voltage drop of the other diode. Because this voltage is so small reverse leakage is not a great problem. In the simple Schottky diode structure, as described above, the reverse leakage is high. Most of this leakage current is generated at the perimeter of the metal, where there is an electric field concentration. In order to reduce this field the metal is extended all around the opening in the oxide, overlaying this oxide. Spacing the metal from the silicon in this way reduces the field and hence the leakage. In applications where low leakage is critical, the use of a P+ guard ring is called for, but this carries with it extra capacitance, so in view of the fact that the reverse voltage is so low the guard ring technique was discarded for this application. Even so, the diodes used in the comparator have low leakage characteristics with a breakdown at about 45V.

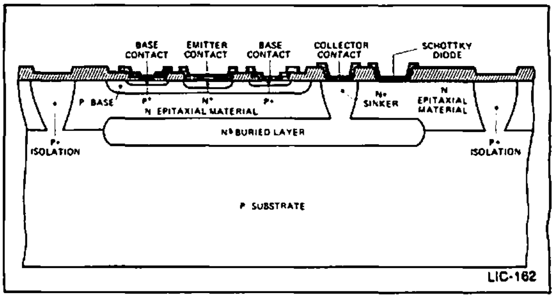


Figure 10. Cross section of transistor and Schottky diode showing sinker and P+ base contact enhancement

At the very high speeds being considered, much effort has to go into reducing capacitances and resistances. Thinning down the epitaxial layer to the minimum required to sustain the voltages encountered is of benefit in two ways: 1) the collector-isolation sidewall area is reduced, lowering the collector-to-substrate capacitance; 2) the collector-series resistance is reduced. The two major contributions to collector-series resistance are the resistance of the epitaxial material between the emitter and the buried N+ layer, and the resistance of the epitaxial layer between the collector contact and the buried layer. However, the first resistance is subject to reduction by conductivity modulation during operation of the device and thus is less important than the second term. The second term can be made very small by using a "sinker", which is a high concentration N-type diffusion from the surface, through the epitaxial layer, to the buried N+ layer. Contact to the collector is then made to the surface of the sinker. (see Figure 10)

Collector-to-base capacitance is held low by using very small dimensions and by using a relatively high epitaxial layer resistivity. The latter also serves to reduce the collector-to-substrate capacitance. A further reduction in collector-to-base capacitance results from using a shallow, high sheet-resistivity diffusion for the base. However, this raises the base resistance, both because the bulk resistance from the contact to the active base region is increased and because the specific contact resistance is increased. These resistances may be reduced by depositing P+ regions under the base contact areas after the main base diffusion.

A compromise has to be made in selecting emitter width. Large emitters are desirable for V_{BE} matching, but very small emitters are essential for high f_T. A stripe emitter, .25-mil wide and 1-mil long, was chosen as optimum. A difference in width, between two otherwise identical emitters, of .01-mil will be sufficient to cause an offset voltage of 1 mV. From this, it can be seen that the photolithography must be extremely carefully controlled, since the offset voltages of three pairs of transistors are summed to give the total offset of the comparator. Because the emitters are so narrow the normal procedure of making a contact cut inside of the emitter cannot be used. Instead, the emitter oxide is simply dissolved in hydrofluoric acid immediately before the aluminum evaporation in order to expose the emitter. As a consequence, the lateral distance between the metal and the emitter-base junction is very small, being equal to the lateral diffusion of the emitter. This means that the sintering process must be carried out at a temperature lower than is customary in linear circuit manufacture in order to avoid short-circuiting the

emitter-base junction by lateral migration of aluminum. An additional reason for lowering the sintering temperature is to avoid penetration of aluminum down through the emitter and base, causing emitter-to-collector shorts.

The requirement for high current gain, for low input bias currents, necessitates narrow base widths. Emitter-to-collector shorts can be a problem in these shallow, narrow-base structures. The probability of shorting can be minimized by careful cleaning procedures and by proper emitter doping levels. Keeping the emitter doping level low also reduces the magnitude of the "emitter dip" effect, whereby the diffusion coefficient of the boron in the region under the emitter is greatly increased by the lattice strain caused by the emitter, resulting in the running-on of the base under the emitter, making it very difficult to achieve a narrow base width.

An area that is neglected in digital circuit processing, because high beta is not necessary, but which is of major importance in linear processing, is the control of surface conditions. If high current gains are to be realized, both the surface area of the emitter-base-depletion region and the surface recombination velocity must be minimized. The former implies that ionic contamination, such as sodium ions, must be eliminated and that the surface state charge density, Qss, should be made as low as possible. The surface recombination velocity is proportional to the fast surface state density and so can be minimized by making this density very low. These three goals; low ionic contamination, low Qss and low fast surface state density are achieved by using the well known techniques of MOS and linear circuit processing, such as annealing in an inert atmosphere and proper choice of sintering cycle.

In the interests of minimum capacitance, the metal interconnects are designed to be narrower than is usual in linear circuits. Special etching techniques have to be employed in order to reproduce these narrow lines reliably. These lines can be seen in the photomicrograph of Figure 11.

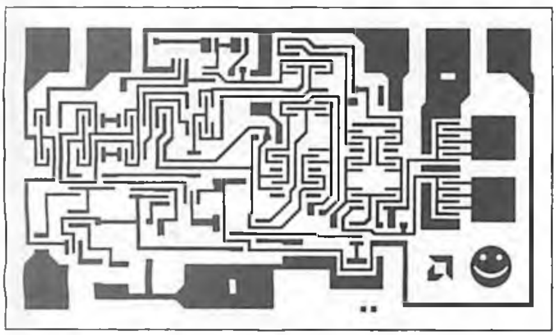


Figure 11. Photomicrograph of the Am685 comparator

PERFORMANCE

The primary design objective for the comparator was to obtain under 10ns propagation delay for large input signals with small overdrive. It should then be as fast or faster for any other input conditions. The performance of the Am685 comparator for a 100mV step input at various overdrives is shown in Figures 12 and 13. The propagation delay is measured from the time the input step crosses the input threshold voltage to the time the output crosses the logic threshold voltage. The input threshold voltage (i.e., the offset voltage) was adjusted for the figures so that the delay can be simply measured by

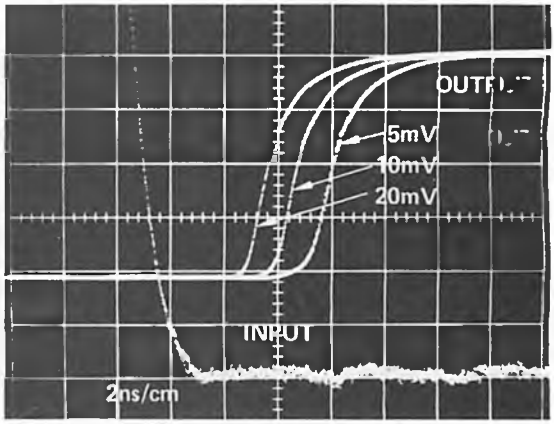


Figure 12. Tpd –"1" for 100mV step input and various overdrives (input = 5mV/cm, output = 200mV/cm)

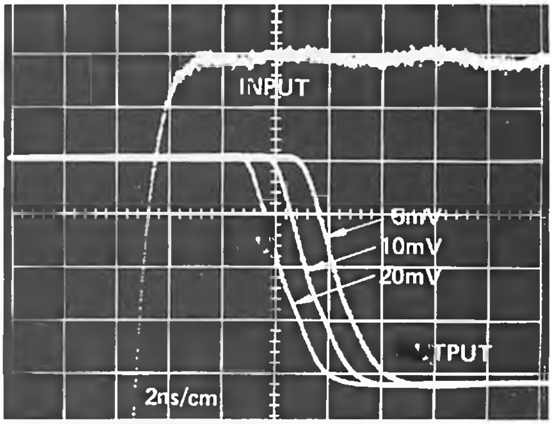


Figure 13. Tpd –"0" for 100mV step input and various overdrives (input = 5mV/cm, output = 200mV/cm)

counting up 5, 10, or 20mV from the bottom of the input pulse. The input pulse, therefore, is displayed on a magnified scale to facilitate this measurement and also to illustrate the purity of input signal required to make accurate measurements at millivolt overdrives.

For a 100mV input step and 5mV overdrive, the propagation delay for a logical "0" is 6.3ns and for a logical "1" is about 300ps less. A graph of delay as a function of overdrive is given in Figure 14. It was previously stated that any other condition

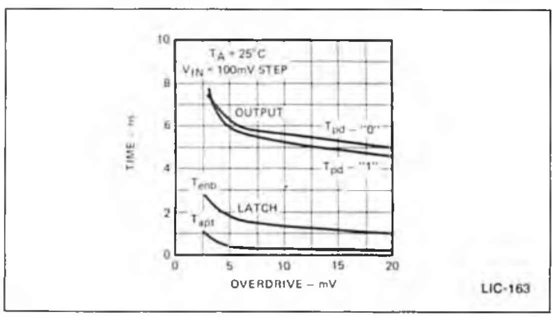


Figure 14. Delay times as a function of input overdrive

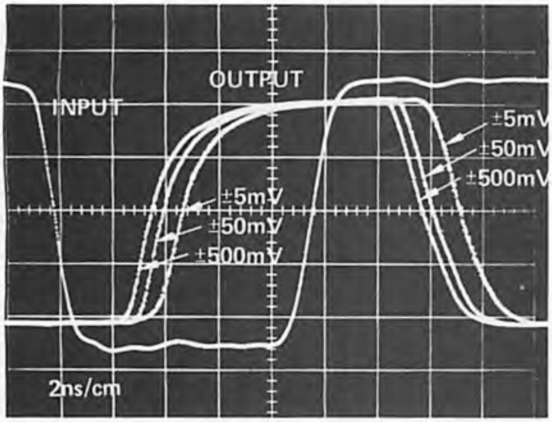
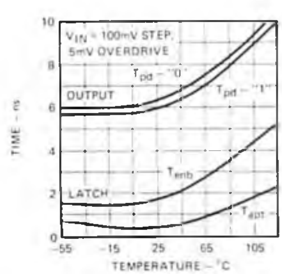


Figure 15. Response to symmetrical input signals

of input signal should give faster response (refer back to Figure 1). This is demonstrated by Figure 15, which illustrates the response of the comparator to symmetrical inputs ranging from ±5mV to ±500mV. The speeds are at least 1 to 2ns faster than for small overdrives.

Figure 16 shows how the delay time varies with temperature. The adverse effects of resistor and gain changes at elevated temperatures result in an increase in delay from 6.3ns at 25°C to 8.4 ns at 85°C and 10.4 ns at 125°C. All of the above data were taken with output loads of 50Ω connected to −2.0V. For lighter loading (such as 500Ω to −5.2V) the output rise and fall times and propagation delays are all slightly faster.

The usefulness of the latch is directly related to how quickly it can be enabled following a change in the input signal. The input signal must be present long enough to pass through the first stage of the comparator before the latching transistors can act upon it. The minimum time that the input must be present before the latch can be turned on is defined as the latch enable time. This is measured as the minimum time that must elapse



LIC-164

Figure 16. Delay times as a function of temperature

between the time the input step crosses the input threshold voltage and the time the latch enable input crosses the logic threshold voltage for which the comparator outputs will assume the correct states.

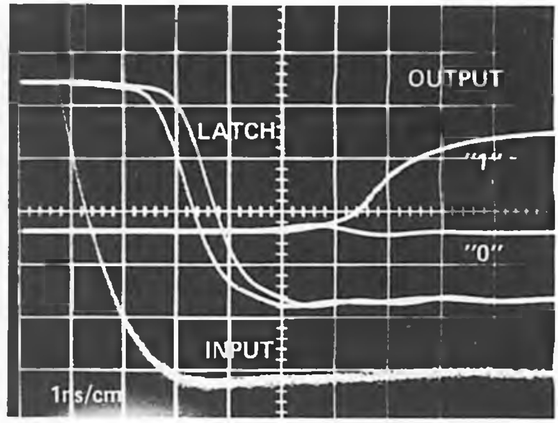


Figure 17. Latch enable time and latch aperature time for 100mV input step, 5mV overdrive (input = 5mV/cm, latch = 200mV/cm, output = 400mV/cm)

The performance of the latch function is illustrated by Figure 17. The input signal is the standard 100mV step with 5mV overdrive and is in the direction to cause the output to switch from a logical "0" to a logical "1". The delay of the latch signal relative to the input is adjusted until the output just switches to a "1"; this is the latch enable time and under these conditions is 1.8 ns. The difference between the latch timing for which the output just barely switches and when it does not switch is the latch aperture time; this is about 500ps for 5mV overdrive. The performance of the latch with input overdrive and temperature generally follows that of the propagation delays (Figure 14 and 16).

The overall performance of the Am685 is summarized in Table II. It is apparent from the table and the previous discussion that the device is ideally suited for applications where both precision and high speed are required, such as in analog-to-digital converters, data acquisition systems, and optical isolators. The device is the first in a family of new wideband linear integrated circuits designed to meet the requirements of very high-speed systems.

Propagation Delay	
(100mV step, 5mV overdrive)	6.5 ns MAX
Input Offset Voltage	2.0mV MAX
Average Temperature Coefficient	
Of Input Offset Voltage	10μV/°C MAX
Input Offset Current	1.0μA MAX
Input Bias Current	10μA MAX
Common Mode Voltage Range	±3.3V MIN
Common Mode Rejection Ratio	80dB MIN
Supply Voltage Rejection Ratio	70dB MIN
Positive Supply Current	22 mA MAX
Negative Supply Current	26 mA MAX

Table II: Performance Characteristics of the Am685 Comparator (T_A = 25°C, V^+ = 6.0V, V^- = −5.2V, R_L = 50Ω to −2.0V)

THE A-D APPLICATION

Very fast, precision, analog-to-digital conversion stands to benefit considerably from the availability of a fast comparator. As the block diagram of a fast 10-bit converter in Fig. 18 shows, a typical rapid conversion technique may resemble the use of feedforward compensation in an operational amplifier.

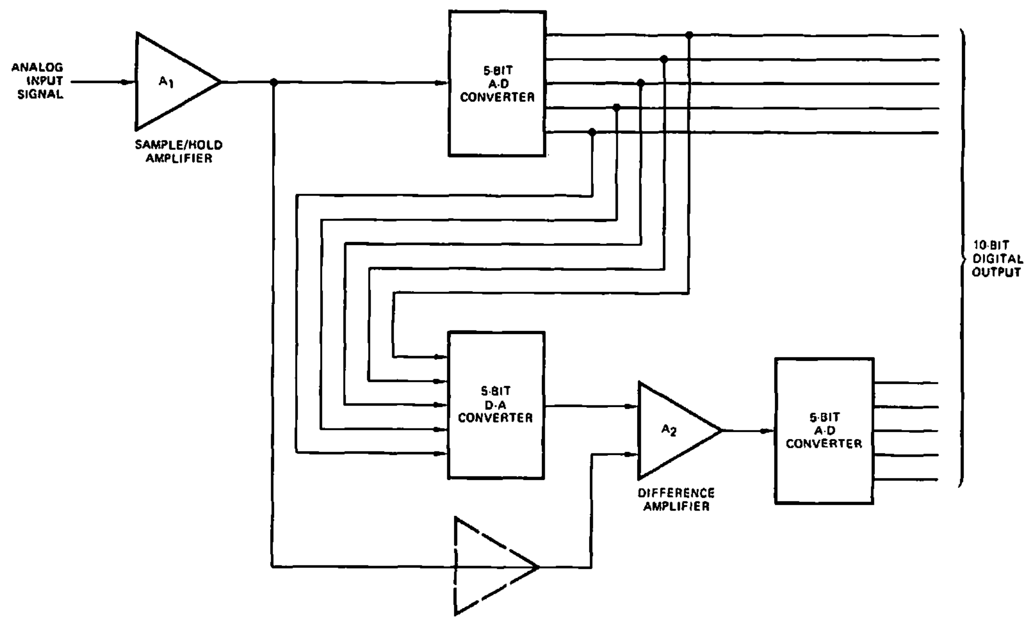
The analog input signal is sampled at the beginning of a conversion period and fed to a fast five-bit a-d converter, which provides the first five most significant bits of the output. These five bits also drive a companion d-a converter, which must be accurate to better than 10 bits. The output of the d-a converter is a replica of the input signal, quantized to five bits. This is compared with the actual input signal stored in the sample-and-hold amplifier. The difference between the two analog levels is the remaining part of the input signal that must be quantized. This difference is amplified and applied to another five-bit a-d converter to provide the five least-significant bits of the final output.

Typical five-bit a-d converters may consist of 31 106-type comparators connected to the signal source and referenced to the full-scale input in steps of 1/32. The output of each comparator goes into a latch, and the latch outputs are decoded by three stages of TTL gages to develop the five-bit digital output.

Typical propagation delays are 40 ns for the comparators, 22 ns for the latches, and 10 ns for the decoding, resulting in a total delay of 80 ns. Average settling time for the five-bit d-a converter and the difference amplifier together comes to about 200 ns, and the settling time for the input sample-and-hold amplifier is 70 ns. Thus, the over-all conversion time for this 10-bit converter amounts to 430 ns.

Substitution of the high-speed ECL comparator for the 106 type in each of the five-bit converters leads to a significant improvement in propagation delay. The typical delay of the comparator is about 6.5 ns, and no external latch is required. With ECL it is possible to wire-OR outputs, so only one level of decoding gates is required. Allowing 1.5 ns for the gates, the total five-bit conversion time is only 8 ns — a tenfold improvement over the existing circuit.

If the latch function of the comparators is used as the sample-and-hold for the first five-bit converter, the sample-and-hold can be put in parallel with the first quantization step, as shown by the dotted lines in Fig. 18. This eliminates its settling time from the over-all delay of the system. With the new comparator, the total 10-bit conversion time drops to 216 ns, with over 90% of the delay attributable to the d-a converter and the difference amplifier. Moreover, the availability of an 8 ns five-bit converter should provide the impetus to improve the slower sections of the system. A 10-bit a-d converter with a delay under 100 ns is not an extravagant prediction.



If the standard 106-type comparator in this a-d converter is replaced by the 10 ns device, a tenfold improvement in speed is possible. What is more, the ECL makes possible both wired-OR outputs and a single level of decoding for gates.

LIC-165

Figure 18. Analog to digital.

Am685/Am686/Am687 DESIGNING WITH HIGH SPEED COMPARATORS

By Leonard Brown

INTRODUCTION

The Am685, Am686 and Am687 are a family of high-speed sampling comparators capable of detecting low-level signals of the order of 5-10mV in 12-15ns over the temperature range $-55°C \leqslant T_A \leqslant 125°C$. The Am686 is fully TTL-compatible and complementary outputs are available generated from a true differential output stage assuring a maximum output skew of under 2ns at 25°C. The Am685 and Am687 are single and dual ECL-compatible versions, respectively, and have output skews of less than 1ns. A high-speed latch is incorporated in the input stage permitting input signals to be acquired in 4.0ns maximum for the ECL versions and 6.0ns for the TTL device.

Applications of the devices are not limited to high-speed designs as the combination of the excellent DC input characteristics, availability of true differential outputs and the latch function permit unique solutions for slower speed applications where the response time of the comparators can be considered negligible.

THE SAMPLING COMPARATOR

The sampling comparator may be visualized as a conventional voltage comparator with the provision that the outputs may be latched into the logic states determined by the input signal conditions existing at the time of application of the latch signal. This is achieved by incorporating the latch circuitry in the input stage of the device. The minimum latch enable pulse width is necessarily less than the propagation delay of the device and, therefore, the comparator can be unlatched for a fraction of its propagation delay (4.0ns for the Am685). The outputs will then change in accordance with the input conditions existing at the time of the latch signal. Note: It is impossible for the comparator to oscillate under these conditions.

If the latch function is not used, the device operates as a conventional voltage comparator.

BACK TO BASICS

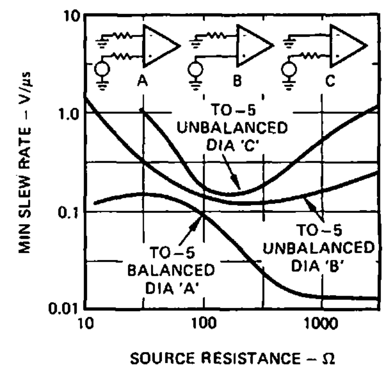
Comparators are designed to have both high gain and large bandwidth. This creates instability problems or oscillations when the device outputs are in the transition region. The tendency of a device to oscillate is a function of the layout, (poor layout increasing the amount of feedback caused by parasitic capacitance) and the source impedance of the circuit employed (The higher the source impedance the less parasitic coupling is necessary to cause oscillation.) It is mandatory with comparators of the gain and bandwidth of the Am685, Am686 and Am687 to ensure that power supplies are well decoupled, lead lengths are kept as short as possible, and wherever possible (especially in the case of the Am686), a ground plane should be employed.

In addition to reducing the effects of stray capacitance, a ground plane substantially reduces the possibility of the output current spike coupling back to the inputs through the ground lead when the TTL output stages switch.

The minimum slew rate at which the input signal must cross the threshold region to prevent oscillation, regardless of the particular layout parasitics, may be determined by applying a DC voltage to the input until the circuit just commences to oscillate and increasing this voltage until the oscillation ceases. The minimum necessary input slew rate is then given by $\Delta V/t_{pd}$ MIN, where ΔV is the input voltage required to prevent oscillation and t_{pd} MIN is the minimum propagation delay of the comparator.

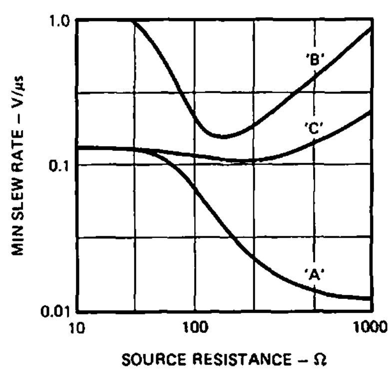
The minimum slew rate will be found to be a function of source impedance and source impedance mismatch.

The curves of Figures 1 and 2 show the minimum slew rate for the Am686 as a function of source impedance and source impedance mismatch.



LIC-166

Figure 1. Minimum Slew Rate Versus Source Resistance (TO–5).



LIC-167

Figure 2. Minimum Slew Rate Versus Source Resistance (DIP).

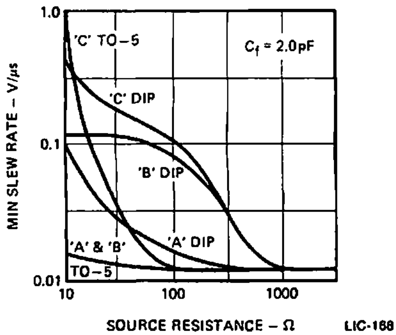


Figure 3. Minimum Slew Rate Versus Source Resistance (TO−5 & DIP).

It can be seen that unbalanced sources dramatically effect the minimum input slew rate required. Note that for optimum performance, the source impedance seen by the comparator should be both DC and AC balanced to reduce the differential feedback to a minimum.

The effect of an AC unbalanced source is seen especially on the Am686 as when the output switches, the output current spike is coupled back to the input. This can be eliminated by forcing the AC unbalance to result in positive feedback, which may be achieved by decoupling the inverting input or applying positive feedback via a 2-4pF capacitor from the Q output to the non-inverting input.

The curves of Figure 3 illustrate the improvement in minimum slew rate when a small amount of positive feedback is employed by virtue of a 2pF feedback capacitor.

OPTIMUM SOURCE CONDITIONS (C_f = 0pF)

With low source impedances (< 50Ω), the majority of the feedback between the output and the input occurs internal to the device. As the source impedance is raised, external feedback increases through the parasitic feedback capacitance until, at high source impedances, the external feedback dominates. This explains the anomolous characteristics of the minimum slew rate curves and suggests that the optimum source resistance for the device is between 300 and 500Ω for unbalanced sources and is approximately 1000Ω for a balanced source.

OPTIMUM SOURCE CONDITIONS (C_f = 2pF)

With a source impedance of 100Ω, the minimum slew rate is 0.15V/µs for the DIP configuration and 0.02V/µs for the TO-5. For balanced sources the minimum slew rate is 0.03V/µs for $R_S \geq 100\Omega$ and for a source impedance between 1kΩ and 3kΩ, the minimum slew rate is <0.02V/µs regardless of impedance, DC imbalance or package type.

The use of the feedback capacitor is recommended when:

1. The input slew rate is within a factor of 2 greater than the minimum theoretical slew rate.
2. System constraints do not permit optimisation of layout and lead lengths.
3. Unbalanced source impedances are used (it is not always possible to provide input conditions which are both DC and AC balanced).

A FAMILY AFFAIR

It must be stressed that the concepts discussed concerning source imbalance and minimum input slew rate apply to all devices in the family. The Am686 was highlighted as it is more sensitive to layout constraints and parasitic feedback because of its significantly higher voltage gain.

Similarly all of the applications which follow may be implemented with any device in the series provided due caution is exercised with regard to the different output logic levels.

THE RELAXATION OSCILLATOR

The principal problems in the design of a classical relaxation oscillator are:

1. The variation in potential to which the energy storage device (normally a capacitor) is charged.
2. The variation in the threshold level at which the capacitor is to be discharged.
3. The variation inherent in the sensor element (normally a comparator) in detecting equivalence between the threshold level and the capacitor's instantaneous potential.

The variations are all functions of both time and temperature and are the primary causes of frequency drift, symmetry error, and jitter.

By taking advantage of two unique properties of the Am686, a relaxation oscillator may be designed to eliminate the first two problems and reduce the third to a second-order effect for oscillation frequencies from 1MHz to 30MHz.

The true differential output stage of the comparator ensures that the Q and $\overline{Q}$ outputs change within 1-2ns of each other. This feature ensures that the outputs can never be in the same logic state instantaneously, either HIGH or LOW, and that the only time they are equal in voltage is when traversing the logic uncertainty levels. This property permits the design of a threshold setting circuit that varies in accordance with the charging voltage applied to the timing capacitor. Therefore, any change in charging potential is automatically compensated by a corresponding change in threshold level.

Second, the combination of the short propagation delay 7-10ns, the minimum difference in propagation delay between outputs and the stability of these delays with temperature assures square wave symmetry of better than 1% @ 1MHz and 5% @ 25MHz and a frequency stability of 1% @ 10MHz and 4% @ 25MHz.

The above statements are true from device to device and over the operating temperature range of −55°C to +125°C. Over the industrial temperature range, a factor of two improvement should be obtained.

CIRCUIT THEORY (Fig. 4)

Assuming the circuit is in an oscillating mode, the voltage appearing at the non-inverting terminal will alternate between V_X and V_Y where:

$$V_X = \frac{R_1}{(R_1 + R_2)}(V_{OH} - V_{OL}) + V_{OL} \quad \text{and}$$

$$V_Y = \frac{R_2}{(R_1 + R_2)}(V_{OH} - V_{OL}) + V_{OL}$$

When $V_{+IN} = V_X$, the timing capacitor C will be charging towards V_{OH}, and when $V_{+IN} = V_Y$, the timing capacitor will be discharging towards V_{OL}.

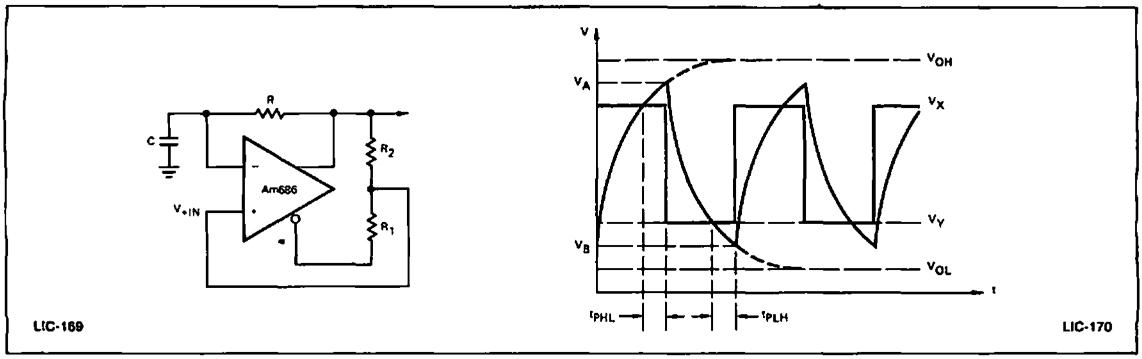


Figure 4. Circuit Design.

After the voltage on the capacitor equals the voltage on the non-inverting input, a finite time will elapse before the output of the circuit changes, during which time (the propagation delay of the Am686) the capacitor will continue to charge towards V_{OH}, or discharge towards V_{OL}.

Therefore, the capacitor will charge to a voltage

$$V_A = V_{OH} - e^{-t_{PHL}/CR} \cdot (V_{OH} - V_X)$$

and discharge to a voltage

$$V_B = V_{OL} + e^{-t_{PLH}/CR} \cdot (V_Y - V_{OL})$$

where t_{PHL} and t_{PLH} = propagation delay of the Am686 from the inputs to the output changing from HIGH – LOW and LOW – HIGH respectively.

The time to charge from V_B to V_A which is the positive half cycle is given by:

$$t^+ = CR\ 1n\ \frac{V_{OH} - V_B}{V_{OH} - V_A}$$

substituting for V_A and V_B

$$t^+ = CR\ 1n\left[\left(\frac{R_1}{R_2} + 1\right) e^{t_{PHL}/CR} - 1\right]$$

Similarily the negative half cycle is given by:

$$t^- = CR\ 1n\ \frac{V_A - V_{OL}}{V_B - V_{OL}}$$

$$t^- = CR\ 1n\left[\left(\frac{R_1}{R_2} + 1\right) e^{t_{PLH}/CR} - 1\right]$$

Note: The only assumptions are:

1. $(V_{OH} - V_{OL})$ of the Q output = $(V_{OH} - V_{OL})$ of the $\overline{Q}$ output.
2. Offset voltage and offset current errors are negligible.
3. $e^{t_{PLH}/CR} \times e^{-t_{PHL}/CR} = 1$

The only factor affecting pulse width variation is, therefore, t_{PHL} and t_{PLH}. As $t_{PHL} > t_{PLH}$ by 1-2ns, it is therefore anticipated that t^+ will be marginally greater than t^-.

MINIMUM OPERATING FREQUENCY

For the Am686, it is specified that the minimum slew rate at the input to insure that the device will not oscillate in the transition region is 1V/μs. This will determine the minimum operating frequency of the circuit.

The rate of change of voltage on the timing node is given by:

$$\rho = \frac{\partial v}{\partial t} = \frac{Vo}{CR} \times e^{-t/CR}$$

In the circuit,

a) $Vo = V_{OH} - V_B$ (assuming positive ramp)

and

b) $t = CR\ 1n\ \left[\left(\frac{R_1}{R_2} + 1\right) e^{t_{PHL}/CR} - 1\right]$

As the slew rate is only critical in determining the lowest operating frequency, it may be assumed that $e^{t_{PHL}/CR} = 1$ ($CR >>> t_{PHL}$); therefore, $Vo = V_{OH} - V_B \approx V_{OH} - V_Y$

$$Vo = (V_{OH} - V_{OL})\ \frac{R_1}{R_1 + R_2} \qquad \text{and, } t = CR\ 1n\ \frac{R_1}{R_2}$$

$$\therefore \rho = \frac{\partial v}{\partial t} = \frac{(V_{OH} - V_{OL})}{CR} \times \frac{R_1}{R_1 + R_2} \times \frac{R_2}{R_1}$$

$$= \frac{\Delta V}{CR} \times \frac{R_2}{R_1 + R_2}$$

where, $\Delta V = (V_{OH} - V_{OL})$

The minimum operating frequency

$$f_{MIN} = \frac{1}{2\,CR\ 1n\ \frac{R_1}{R_2}}$$

substituting

$$CR = \frac{\Delta V}{\rho}\ \frac{R_2}{R_1 + R_2} \qquad f_{MIN} = \frac{\rho}{2\Delta V} \times \frac{(R_1/R_2 + 1)}{1n\ R_1/R_2}$$

The expression for minimum frequency indicates that an optimum ratio of R_1/R_2 exists that is independent of any particular RC time constant which may have been chosen.

The ratio may be determined by differentiating f_{MIN} with respect to R_1/R_2.

$$\frac{\partial f_{MIN}}{\partial \frac{R_1}{R_2}} = \frac{\rho}{2\Delta V} \times \frac{1n\frac{R_1}{R_2} - (\frac{R_1}{R_2}+1)/\frac{R_1}{R_2})}{(1n\frac{R_1}{R_2})^2}$$

$$= \frac{\rho}{2\Delta V} \times \frac{1n\frac{R_1}{R_2} - 1 - \frac{R_2}{R_1}}{(1n\frac{R_1}{R_2})^2}$$

Setting $\frac{\partial F}{\partial \frac{R_1}{R_2}} = 0$

$$1n\frac{R_1}{R_2} - 1 - \frac{R_2}{R_1} = 0$$

$$\frac{R_1}{R_2} = \frac{1}{1n\frac{R_1}{R_2} - 1}$$

$$\therefore \frac{R_1}{R_2} = 3.59112$$

Therefore, the lowest frequency the oscillator will perform consistent with the 1V/µs constraint is:

$$f_{MIN} = \frac{1 \times 4.6}{2 \times 3.5\ 1n\,3.6} = .513\text{MHz}$$

D.C. OFFSET ERRORS

The presence of DC errors resulting from the bias and offset currents and offset voltage of the Am686 will cause the V_Y and V_X thresholds to be both shifted either positive or negative by an equal amount δV where δV is the sum of all such errors.

The magnitude of these effects may be calculated as follows:

When the capacitor is discharging –

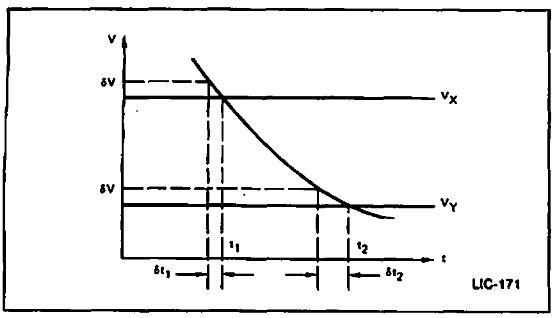


Figure 5.

$$V_{(t)} = V_o e^{-t/CR}$$

$$\frac{dv}{dt} = -\frac{1}{CR} V_o e^{-t/CR} = -\frac{1}{CR} V_{(t)}$$

$$\delta t_1 = -\frac{\delta V}{V_{(t_1)}} CR$$

$$\delta t_2 = \frac{-\delta VCR}{V_{(t_2)}}$$

Δt^- Negative Pulse Width Change =

$$\delta t_2 - \delta t_1 = \delta VCR \frac{V_{(t_2)} - V_{(t_1)}}{V_{(t_1)}\ V_{(t_2)}}$$

As $V_X = V_{t_1}, V_Y = V_{t_2}$

$$\Delta t^- = \frac{\delta VCR\ (V_Y - V_X)}{V_X V_Y}$$

Similarly for the positive pulse

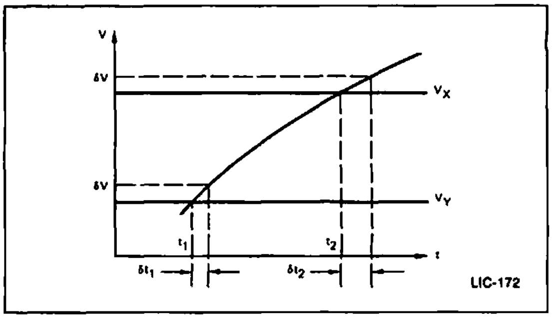


Figure 6.

$$V_{(t)} = Vo\ (1 - e^{-t/CR})$$

Whence, $dv/dt = \frac{1}{CR}(Vo - V_{(t)})$

$$\therefore \delta t_1 = \frac{\delta VCR}{Vo - V_{t_1}}$$

$$\delta t_2 = \frac{\delta VCR}{Vo - V_{t_2}}$$

Positive Pulse Width Change $\Delta t^+ = \delta t_2 - \delta t_1$

$$= \delta VCR\ \frac{1}{Vo - V_{(t_2)}} - \frac{1}{Vo - V_{(t_1)}}$$

In the circuit $V_{t_2} = V_X, V_{t_1} = V_Y, Vo - V_X = V_Y$

$$\Delta t^+ = \delta VCR\left(\frac{1}{V_Y} - \frac{1}{V_X}\right) = \delta VCR\ \frac{V_X - V_Y}{V_X V_Y} = -\Delta t^-$$

∴ Offset errors do not affect the frequency of oscillation, only the symmetry of the waveshape.

SYMMETRY ERROR

$$\text{Symmetry } S = \frac{\Delta t^+ - \Delta t^-}{2T} \times 100\% \text{ where } T = CR \ln \frac{V_Y}{V_X}$$

$$S = \frac{2\Delta t^+}{2T} \times 100\%$$

$$= \frac{\delta VCR\,(V_X - V_Y)}{V_X V_Y} \times \frac{1}{CR \ln V_Y/V_X}$$

Symmetry is worse for maximum value of $V_X - V_Y$. Maximum value of $V_X - V_Y$ occurs when R_1 and R_2 are arranged for minimum operating frequency, i.e., $R_1/R_2 = 3.6$

Substituing $\delta V = 5\text{mV}$

$$V_X/V_Y = 3.6$$

$$V_X V_Y = \frac{1}{4.6} V_{OH} \times \frac{3.6}{4.6} V_{OH}$$

$V_{OH} = 3.5\text{V}$ and neglecting V_{OL}

Symmetry is $< 0.38\%$

Note: 1. For any given ratio of $R_1 : R_2$ (i.e., V_X and V_Y), offset voltage Symmetry error is independent of frequency.

2. Symmetry improves to .33% @ $R_1 : R_2 = 2.5$

EXTENDING LOW FREQUENCY PERFORMANCE

If it is necessary to extend the lower limit of the oscillation frequency, a small amount of positive feedback may be introduced by connecting a 2-4pF capacitor between the Q output and the non-inverting input. This will decrease the minimum input slew rate required and enable oscillation frequencies of 1kHz to be achieved without spurious oscillations occuring on the rising or falling edges of the waveform. At frequencies below 1MHz, it is not necessary to take into account any potential frequency shift this additional feedback introduces. (Above 1MHz, it is not necessary to use this additional feedback.)

PERFORMANCE CHARACTERISTICS:

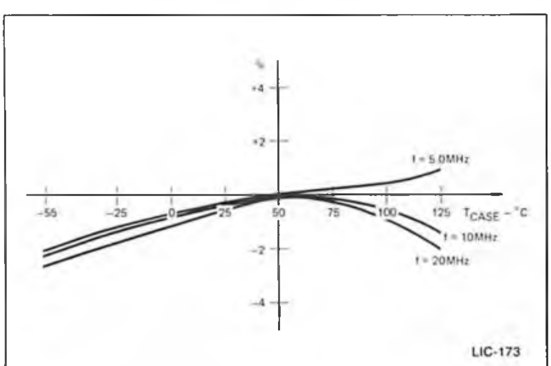


Figure 7. Percentage Change in Frequency Versus Case Temperature.

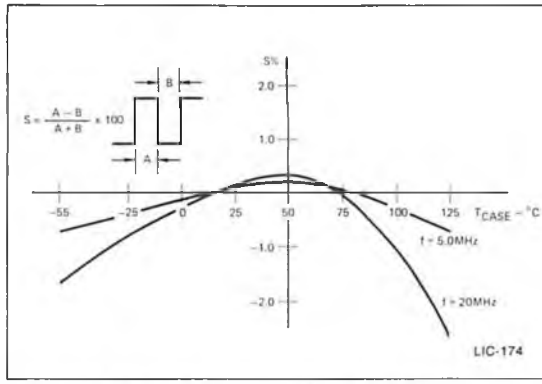


Figure 8. Change in Symmetry Versus Case Temperature.

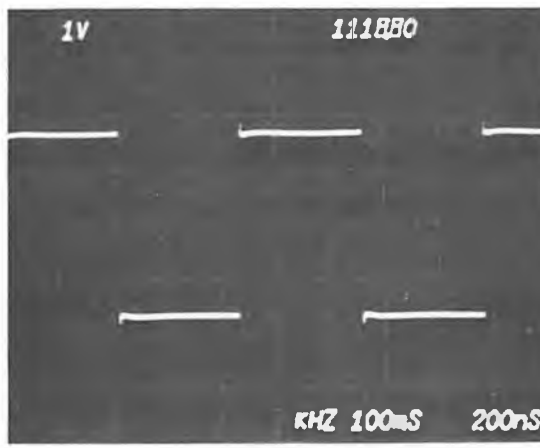


Figure 9. Output Waveform at 1.0MHz.

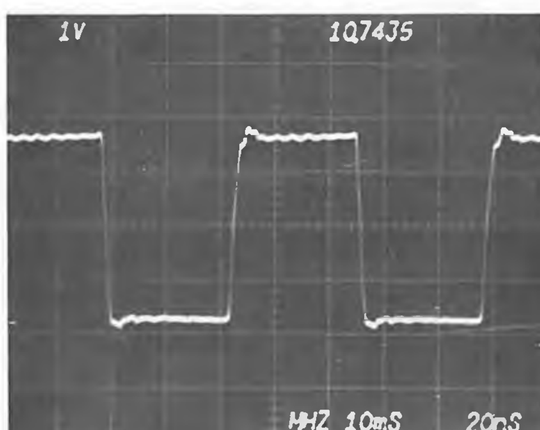


Figure 10. Output Waveform at 10MHz.

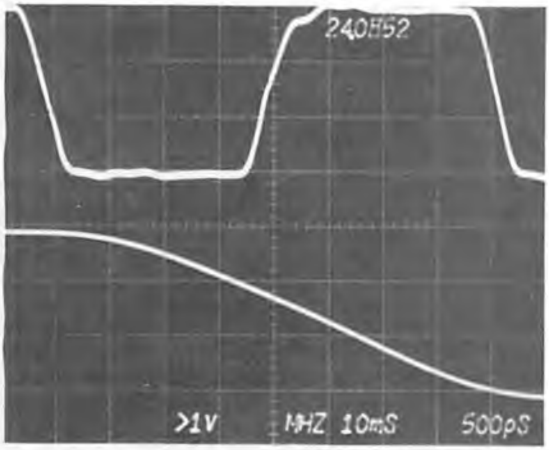


Figure 11. Output Waveform at 24MHz and Expanded Falling Edge Exhibiting <50ps Jitter.

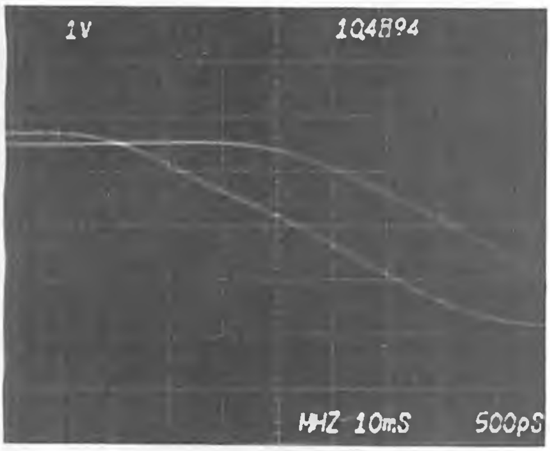


Figure 12. Change in Pulse Width and Jitter from 25°C to 125°C, f = 10MHz.

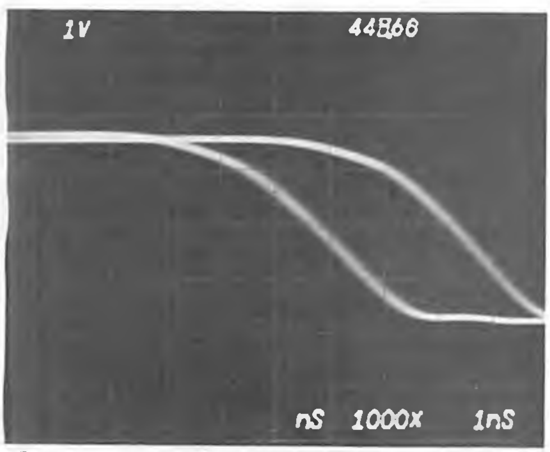


Figure 13. Expanded Fall Time Showing Change in Pulse Width from 25°C to 125°C, f = 1.0MHz, (Jitter ~ 300ps).

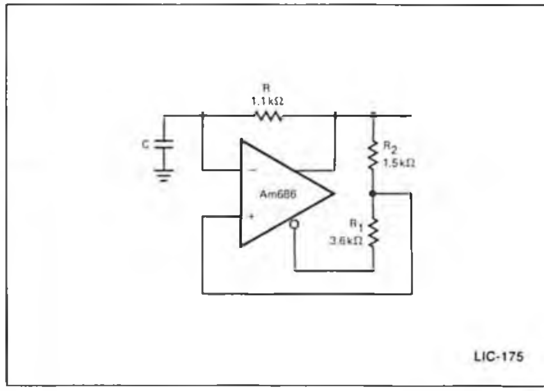


Figure 14. Circuit and Component Values used in Obtaining Performance Characteristics.

LOW LEVEL PULSE DETECTOR

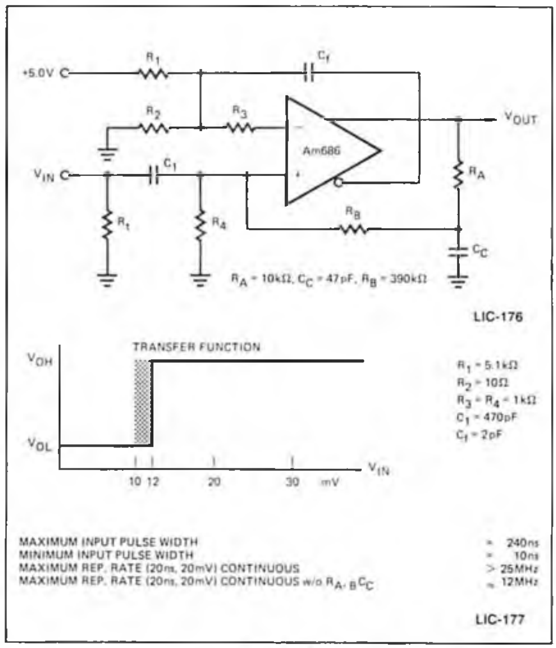


Figure 15.

CIRCUIT OPERATION

The input resistance is essentially determined by R_4 which was chosen to be 1kΩ on the basis that most sources would not be unduly loaded at this value and consequentially higher values would make the circuit excessively prone to oscillation. To minimize bias current errors, the inverting input is connected to the 10mV reference source (R_1 and R_2) through an equal-valued resistor (R_3).

Positive feedback is provided by C_f which provides a 50-60mV, 3-4ns pulse, significantly improving the switching time and narrowing the uncertainty region for pulses just in excess of the 10mV threshold.

Capacitor C_1 provides A-C coupling and thus isolates the circuit from slowly varying signals which may be superimposed on the signal to be detected. Such is the case for a detector sensing the output from a fibreoptic cable receiver. The A-C coupling imposes additional constraints; namely, the repetition rate and duty cycle of the input signal.

The signal which is seen by the non-inverting terminal and then compared to the reference is not simply the peak value of the input pulse but the peak value less the average D.C. value of the input signal.

Assuming a 20mV input pulse, 20ns wide and repeated every 20ns, the signal seen across R_4 will be as follows:

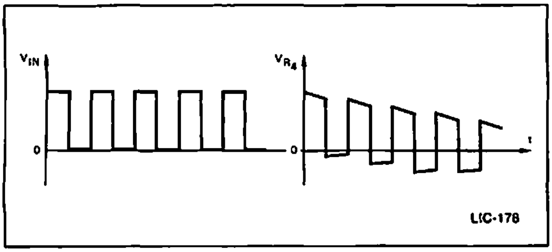


Figure 16.

By the ninth pulse, the peak signal will be 15.2mV dropping to 14.6mV by the end of the pulse; thus, after a pulse train of ~10 pulses, the detector will not detect the incoming signal.

Additionally, consider the case of a 20ns pulse repeated every 60 nanoseconds.

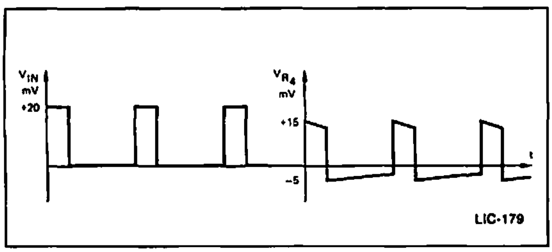


Figure 17.

The peak signal at the input will now be only 15mV; therefore, the maximum repetition rate consistent with providing a 5.0mV overdrive is 1/80ns or 12.5MHz.

Therefore, the circuit will only successfully detect 20mV, 20ns signals if: a) the pulse train is ⩽ 10 pulses or b) the repetition rate ⩽ 12MHz.

To compensate for these problems, a DC feedback signal is generated by R_A, R_B and C_C, which adjusts the reference level accordingly.

R_A and C_C form a low-pass filter that gives a maximum DC level of 1.7 volts at a 1:1 duty cycle. At this duty cycle, it is required to reduce the reference level by 5mV to maintain adequate overdrive. R_B and R_4 form an attenuator and the DC voltage level returned to the non-inverting input = 1.7V x $R_4/(R_4 + R_B)$ = 4.3mV. Using this network permits the circuit to work up to 25MHz, or better than a 1 : 1 duty cycle and removes the limitation imposed by the input A-C coupling.

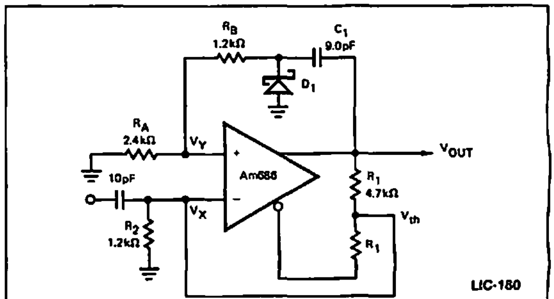
Note: The response time of the feedback path must be the same as the input network; i.e., $R_AC_C = R_4C_1$ in order for the feedback to follow rapid changes in repetition rate or duty cycle.

PRECISION MONOSTABLE

Commercially available one-shots encounter problems in the generation of narrow (< 100ns) pulses. Namely, there is a significant delay between the input pulse and the output pulse of the order of 20ns and the resultant output pulse width is highly temperature dependent due to the variation in internal delays with temperature. Second, the input pulse must be of the logic level for the type of logic employed in the design – TTL, DTL, RTL, etc. Thus, the circuits are incapable of responding to low-level input signals in the millivolt range.

The Am685 series of sampling comparators can be employed in the design of a custom one-shot to overcome both of these problems.

Figure 18 shows the design of a monostable employing the Am686 to generate precision output pulses in the 20-100ns range and the values shown are for a 50ns pulse width.



$$t_{pw} = C(R_A+R_B)\ \ln\left[\left(\frac{1-V_{OL}/V_{OH}}{1+V_{OL}/V_{OH}}\right)\left(\frac{R_A}{R_A+R_B}\right)\left(2+\frac{R_2}{R_1}\right)e^{+t_{pd}/C(R_A+R_B)}\right]$$

Figure 18.

The timing diagram illustrates the circuit operation.

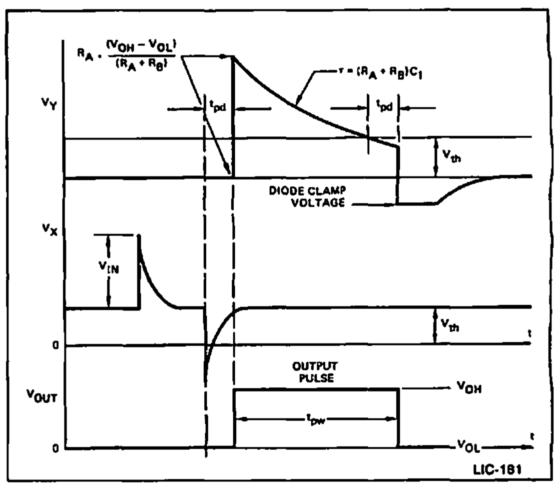


Figure 19.

The circuit triggers on the negative-going edge of the input pulse and the Q output switches high. The output signal is attenuated by R_A and R_B to keep the coupled pulse inside the common mode limits of the device. The output remains high until the voltage on the non-inverting input reaches the threshold set by R_1 and R_2. In order that the pulse width be independent of the input pulse amplitude, it is important to make the input time constant small compared to the desired output pulse width.

A unique feature of the circuit is the use of the differential outputs of the device to set the threshold, V_{th} thus providing temperature compensation and a reduction in pulse width variation from device to device.

Diode D_1 shortens the recovery time of the timing capacitor *and permits* retriggering 30ns after the end of the pulse with less than a 5% change in pulse width.

Complete isolation of the input signal and the timing network may be achieved by employing the latch function as shown *below:*

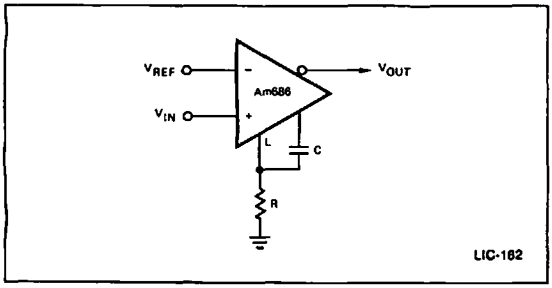


Figure 20.

When the input signal exceed V_{REF}, the output will switch and latch the comparator in the high state. When timing capacitor charges to the latch threshold, the latch will become disabled and the output will switch back to zero, providing the input is now below V_{REF}.

The advantages of this approach are:

1. No interaction between input signal and timing capacitor.
2. The input threshold set by V_{REF} is independent of the timing threshold.

Thus, the input threshold can be varied from millivolts to volts. A practical circuit is shown:

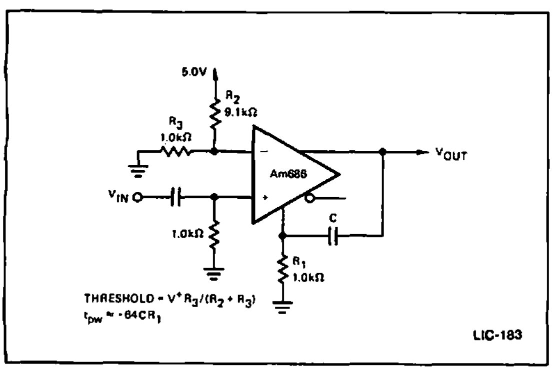


Figure 21.

The circuit is applicable for situations where accuracy of trigger threshold is important, a large variation in input signal level is expected or the input signal level is low. Timing accuracy (pulse width) is independent of the amplitude of the input pulse, but the output pulse width varies with temperature in accordance with the temperature dependence of the latch threshold (~ 3.0mV/°C for Am686).

APPLICATIONS REQUIRING INPUT HYSTERESIS

Comparators are frequently employed in systems where it is required that the transfer function contain a defined amount of hysteresis. Conventional comparators employing positive feedback can be used to generate hysteresis as shown below:

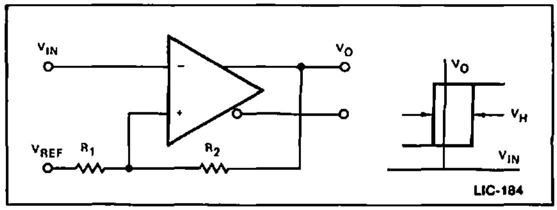


Figure 22.

Drawbacks of this technique include:

1. Response time of hysteresis loop ⩾ comparator propagation delay
2. Hysteresis varies with V_{OH} and VOL changes
3. Hysteresis is not centered about zero unless an additional reference is used.

By utilizing the latch function on the Am685, Am686 and Am687, hysteresis can be inserted in a manner to overcome these drawbacks; namely:

1. Response time of hysteresis loop << propagation delay
2. Hysteresis not affected by V_{OH} and V_{OL} changes
3. Hysteresis is symmetrical about zero.
4. Full input differential capability maintained over complete common mode range.

The hysteresis is obtained by applying a slight bias to the latch inputs. The technique is illustrated in the test circuit shown for the Am687.

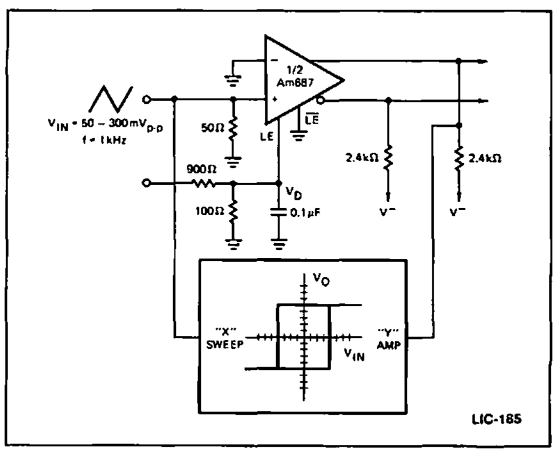


Figure 23.

The hysteresis is essentially symmetrical about zero and between ±5 and ±50mV of hysteresis can be generated before the relationship between the latch voltage and the thresholds become too sensitive.

The hysteresis is independent of changes in the positive supply voltage and the input common mode range and varies only with changes in temperature and negative supply voltage.

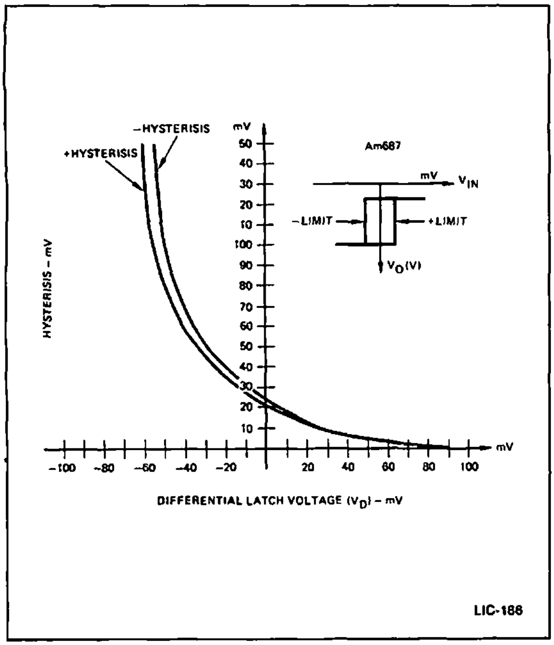


Figure 24. Input Hysteresis Versus Latch Voltage, T_A = 25°C.

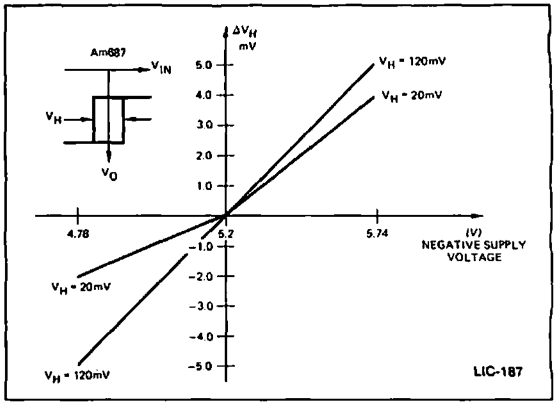


Figure 25. Change in Hysteresis Versus Change in Negative Supply Voltage.

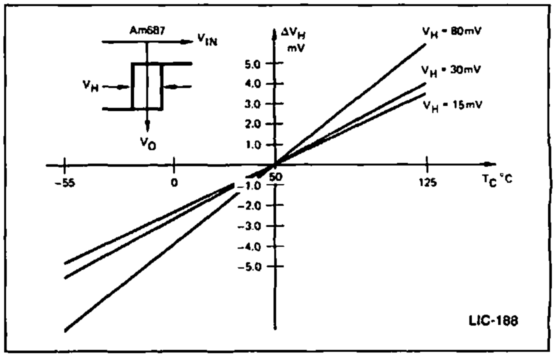
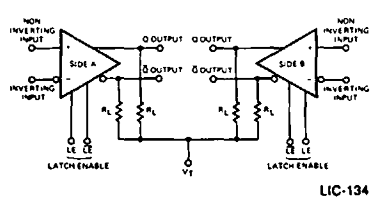


Figure 26. Change in Hysteresis Versus Case Temperature.

COMPARATOR PERFORMANCE SPECIFICATIONS

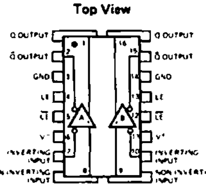
Am687

FUNCTIONAL DIAGRAM



The outputs are open emitters; therefore external pull-down resistors are required. These resistors may be in the range of 50-200Ω connected to −2.0V, or 200-2000Ω connected to −5.2V.

CONNECTION DIAGRAM
Top View



Note 1. Pin 6 is connected to bottom of case.

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

DC Characteristics

Symbol	Parameter	Conditions (Note 3)	Am687A-L / Am687-L Min.	Am687A-L / Am687-L Max.	Am687A-M / Am687-M Min.	Am687A-M / Am687-M Max.	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\Omega$, T_A = 25°C	−3.0	+3.0	−2.0	+2.0	mV
		$R_S \leq 100\Omega$	−3.5	+3.5	−3.0	+3.0	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\Omega$	−10	+10	−10	+10	µV/°C
I_{OS}	Input Offset Current	25°C ≤ T_A ≤ $T_{A(max.)}$	−1.0	+1.0	−1.0	+1.0	µA
		$T_A = T_{A(min.)}$	−1.3	+1.3	−1.6	+1.6	µA
I_B	Input Bias Current	25°C ≤ T_A ≤ $T_{A(max.)}$		10		10	µA
		$T_A = T_{A(min.)}$		13		16	µA
V_{CM}	Input Voltage Range		−3.3	+2.7	−3.3	+2.7	V
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\Omega$, $-3.3 \leq V_{CM} \leq +2.7$ V	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\Omega$, ΔV_S = ±5%	70		70		dB
V_{OH}	Output HIGH Voltage	T_A = 25°C	−0.960	−0.810	−0.960	−0.810	V
		$T_A = T_{A(min.)}$	−1.060	−0.890	−1.100	−0.920	V
		$T_A = T_{A(max.)}$	−0.890	−0.700	−0.850	−0.620	V
V_{OL}	Output LOW Voltage	T_A = 25°C	−1.850	−1.650	−1.850	−1.650	V
		$T_A = T_{A(min.)}$	−1.890	−1.675	−1.910	−1.690	V
		$T_A = T_{A(max.)}$	−1.825	−1.625	−1.810	−1.575	V
I^+	Positive Supply Current			35		32	mA
I^-	Negative Supply Current			48		44	mA
P_{DISS}	Power Dissipation			485		450	mW

Switching Characteristics (V_{in} = 100mV, V_{od} = 5 mV)

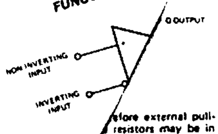
Symbol	Parameter	Conditions	Am687A-L / Am687-L Min.	Am687A-L / Am687-L Max.	Am687A-M / Am687-M Min.	Am687A-M / Am687-M Max.	Units
t_{pd+}, t_{pd-}	Propagation Delay, Am687A	$T_{A(min.)} \leq T_A \leq$ 25°C		8.0		8.0	ns
		$T_A = T_{A(max.)}$		10		12.5	ns
t_{pd+}, t_{pd-}	Propagation Delay, Am687	$T_{A(min.)} \leq T_A \leq$ 25°C		10		10	ns
		$T_A = T_{A(max.)}$		14		20	ns
t_s	Minimum Latch Set-up Time	T_A = 25°C		4.0		4.0	ns

Notes: 2. Derate at 9mW/°C for operation at ambient temperatures above +115°C.
3. Unless otherwise specified V^+ = +5.0V, V^- = −5.2V, V_T = −2.0V, and R_L = 50Ω, all switching characteristics are for a 100mV input step with 5mV overdrive. The specifications given for V_{os}, I_{os}, I_B, CMRR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltages. The Am687 and Am687A are designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

COMPARATOR PERFORMANCE SPECIF..TIONS (Cont.)

Am685

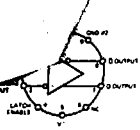
FUNCTIONAL DIAG...



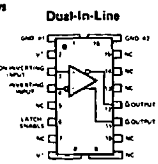
...fore external pull-
...resistors may be in
...to −2.0 V, or 200−

LIC-118

...ECTION DIAGRAMS
Top Views



Dual-In-Line



Note 1: On metal package, pin 5 is connected to case.
On DIP, pin 8 is connected to case.

LIC-120 LIC-121

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

DC Characteristics

Symbol	Parameter (see definitions)	Conditions (Note 3)	Am685-L Min.	Am685-L Max.	Am685-M Min.	Am685-M Max.	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25°C$	−2.0	+2.0	−2.0	+2.0	mV
		$R_S \leq 100\Omega$	−2.5	+2.5	−3.0	+3.0	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\Omega$	−10	+10	−10	+10	µV/°C
I_{OS}	Input Offset Current	$T_A = 25°C$	−1.0	+1.0	−1.0	+1.0	µA
			−1.3	+1.3	−1.6	+1.6	µA
I_B	Input Bias Current	$T_A = 25°C$		10		10	µA
				13		16	µA
R_{IN}	Input Resistance	$T_A = 25°C$	6.0		6.0		kΩ
C_{IN}	Input Capacitance	$T_A = 25°C$		3.0		3.0	pF
V_{CM}	Input Voltage Range		−3.3	+3.3	−3.3	+3.3	V
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\Omega$, $-3.3 \leq V_{CM} \leq +3.3V$	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output HIGH Voltage	$T_A = 25°C$	−0.960	−0.810	−0.960	−0.810	V
		$T_A = T_{A(min.)}$	−1.060	−0.890	−1.100	−0.920	V
		$T_A = T_{A(max.)}$	−0.890	−0.700	−0.850	−0.620	V
V_{OL}	Output LOW Voltage	$T_A = 25°C$	−1.850	−1.650	−1.850	−1.650	V
		$T_A = T_{A(min.)}$	−1.890	−1.675	−1.910	−1.690	V
		$T_A = T_{A(max.)}$	−1.825	−1.625	−1.810	−1.575	V
I^+	Positive Supply Current			22		22	mA
I^-	Negative Supply Current			26		26	mA
P_{DISS}	Power Dissipation			300		300	mW

Switching Characteristics (V_{in} = 100mV, V_{od} = 5mV)

t_{pd+}	Input to Output HIGH	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	6.5	12	ns
t_{pd-}	Input to Output LOW	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	6.5	12	ns
$t_{pd+}(E)$	Latch Enable to Output HIGH (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	6.5	12	ns
$t_{pd-}(E)$	Latch Enable to Output LOW (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	6.5	12	ns
t_s	Minimum Set-up Time (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$		3.0		3.0	ns
		$T_A = T_{A(max.)}$		4.0		6.0	ns
t_h	Minimum Hold Time (Note 4)	$T_{A(min)} \leq T_A \leq T_{A(max.)}$		1.0		1.0	ns
$t_{pw}(E)$	Minimum Latch Enable Pulse Width (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$		3.0		3.0	ns
		$T_A = T_{A(max.)}$		4.0		6.0	ns

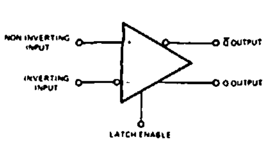
NOTES: 2: For the metal can package, derate at 6.8 mW/°C for operation at ambient temperatures above +100°C; for the dual in-line package, derate at 9 mW/°C for operation at ambient temperatures above +105°C.

3: Unless otherwise specified V^+ = 6.0V, V^- = −5.2V, V_T = −2.0V, and R_L = 50Ω; all switching characteristics are for a 100 mV input step with 5 mV overdrive. The specifications given for V_{OS}, I_{OS}, I_B, CMRR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltages. The Am685 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

4: Owing to the difficult and critical nature of switching measurements involving the latch, these parameters can not be tested in production. Engineering data indicates that at least 95% of the units will meet the specifications given.

Am686

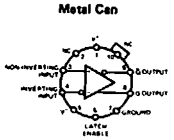
FUNCTIONAL DIAGRAM



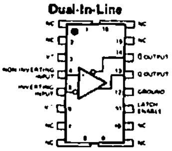
LIC-189

CONNECTION DIAGRAMS
Top Views

Metal Can



Dual-In-Line



Note 1: On metal package, pin 5 is connected to case.
On DIP, pin 6 is connected to case.

LIC-131 LIC-132

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

Symbol	Parameter	Conditions (Note 3)	Am686-C	Am686-M	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25°C$	3.0	2.0	mV MAX.
		$R_S \leq 100\Omega$	3.5	3.0	mV MAX.
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\Omega$	10	10	µV/°C MAX.
I_{OS}	Input Offset Current	$25°C \leq T_A \leq T_A$ (max.)	1.0	1.0	µA MAX.
		$T_A = T_A$ (min.)	1.3	1.6	µA MAX.
I_B	Input Bias Current	$25°C \leq T_A \leq T_A$ (max.)	10	10	µA MAX.
		$T_A = T_A$ (min.)	13	16	µA MAX.
V_{CM}	Input Voltage Range		+2.7, −3.3	+2.7, −3.3	V MIN.
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\Omega$, $-3.3V \leq V_{CM} \leq +2.7V$	60	[illegible]	dB MIN.
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\Omega$	70	70	dB MIN.
V_{OH}	Output HIGH voltage	$I_L = -10mA$, $V_S = V_S$ (min.)	2.7	2.5	V MIN.
V_{OL}	Output LOW Voltage	$I_L = 10mA$, $V_S = V_S$ (max.)	0.5	0.5	V MAX.
I^+	Positive Supply Current		42	40	mA MAX.
I^-	Negative Supply Current		34	32	mA MAX.
P_{DISS}	Power Dissipation		415	400	mW MAX.

Switching Characteristics (V^+ = +5.0V, V^- = −6.0V, V_{in} = 100mV, V_{od} = 5.0mV, C_L = 15pF) (Note 4)

t_{pd+}	Propagation Delay, Input to Output HIGH	T_A (min.) $\leq T_A \leq 25°C$	12	12	ns MAX.
		$T_A = T_A$ (max.)	15	15	ns MAX.
t_{pd-}	Propagation Delay, Input to Output LOW	T_A (min.) $\leq T_A \leq 25°C$	12	12	ns MAX.
		$T_A = T_A$ (max.)	15	15	ns MAX.
Δt_{pd}	Difference in Propagation Delay between Outputs	$T_A = 25°C$	2.0	2.0	ns MAX.

Notes: 2. For the metal can package, derate at 6.8mW/°C for operation at ambient temperatures above +95°C, for the dual-in-line package, derate at 9mW/°C for operation at ambient temperatures above 115°C.

3. Unless otherwise specified, V^+ = +5.0V, V^- = −6.0V and the Latch Enable input is at V_{OL}. The switching characteristics are for a 100mV input step with 5.0mV overdrive.

4. The outputs of the Am686 are unstable when biased into their linear range. In order to prevent oscillation, the rate-of-change of the input signal as it passes through the threshold of the comparator must be at least 1V/µs. For slower input signals, a small amount of external positive feedback may be applied around the comparator to give a few millivolts of hysteresis.

Data Conversion Products – Section III

Application Notes

AmDAC-08

8-Bit High Speed Multiplying D/A Converter

Distinctive Characteristics

- Fast settling output current – 85nsec
- Full scale current prematched to ±1.0 LSB
- Direct interface to TTL, CMOS, ECL, HTL, NMOS
- Nonlinearity to ±0.1% max over temperature range
- High output impedance and compliance −10V to +18V
- Differential current outputs
- Wide range multiplying capability 1.0MHz bandwidth
- Low FS current drift – ±10ppm/°C
- Wide power supply range – ±4.5V to ±18V
- Low power consumption – 33mW @ ±5V

3

GENERAL DESCRIPTION

The DAC-08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85 nsec settling times with very low "glitch" and a low power consumption. Monotonic multiplying performance is attained over more than a 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

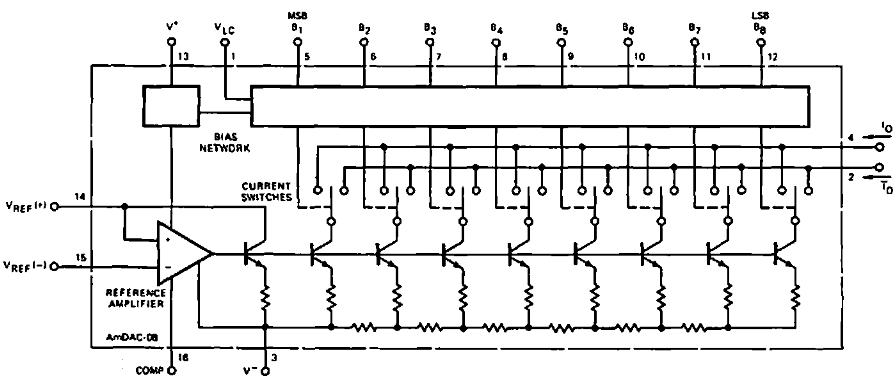
High voltage compliance dual complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications. All devices are processed to MIL-STD-883.

DAC-08 applications include 8-bit, 1.0μsec A/D converters, servo-motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high speed modems and other applications where low cost, high speed and complete input/output versatility are required.

EQUIVALENT CIRCUIT



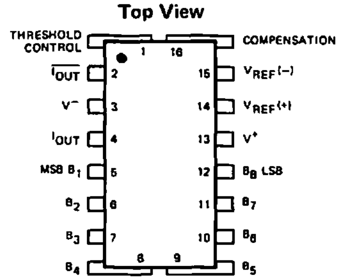
LIC-190

ORDERING INFORMATION

Order Number	Temperature Range	Nonlinearity
DAC-08AQ	−55°C to +125°C	±.1%
DAC-08Q	−55°C to +125°C	±.19%
DAC-08EQ	0°C to +70°C	±.19%
DAC-08CQ	0°C to +70°C	±.39%
DAC-08HQ	0°C to +70°C	±.1%
DAC-08HN	0°C to +70°C	±.1%
DAC-08EN	0°C to +70°C	±.19%
DAC-08CN	0°C to +70°C	±.39%

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

LIC-191

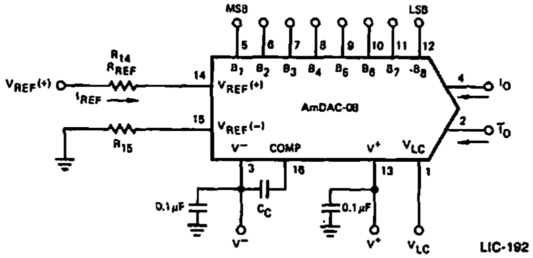
MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

Operating Temperature	
DAC-08AQ, Q	−55°C to +125°C
DAC-08EQ, CQ, HQ	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	500mW
Derate above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C
V+ supply to V− Supply	36V
Logic Inputs	V− to V+ plus 36V
V_{LC}	V− to V+
Analog Current Outputs	See Fig. 12
Reference Inputs (V_{14}, V_{15})	V− to V+
Reference Input Differential Voltage (V_{14} to V_{15})	±18V
Reference Input Current (I_{14})	5.0mA

ELECTRICAL CHARACTERISTICS (V_S = ±15V, I_{REF} = 2.0mA)

Parameter	Description	Test Conditions	AmDAC-08A AmDAC-08H Min.	Typ.	Max.	AmDAC-08 AmDAC-08E Min.	Typ.	Max.	AmDAC-08C Min.	Typ.	Max.	Units
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	8	8	8	Bits
	Nonlinearity	T_A = MIN. to MAX.			±0.1			±0.19			±0.39	%FS
t_s	Settling Time	To ±1/2 LSB, all bits switched ON or OFF T_A = 25°C; DAC-08A, DAC-08		85	135		85	135				ns
		DAC-08E, DAC-08C					85	150		85	150	
t_{PLH}, t_{PHL}	Propagation Delay, Each Bit	T_A = 25°C		35	60		35	60		35	60	ns
	Propagation Delay, All Bits Switched			35	60		35	60		35	60	
TCI_{FS}	Full Scale Tempco			±10	±50		±10	±50		±10	±80	ppm/°C
V_{OC}	Output Voltage Compliance	Full scale current change < 1/2 LSB R_{OUT} > 20MegΩ typ.	−10		+18	−10		+18	−10		+18	Volts
I_{FS4}	Full Scale Current	V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ T_A = 25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.89	2.04	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$		±0.8	±4.0		±1.0	±8.0		±2.8	±16	μA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0		0.2	4.0	μA
I_{FSR}	Output Current Range	V^- = −5.0V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		V^- = −7.0V to −18V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	
V_{IL}	Logic Input Levels, Logic "0"	V_{LC} = 0V			0.8			0.8			0.8	Volts
V_{IH}	Logic Input Levels, Logic "1"		2.0			2.0			2.0			
I_{IL}	Logic Input Current, Logic "0"	V_{LC} = 0V, V_{IN} = −10V to +0.8V		−2.0	−10		−2.0	−10		−2.0	−10	μA
I_{IH}	Logic Input Current, Logic "1"	V_{LC} = 0V, V_{IN} = 2.0V to 18V		0.002	10		0.002	10		0.002	10	
V_{IS}	Logic Input Swing	V^- = −15V	−10		+18	−10		+18	−10		+18	Volts
V_{THR}	Logic Threshold Range	V_S = ±15V	−10		+13.5	−10		+13.5	−10		+13.8	Volts
I_{15}	Reference Bias Current			−1.0	−3.0		−1.0	−3.0		−1.0	−3.0	μA
dI/dt	Reference Input Slew Rate		4.0	8.0		4.0	8.0		4.0	8.0		mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	V^+ = 4.5V to 18V		±0.0003	±0.01		±0.0003	±0.01		±0.0003	±0.01	%/%
$PSSI_{FS-}$		V^- = −4.5V to −18V I_{REF} = 1.0mA		±0.002	±0.01		±0.002	±0.01		±0.002	±0.01	
I^+	Power Supply Current	V_S = ±5.0V, I_{REF} = 1.0mA		2.3	3.8		2.3	3.8		2.3	3.8	mA
I^-				−4.3	−5.8		−4.3	−5.8		−4.3	−5.8	
I^+		V_S = +5.0V, −15V, I_{REF} = 2.0mA		2.4	3.8		2.4	3.8		2.4	3.8	
I^-				−6.4	−7.8		−6.4	−7.8		−6.4	−7.8	
I^+		V_S = ±15V, I_{REF} = 2.0mA		2.5	3.8		2.5	3.8		2.5	3.8	
I^-				−6.5	−7.8		−6.5	−7.8		−6.5	−7.8	
P_D	Power Dissipation	±5.0V, I_{REF} = 1.0mA		33	48		33	48		33	48	mW
		+5.0V, −15V, I_{REF} = 2.0mA		108	136		108	136		108	136	
		±15V, I_{REF} = 2.0mA		135	174		135	174		135	174	

BASIC CONNECTIONS



$$I_{FS} = \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$ FOR ALL LOGIC STATES

FOR FIXED REFERENCE, TTL OPERATION, TYPICAL VALUES ARE:

$V_{REF} = +10.000V$
$R_{REF} = 5.000k$
$R_{15} \approx R_{REF}$
$C_C = 0.01\mu F$
$V_{LC} = 0V$ (GROUND)

Figure 1. Basic Positive Reference Operation.

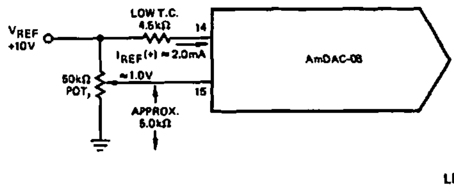
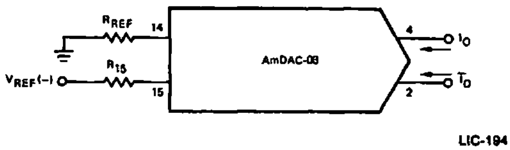


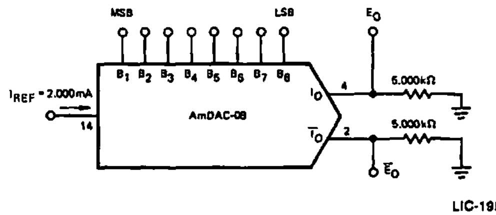
Figure 2. Recommended Full Scale Adjustment Circuit.



$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

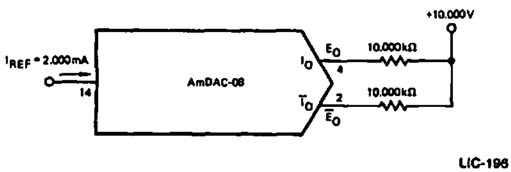
Note 1. R_{REF} Sets I_{FS}; R_{15} is for Bias Current Cancellation.

Figure 3. Basic Negative Reference Operation.



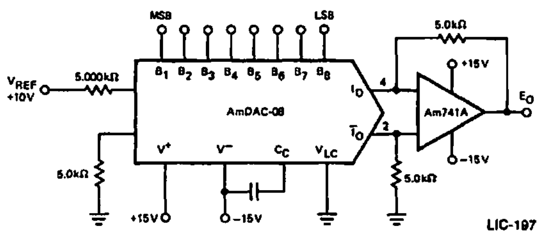
	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
FULL SCALE	1	1	1	1	1	1	1	1	1.992	000	−9.960	000
FULL SCALE −LSB	1	1	1	1	1	1	1	0	1.984	.008	−9.920	−.040
HALF SCALE +LSB	1	0	0	0	0	0	0	1	1.008	.984	−5.040	−4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	.992	−5.000	−4.960
HALF SCALE −LSB	0	1	1	1	1	1	1	1	.992	1.000	−4.960	−5.000
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	.008	1.984	−.040	−9.920
ZERO SCALE	0	0	0	0	0	0	0	0	.000	1.992	.000	−9.960

Figure 4. Basic Unipolar Negative Operation.



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS FULL SCALE	1	1	1	1	1	1	1	1	−9.920	+10.000
POS FULL SCALE −LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
ZERO SCALE +LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	+0.080
ZERO SCALE −LSB	0	1	1	1	1	1	1	1	+0.080	0.000
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	+10.000	−9.920

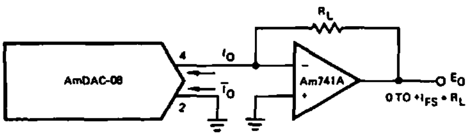
Figure 5. Basic Bipolar Output Operation.



	B1	B2	B3	B4	B5	B6	B7	B8	E_O
POS FULL SCALE	1	1	1	1	1	1	1	1	+9.960
POS FULL SCALE −LSB	1	1	1	1	1	1	1	0	+9.880
(+) ZERO SCALE	1	0	0	0	0	0	0	0	+0.040
(−) ZERO SCALE	0	1	1	1	1	1	1	1	−0.040
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	−9.880
NEG FULL SCALE	0	0	0	0	0	0	0	0	−9.960

Figure 6. Symmetrical Offset Binary Operation.

BASIC CONNECTIONS (Cont.)

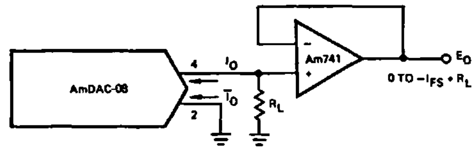


LIC-198

$$I_{FS} \cong \frac{255}{256} I_{REF}$$

FOR COMPLEMENTARY OUTPUT (OPERATION AS NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2), CONNECT I_O (PIN 4) TO GROUND

Figure 7. Positive Low Impedance Output Operation.

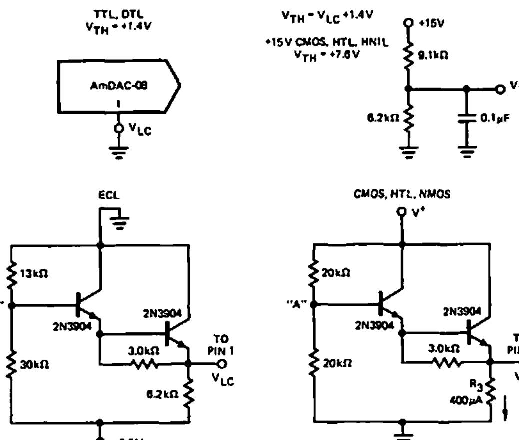


LIC-199

$$I_{FS} \cong \frac{255}{256} I_{REF}$$

FOR COMPLEMENTARY (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

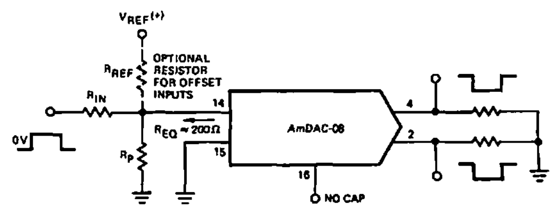
Figure 8. Negative Low Impedance Output Operation.



LIC-200

SET VOLTAGE AT NODE "A" EQUAL TO DESIRED LOGIC THRESHOLD.

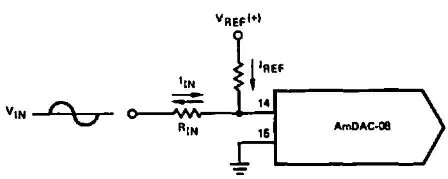
Figure 9. Interfacing With Various Logic Families.



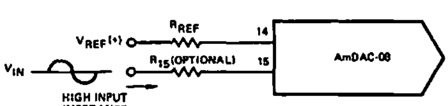
LIC-201

TYPICAL VALUES:
R_{IN} = 5k
$+V_{IN}$ = 10V

Figure 10. Pulsed Reference Operation.



a) $I_{REF} \geq$ Peak Negative Swing of I_{IN}.

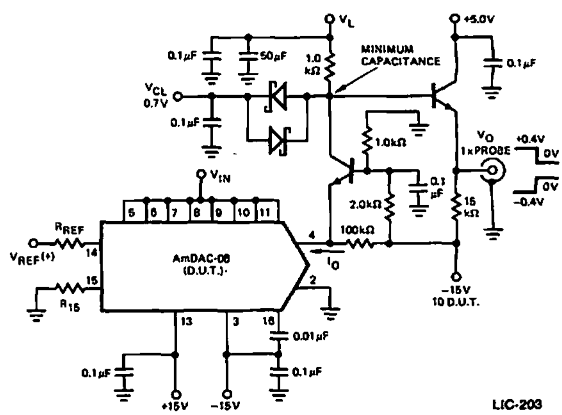


$R_{REF} \approx R_{15}$

LIC-202

b) $+V_{REF}$ Must Be Above Peak Positive Swing of V_{IN}.

Figure 11. Accomodating Bipolar References.



LIC-203

FOR TURN-ON, V_L = 2.7V
FOR TURN-OFF, V_L = 0.7V

Figure 12. Settling Time Measurement.

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SET-UP

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FS} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = I_{14}.$$

In positive reference applications (Fig. 1), an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15 (Fig. 3); reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors; R_{15} may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15 as shown in Fig. 11. The negative common mode range of the reference amplifier is given by: $V_{CM}- = V-$ plus ($I_{REF} \times 1.0k\Omega$) plus 2.5V. The positive common mode range is V+ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, a +10.0V reference is recommended for optimum full scale temperature coefficient performance. This will minimize the contributions of reference amplifier V_{OS} and TCV_{OS}. For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}. An improved method of full scale trimming which eliminates potentiometer T.C. effects is shown in Fig. 2.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 16 to V−. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC-08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4.0mA to 4.0μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA; consult factory for devices selected for monotonic operation over wider I_{REF} ranges.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to pin 14: for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1.0kΩ and C_C = 15pF, the reference amplifier slews at 4.0mA/μs enabling a transition from I_{REF} = 0 to I_{REF} = 2.0mA in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme shown in Fig. 10. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full scale transition (0 to 2.0mA) occurs in 120ns when the equivalent impedance at pin 14 is 200Ω and C_C = 0. This yields a reference slew rate of 16mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2.0μA logic input current and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V− plus ($I_{REF} \times 1.0k\Omega$) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1.0mA is recommended. For interfacing other logic families, see Fig. 9. For general set-up of the logic control circuit, it should be noted that pin 1 will source 100μA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1.0kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided, when $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V− and is independent of the positive supply. Negative compliance is given by V− plus ($I_{REF} \cdot 1.0k\Omega$) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leqslant 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range. For example, operation at −4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required: however, an artificial ground may be useful to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:

P_d = (I+) (V+) + (I+) (V−) + (2 I_{REF}) (V−). A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is tight, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

Full scale output drift performance will be best with +10.0V references as V_{OS} and TCV_{OS} of the reference amplifier will be very small compared to 10.0V. The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC-08 decrease approximately 10% at −55°C; at +125°C an increase of about 15% is typical.

SETTLING TIME

The DAC-08 is capable of extremely fast settling times, typically 85nsec at I_{REF} = 2.0mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35nsec for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35nsec, with each progressively larger bit taking successively longer. The MSB settles in 85nsec, thus determining the overall settling time of 85nsec. Settling to 6-bit accuracy requires about 65 to 70nsec. The output capacitance of the DAC-08 including the package is approximately 15pF, therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4μA, therefore a 1kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of Fig. 12 uses a cascode design to permit driving a 1kΩ load with less than 5pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC-08 switching transients of "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

LF198/LF298/LF398

Monolithic Sample and Hold Circuits

Distinctive Characteristics

- Operates from ±5V to ±18V supplies
- Less than 10μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at $C_h = 0.01\mu F$
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

GENERAL DESCRIPTION

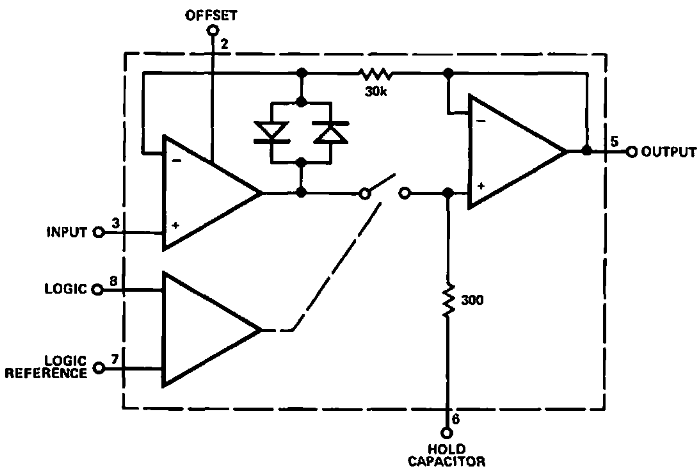
The LF198/LF298/LF398 are BI-FET monolithic sample and hold circuits with ultra-high DC accuracy, fast acquisition time (6μs to 0.01%) and low droop rate. A bipolar input stage is used to obtain the lowest possible offset voltage and wide bandwidth. These circuits are designed to have high common mode rejection and a gain accuracy of 0.002%. High input impedance ($10^{10}\Omega$) permits their use with a high impedance source without degrading accuracy.

The output buffer has a p-channel JFET input with a typical input current of 30pA, giving a droop rate as low as 5mV/Min with a 1μF hold capacitor. The JFET has a very low noise level and high temperature stability.

A differential logic input allows the logic to be referenced to a separate ground from analog ground, permitting a direct interface to nearly any logic family. The LF198 series guarantees no feed through in the hold mode including input signal swings equal to the power supply.

3

FUNCTION DIAGRAM



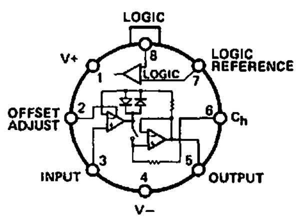
LIC-204

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
LF398	Metal Can Dice	0°C to +70°C	LF398H LD398
LF298	Metal Can	−25°C to +85°C	LF298H
LF198	Metal Can Dice	−55°C to +125°C	LF198H LD198

CONNECTION DIAGRAM

Metal Can
Top View



LIC-205

ABSOLUTE MAXIMUM RATINGS

Operating Ambient Temperature Range	
LF198	−55°C to +125°C
LF298	−25°C to +85°C
LF398	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (Package Limitation, Note 1)	500mW
Supply Voltage	±18V
Input Voltage	Equal to Supply Voltage
Logic to Logic Reference Differential Voltage (Note 2)	+7V, −30V
Hold Capacitor Short Circuit Duration	10 sec
Lead Temperature (Soldering 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (Note 3)

Parameter	Test Conditions	LF198/LF298 Min.	LF198/LF298 Typ.	LF198/LF298 Max.	LF398 Min.	LF398 Typ.	LF398 Max.	Unit
Input Offset Voltage, (Note 6)	$T_j = 25°C$		1	3		2	7	mV
	Full Temperature Range			5			10	mV
Input Bias Current, (Note 6)	$T_j = 25°C$		5	25		10	50	nA
	Full Temperature Range			75			100	nA
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k\Omega$		0.002	0.005		0.004	0.01	%
	Full Temperature Range			0.02			0.02	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\mu F$	86	96		80	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode		0.5	2		0.5	4	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 4)	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply Current, (Note 6)	$T_j > 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	$T_j = 25°C$, (Note 5) Hold Mode		30	100		30	200	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000$ pF		4			4		μs
	$C_h = 0.01\mu F$		20			20		μs
Hold Capacitor Charge Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

Notes: 1. The maximum junction temperature is 150°C for the LF198, 115°C for the LF298, and 100°C for the LF398. When used at a higher ambient temperature, the TO-5 can package must be derated based on a thermal resistance (θjA) of 150°C/W.

2. The differential voltage may not exceed this limit. The common mode voltage on the logic pins may equal the supply voltage without causing damage to the device. For the LF198 to operate properly, one of the logic pins must be at least 2V below the positive supply and 3V above the negative supply.

3. The following conditions apply unless otherwise noted: Device is in "sample mode". $T_j = 25°C$, $V_S = \pm 15V$, $-11.5V < V_{IN} < +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k\Omega$. Logic reference voltage = 0V. Logic input voltage = 2.5V.

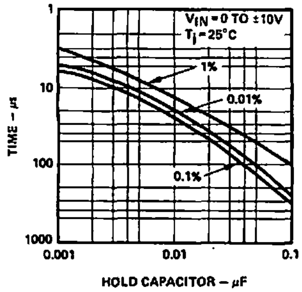
4. The hold step is produced by a charge which is coupled from the logic input signal to the hold capacitor via parasitic capacitance and internal operating point changes. Stray capacitance equal to 1pF will create a 0.5mV step with a 5 volt logic swing and a 0.01μF hold capacitor. This step can be reduced by increasing the magnitude of the hold capacitor.

5. Leakage current is measured at a junction temperature of 25°C. The junction temperature doubles the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over the full input signal range.

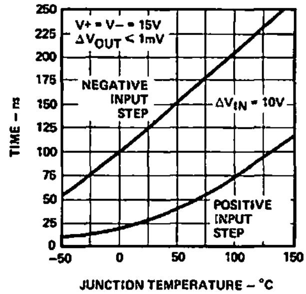
6. These values are guaranteed over the ±5 to ±18V supply range.

TYPICAL PERFORMANCE CHARACTERISTICS

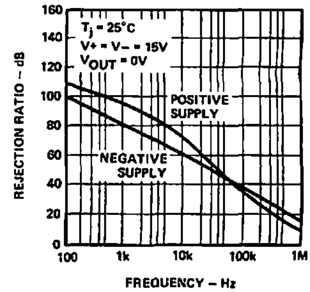
Acquisition Time



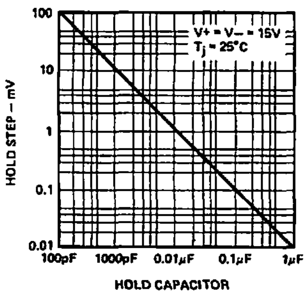
Aperture Time



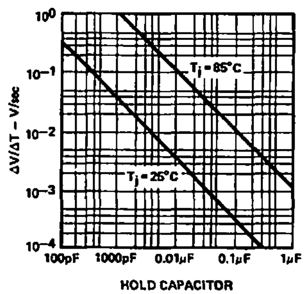
Power Supply Rejection



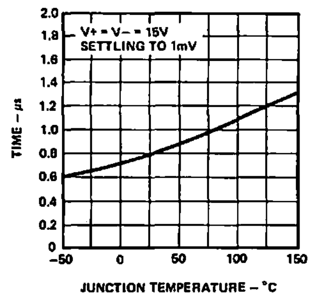
Hold Step



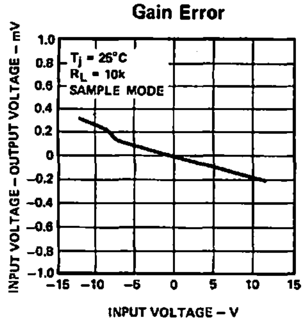
Output Droop Rate



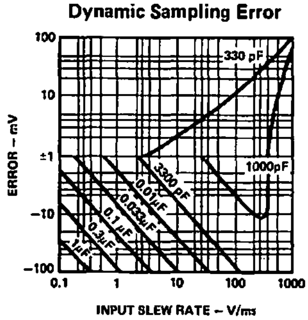
"Hold" Settling Time



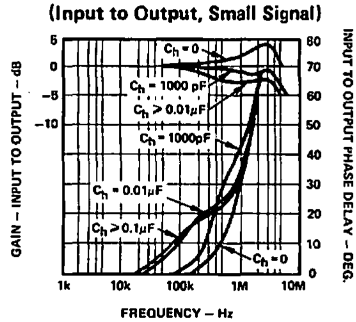
Gain Error



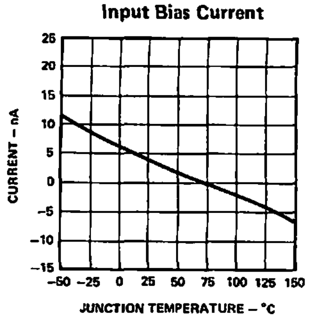
Dynamic Sampling Error



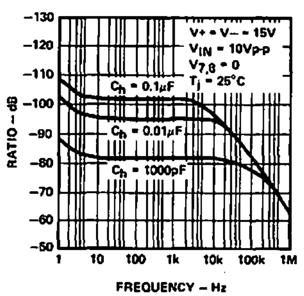
Phase and Gain (Input to Output, Small Signal)



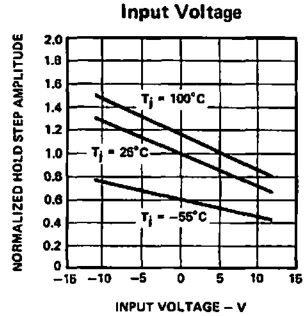
Input Bias Current



Feedthrough Rejection Ratio (Hold Mode)



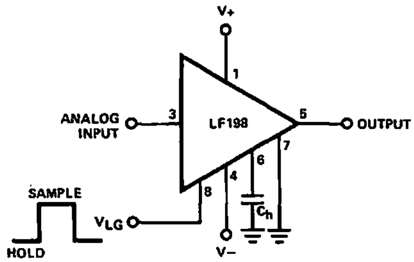
Hold Step Versus Input Voltage



LIC-206

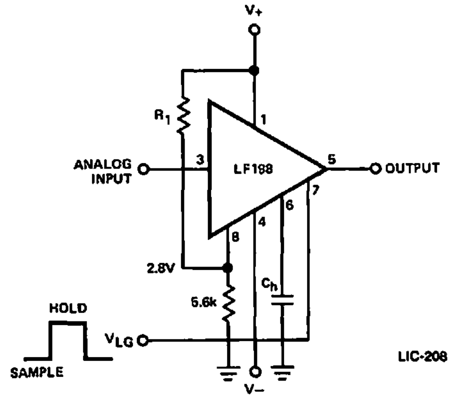
LOGIC INPUT CONFIGURATIONS

TTL AND CMOS
3V ≤ V_{LG}(HI STATE) ≤ 7V



LIC-207

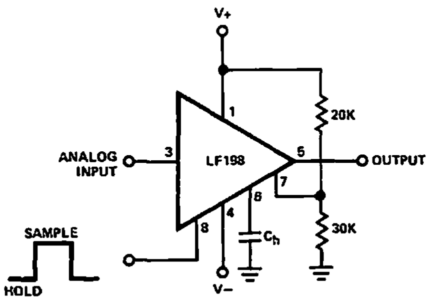
Threshold = 1.4V



LIC-208

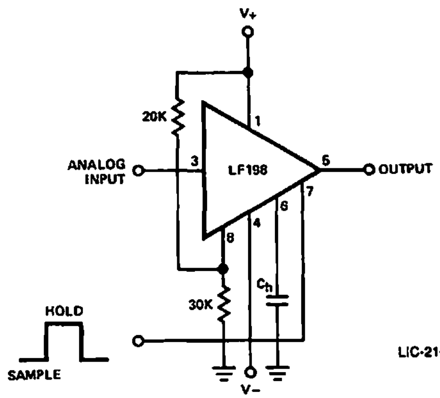
Threshold = 1.4V
R_1 select for 2.8V at Pin 8

CMOS
7V ≤ V_{LG}(HI STATE) ≤ 15V



LIC-209

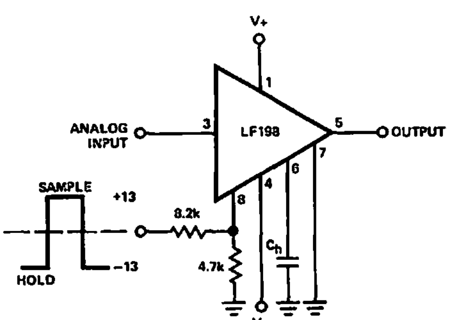
Threshold = 0.6 (V+) + 1.4V



LIC-210

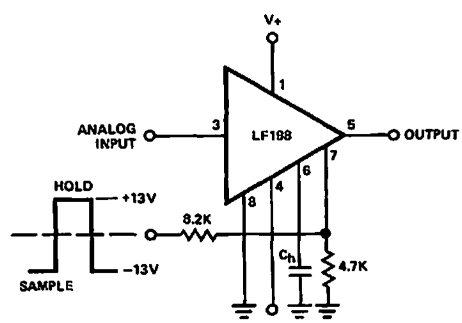
Threshold = 0.6 (V+) − 1.4V

OP AMP DRIVE
OUTPUT VOLTAGE ≈ ±13V



LIC-211

Threshold ≃ 4V



LIC-212

Threshold = −4V

APPLICATION INFORMATION

Freezing the input to an analog-to-digital (A/D) converter is an important application for the sample and hold amplifier. If the analog input to the A/D changes during conversion by the amount ±1/2LSB, an ideal A/D would produce 1 LSB error beyond normal quantization error. A sample and hold amplifier eliminates this problem by holding the input signal to the A/D converter during the conversion interval. The proper choice of hold capacitor value and type is necessary to obtain optimum performance. The capacitor value directly affects several circuit parameters, particularly acquisition time, droop rate, and hold step. The hold step error is inversely proportional to the value of the hold capacitor.

Graphs are provided in this data sheet for use as guides in selecting a suitable value of capacitance. However, the capacitor should have extremely high insulation resistance and low dielectric absorption, or dielectric hysteresis. Polypropylene (below +85°C) and Teflon (above +85°C) types are recommended. The hysteresis error can be significantly reduced if the output of the LF198 is digitized immediately after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10-50ms, thus if A/D conversion can be made within 1ms, hysteresis error will be reduced by a factor of ten.

The logic inputs on the LF198 are fully differential with low input current and will operate from TTL levels up to 15V. Some typical logic input configurations are shown in this data sheet. The logic signal into the LF198 must have a minimum slew rate of 0.2V/µs. Slower signals cause excess hold step errors.

When switched from sample to hold, delay in response to the hold command (aperture time and aperture time uncertainty) can cause the frozen value of a fast moving waveform to differ from the value it had at the instant the hold command is given. However, the hold capacitor has an additional lag due to the 300Ω series resistor on the chip which cancels out some of the error due to aperture time and aperture time uncertainty.

For example, using an analog input of 20 volts p-p at 10kHz, maximum slew rate 0.5V/µs, with no phase delay and 80ns logic delay, one could expect up to (0.08µs) • (0.5V/µs) = 40mV error if the input is sampled during the maximum dv/dt period. A positive going input would give a +40mV error. Assume that the slew rate of the charging amplifier and the RC constant of the analog loop cause a delay of 120ns. If the hold capacitor sees this exact delay, then the analog delay would be (0.5µV/sec)•(.12µs) = −60mV. Total output error is +40mV −60mV = −20mV.

For a sample and hold amplifier in a multiplexed A/D system, acquisition and aperture times are critical parameters. In order to maintain the acquired signal level within the specified accuracy, these times must be considered when selecting the sampling rate. For example, if a 16 channel MUX drives a sample and hold amplifier in which each channel is 5KHz and 2 samples per cycle are needed to satisfy the Nyquist criteria, the minimum sampling rate = 160000 samples/sec. ((5KHz X 16) cycles/sec X 2 samples/cycle). The minimum channel period is the reciprocal of the sampling rate of 6.25µs. During the hold mode the MUX can switch to another channel. This eliminates the need to consider the MUX and source settling time and shortens the channel period.

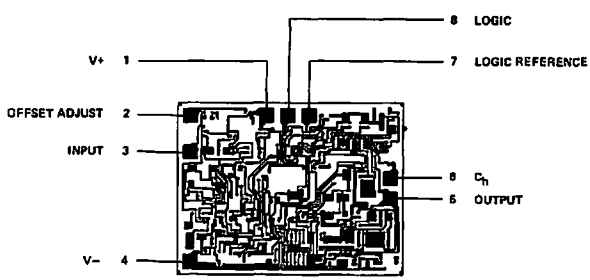
Calculating the sum of the sample and hold acquisition time, aperture time and A/D conversion time is usually a convenient method for estimating maximum channel period.

In multiplex applications, sample and hold feed-through is a significant problem. Since each channel voltage differs, the sample and hold input signal becomes a series of varied height pulses that cause errors in the sample and hold voltage.

Digital feed through occurs when a fast rising logic signal is coupled into the analog input. To minimize it, the logic signal trace in the PCB layout should be kept as far as possible from the analog input. Guarded trace may also be used around the input pin for shielding purposes.

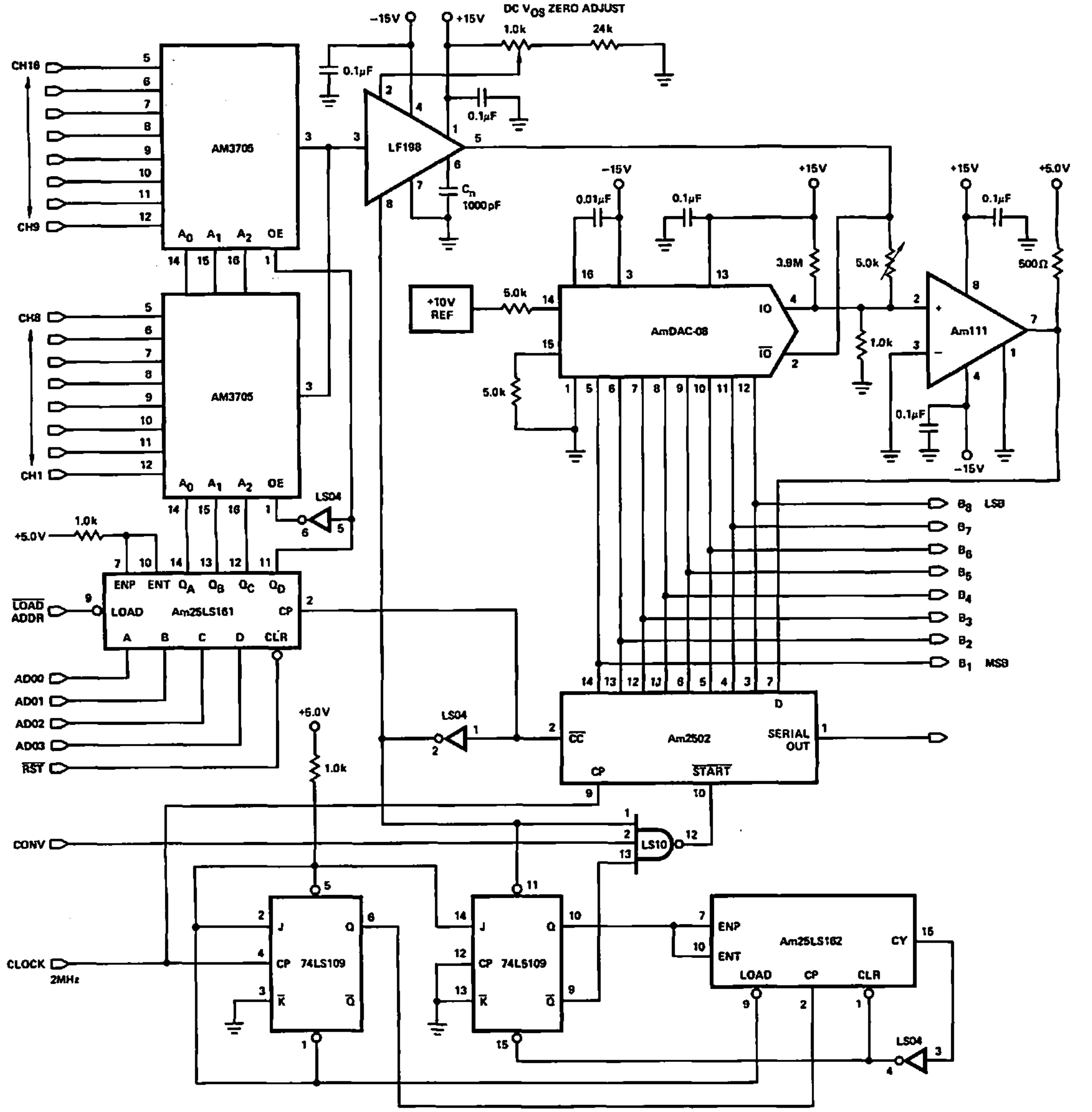
To adjust the DC offset zeroing, the wiper of a 1K potentiometer is connected to the offset adjust pin. One end of the potentiometer is connected to VCC and the other is connected through a resistor to ground. The value of the resistor is selected such that the current flows through it at approximately 6mA.

Metallization and Pad Layout



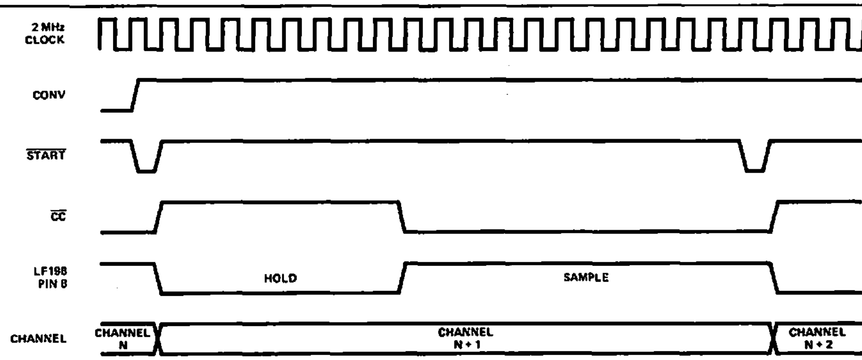
51 X 66 Mils

APPLICATIONS



SEQUENTIAL ADDRESSING OVERLAP MODE A/D CONVERSION

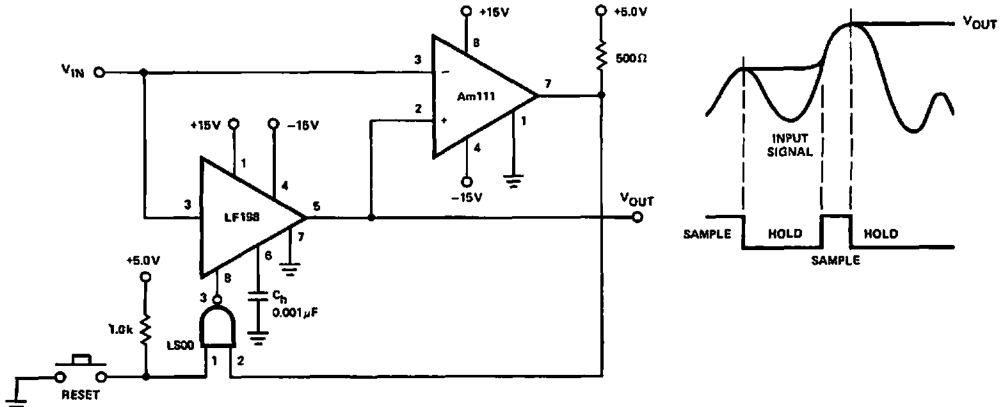
LIC-213



TIMING DIAGRAM FOR SEQUENTIAL ADDRESSING OVERLAP MODE A/D CONVERSION

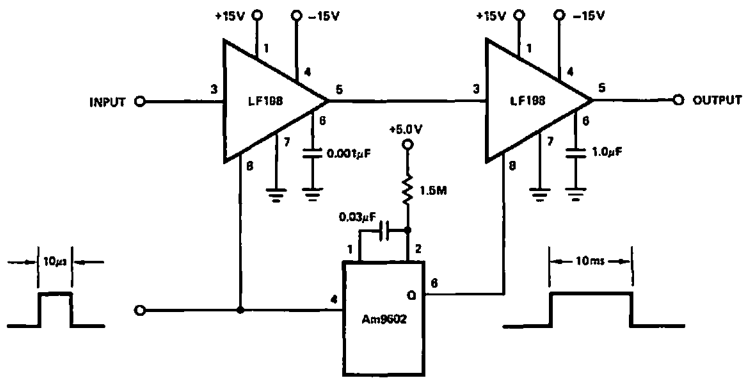
LIC-214

APPLICATIONS (Cont.)



TRACK AND HOLD PEAK RECORDER

LIC-215



FAST ACQUISITION, LOW DROOP SAMPLE AND HOLD

LIC-216

DEFINITION OF TERMS

Acquisition Time – The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture time – The delay between the command to hold and the actual opening of the hold switch.

Aperture time uncertainty – The tolerance, or jitter of the aperture time.

Droop rate – The rate of change of output voltage in the hold mode. It is caused by leakage currents at the hold capacitor node.

Feed-through – During hold, a small part of the input signal feeds through the capacitor of the switch to the hold capacitor and output. This is usually a function of the level and frequency of the input signal and is expressed in dB.

Dynamic sampling error – The error introduced into the outputs due to input voltage varying when the hold command is issued. Error is expressed in mV with a given hold capacitor.

Gain error – The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold step – The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (DC) analog input voltage.

Am1508/1408 • SSS1508A/1408A

8-Bit Multiplying D/A Converter

Distinctive Characteristics

- Improved direct replacement for MC1508/1408
- ±0.19% nonlinearity guaranteed over temperature range
- Improved settling time (SSS1508A/1408A) 250ns, typ.
- Improved power consumption (SSS1508A/1408A) 157mW, typ.
- Compatible with TTL, CMOS logic
- Standard supply voltage: +5.0V and −5.0V to −15V
- Output voltage swing: +0.5V to −5.0V
- High speed multiplying input: 4.0mA/μs

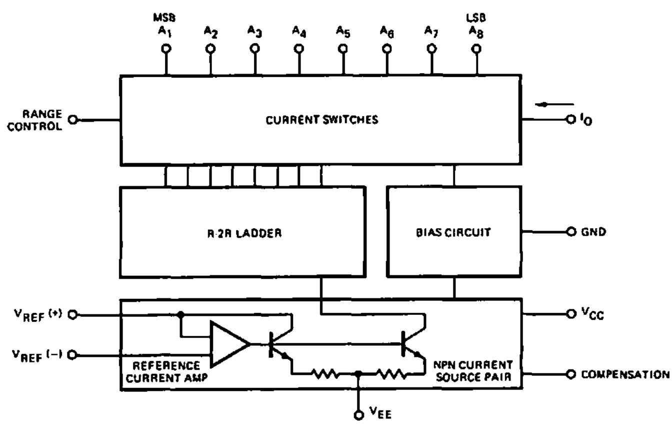
FUNCTIONAL DESCRIPTION

The SSS1508A/1408A, Am1508/1408 are 8-bit monolithic multiplying Digital-to-Analog Converters consisting of a reference current amplifier, an R-2R ladder, and eight high speed current switches. For many applications, only a reference resistor and reference voltage need be added. Improvements in design and processing techniques provide faster settling times combined with lower power consumption while retaining direct interchangeability with MC1508/1408 devices.

The R-2R ladder divides the reference current into eight binarily-related components which are fed to the switches. A remainder current equal to the least significant bit is always shunted to ground, therefore the maximum output current is 255/256 of the reference amplifier input current. For example, a full scale output current of 1.992mA would result from a reference input current of 2.0mA.

The SSS1508A/1408A, Am1508/1408 is useful in a wide variety of applications, including waveform synthesizers, digitally programmable gain and attenuation blocks, CRT character generation, audio digitizing and decoding, stepping motor drives, programmable power supplies and in building Tracking and Successive Approximation Analog-to-Digital Converters.

BLOCK DIAGRAM

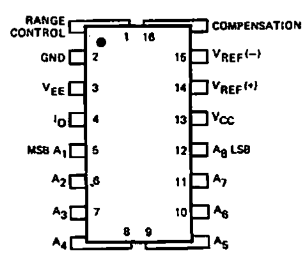


LIC-217

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am1408	Hermetic DIP	0°C to +70°C	AM1408L8
	Hermetic DIP	0°C to +70°C	AM1408L7
	Hermetic DIP	0°C to +70°C	AM1408L6
	Hermetic DIP	0°C to +70°C	SSS1408A-8Q
	Hermetic DIP	0°C to +70°C	SSS1408A-7Q
	Hermetic DIP	0°C to +70°C	SSS1408A-6Q
	Plastic DIP	0°C to +70°C	AM1408N8
	Plastic DIP	0°C to +70°C	AM1408N7
	Plastic DIP	0°C to +70°C	AM1408N6
	Dice	0°C to +70°C	LD1408
Am1508	Hermetic DIP	−55°C to +125°C	AM1508L8
	Hermetic DIP	−55°C to +125°C	SSS1508A-8Q
	Dice	−55°C to +125°C	LD1508

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-218

MAXIMUM RATINGS (Above which the useful life may be impaired)

(T_A = +25°C unless otherwise noted)

Power Supply Voltage	
V_{CC}	+5.5Vdc
V_{EE}	−16.5Vdc
Digital Input Voltage, V_5–V_{12}	+5.5, 0Vdc
Applied Output Voltage, V_O	+0.5, −5.2Vdc
Reference Current, I_{14}	5.0mA
Reference Amplifier Inputs, V_{14}, V_{15}	V_{CC}, V_{EE} Vdc
Power Dissipation (Package Limitation), P_D	
Ceramic Package	1000mW
Derate above T_A = +25°C	6.7mW/°C
Operating Temperature Range, T_A	
SSS1508A-8, Am1508	−55°C to +125°C
SSS1408A Series, Am1408 Series	0°C to +75°C
Storage Temperature, T_{stg}	−65°C to +150°C

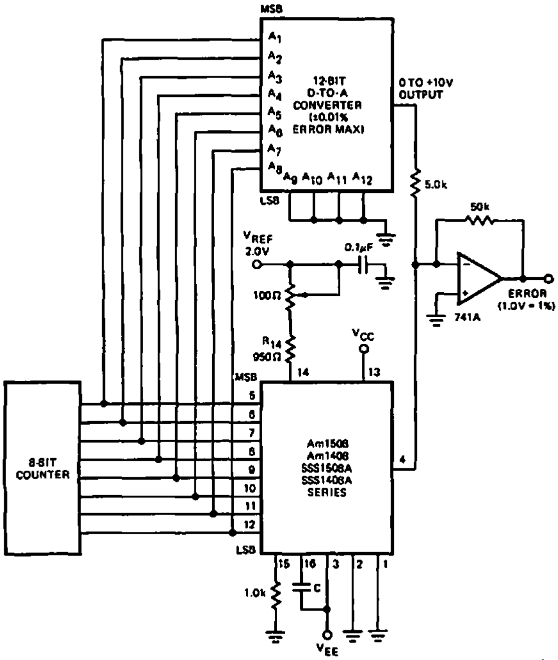
ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

(V_{CC} = 5.0Vdc, V_{EE} = −15Vdc, $\frac{V_{ref}}{R_{14}}$ = 2.0mA, SSS1508A-8/Am1508L8: T_A = −55°C to +125°C, SSS1408A/Am1408 Series: T_A = 0°C to +75°C unless otherwise noted. All digital inputs at high logic level.)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
E_R	Relative Accuracy					% IFS
	SSS1508A-8, SSS1408A-8, Am1508L8, Am1408L8				±0.19	
	SSS1408A-7, Am1408L7				±0.39	
	SSS1408A-6, Am1408L6				±0.78	
t_S	Settling Time to within 1/2 LSB (includes t_{PLH})					ns
	SSS1508A/1408A	T_A = +25°C		250		
	Am1508/1408			300		
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = +25°C		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		PPM/°C
	Digital Input Logic Levels (MSB)					Vdc
V_{IH}	High Level, Logic "1"		2.0			
V_{IL}	Low Level, Logic "0"				0.8	
I_{IH}	Digital Input Current (MSB)	High Level, V_{IH} = 5.0V		0	0.04	mA
I_{IL}		Low Level, V_{IL} = 0.8V		−0.002	−0.8	
I_{15}	Reference Input Bias Current (Pin 15)					µA
	SSS1508A/1408A			−1.0	−3.0	
	Am1508/1408			−1.0	−5.0	
I_{OR}	Output Current Range	V_{EE} = −5.0V	0	2.0	2.1	mA
		V_{EE} = −7.0V to −15V	0	2.0	4.2	
I_O	Output Current	V_{ref} = 2.000V, R_{14} = 1000Ω	1.9	1.99	2.1	mA
$I_{O(min.)}$	Output Current (All Bits Low)			0	4.0	µA
V_O	Output Voltage Compliance	V_{EE} = −5V			−0.6, +0.5	Vdc
	(E_r ≤ 0.19% at T_A = +25°C)	V_{EE} below −10V			−5.0, +0.5	
SRI_{ref}	Reference Current Slew Rate			4.0		mA/µs
$PSSI_O$	Output Current Power Supply Sensitivity			0.5	2.7	µA/V
	Power Supply Current					mA
I_{CC}	SSS1508A/1408A			2.5	14	
I_{EE}				−6.4	−13	
I_{CC}	Am1508/1408			2.5	22	
I_{EE}				−6.4	−13	
V_{CCR}	Power Supply Voltage Range	T_A = +25°C	4.5	5.0	5.5	Vdc
V_{EER}			−4.5	−15	−16.5	
P_d	Power Dissipation					mW
	SSS1508A/1408A	All Bits Low				
		V_{EE} = −5.0Vdc		34	136	
		V_{EE} = −15Vdc		108	265	
		All Bits High				
		V_{EE} = −5.0Vdc		34		
		V_{EE} = −15Vdc		108		
	Am1508/1408	All Bits Low				
		V_{EE} = −5.0Vdc		34	170	
		V_{EE} = −15Vdc		108	305	
		All Bits High				
		V_{EE} = −5.0Vdc		34		
		V_{EE} = −15Vdc		108		

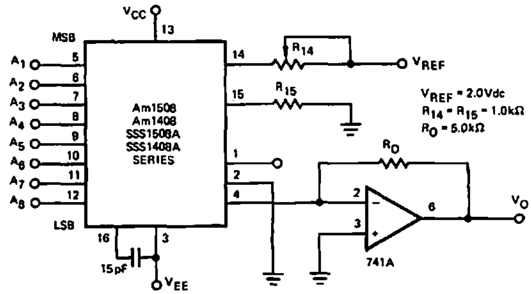
TYPICAL APPLICATIONS

RELATIVE ACCURACY TEST CIRCUIT



LIC-219

USE WITH CURRENT-TO-VOLTAGE CONVERTING OP AMP



THEORETICAL V_O

$$V_O = \frac{V_{REF}}{R_{14}}(R_O)\left[\frac{A_1}{2}+\frac{A_2}{4}+\frac{A_3}{8}+\frac{A_4}{16}+\frac{A_5}{32}+\frac{A_6}{64}+\frac{A_7}{126}+\frac{A_8}{256}\right]$$

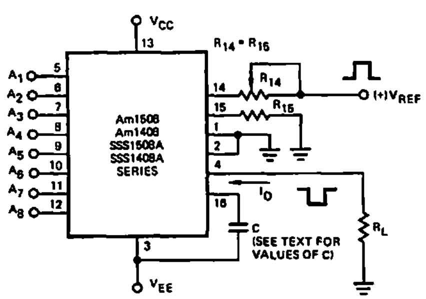
ADJUST V_{REF}, R_{14} OR R_O SO THAT V_O WITH ALL DIGITAL INPUTS AT HIGH LEVEL IS EQUAL TO 9.961 VOLTS

$$V_O = \frac{2V}{1k}(5k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{126}+\frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

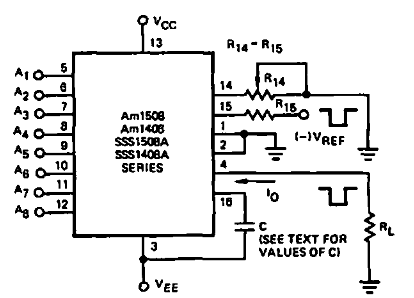
LIC-220

USE WITH POSITIVE V_{REF}



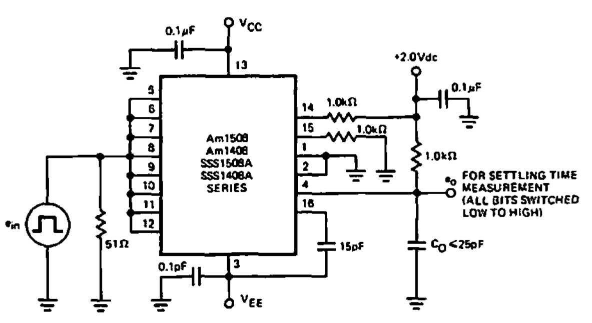
LIC-221

USE WITH NEGATIVE V_{REF}



LIC-222

TRANSIENT RESPONSE AND SETTLING TIME TEST CIRCUIT



LIC-223

GENERAL INFORMATION AND APPLICATION NOTES

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14} must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive voltage are shown on page 3. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R_{15} with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R_{14} to maintain proper phase margin; for R_{14} values of 1.0, 2.5 and 5.0 kilohms, minimum capacitor values are 15, 37, and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} as shown. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4.0 volts above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be decoupled by connecting it to +5.0V through another resistor and bypassing the junction of the two resistors with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.6 to +0.5 volts when V_{EE} = −5.0V due to the current switching methods employed in the SSS1508A-8, Am1508.

The negative output voltage compliance of the SSS1508A-8, Am1508 is extended to −5.0V where the negative supply voltage is more negative than −10 volts. Using a full scale current of 1.992mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance but a 2.5-kilohm load increases "worst case" settling time to 1.2μS (when all bits are switched on). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2mA may be used only for negative supply voltages more negative than −7.0 volts, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the SSS1508A-8, Am1508 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the SSS1508A-8 has a very low full scale current drift with temperature.

The SSS1508A-8/Am1508 Series is guaranteed accurate to within ±1/2 LSB at a full scale output current of 1.992mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0mA, with the loss of one LSB (8.0μA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown on page 3. The 12-bit converter is calibrated for a full scale output current of 1.992mA. This is an optional step since the SSS1508A-8, Am1508 accuracy is essentially the same between 1.5 and 2.5mA. Then the SSS1508A-8, Am1508 circuits' full scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65,536 or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the SSS1508A-8, Am1508.

MULTIPLYING ACCURACY

The SSS1508A-8, Am1508 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16μA to 4.0mA, the additional error contributions are less than 1.6μA. This is well within eight-bit accuracy when referred to full scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the SSS1508A-8, Am1508 is monotonic for all values of reference current above 0.5mA. The recommended range for operation with a dc reference current is 0.5 to 4.0mA.

SETTLING TIME

The "worst case" switching condition occurs when all bits are switched "on," which coresponds to a LOW-to-HIGH transition for all bits. This time is typically 250ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100ns. These times apply when $R_L \leqslant 500$ ohms and $C_O \leqslant 25$pF.

The slowest single switch is the least significant bit. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 250ns may be realized.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

Am2502/2503/2504

Eight-Bit/Twelve-Bit Successive Approximation Registers

Distinctive Characteristics

- Contains all the storage and control for successive approximation A-to-D converters.
- Provision for register extension or truncation.
- Can be operated in START-STOP or continuous conversion mode.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Can be used as serial-to-parallel converter or ring counters.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

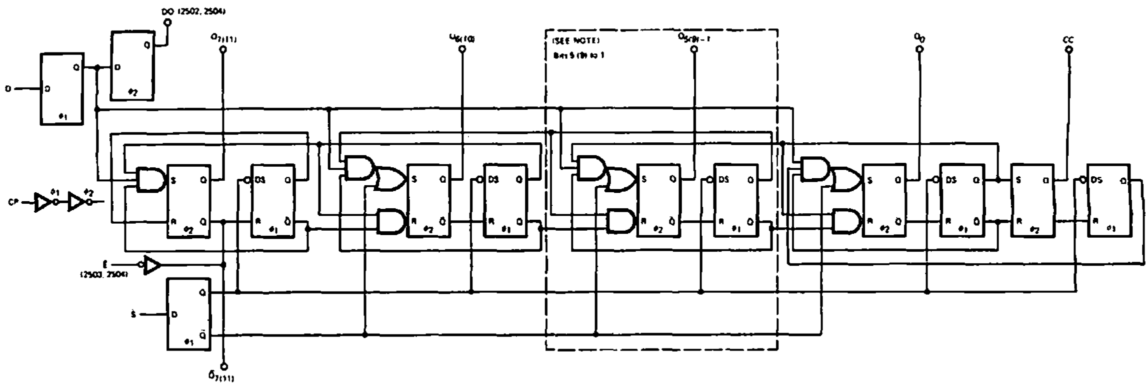
The Am2502, Am2503 and Am2504 are 8-bit and 12-bit TTL Successive Approximation Registers. The registers contain all the digital control and storage necessary for successive approximation analog-to-digital conversion. They can also be used in digital systems as the control and storage element in recursive digital routines.

The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the Am2502 and Am2504 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state $Q_7(11)$ LOW, (Note 2) and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. The $\overline{S}$ signal should not be brought back HIGH until after the clock LOW-to-HIGH transition in order to guarantee correct resetting. After the clock has gone HIGH resetting the register, the $\overline{S}$ signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the $Q_7(11)$ register bit and the $Q_6(10)$ register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the $Q_6(10)$ register bit and $Q_5(9)$ is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q_0, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

In order to allow complementary conversion the complementary output of the most significant register bit is made available. An active LOW enable input, $\overline{E}$, on the Am2503 and Am2504 allows devices to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs together and connecting the $\overline{CC}$ output of one device to the $\overline{E}$ input of the next less significant device. When the Start signal resets the register, the $\overline{E}$ signal goes HIGH, forcing the $Q_7(11)$ bit HIGH and inhibiting the device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used the $\overline{E}$ input should be held at a LOW logic level (Ground). If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the $\overline{CC}$ signal to indicate the end of conversion.

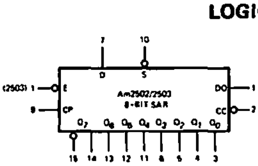
LOGIC DIAGRAMS



Notes: 1. Cell logic is repeated for register stages. Q_5 to Q_1 Am2502/3, Q_9 to Q_1 Am2504.
2. Numbers in parentheses are for Am2504.

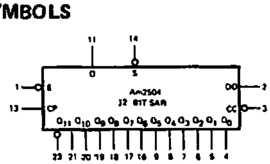
LIC-224

LOGIC SYMBOLS



LIC-225

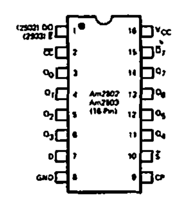
V_{CC} = Pin 16
GND = Pin 8



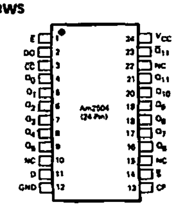
LIC-226

V_{CC} = Pin 24
GND = Pin 12
NC = Pins 10, 16 22

CONNECTION DIAGRAMS
Top Views



LIC-227



Note: Pin 1 is marked for orientation.

LIC-228

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential Continuous	–0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	–0.5 V to $+V_{CC}$ max
DC Input Voltage	–0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	–30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

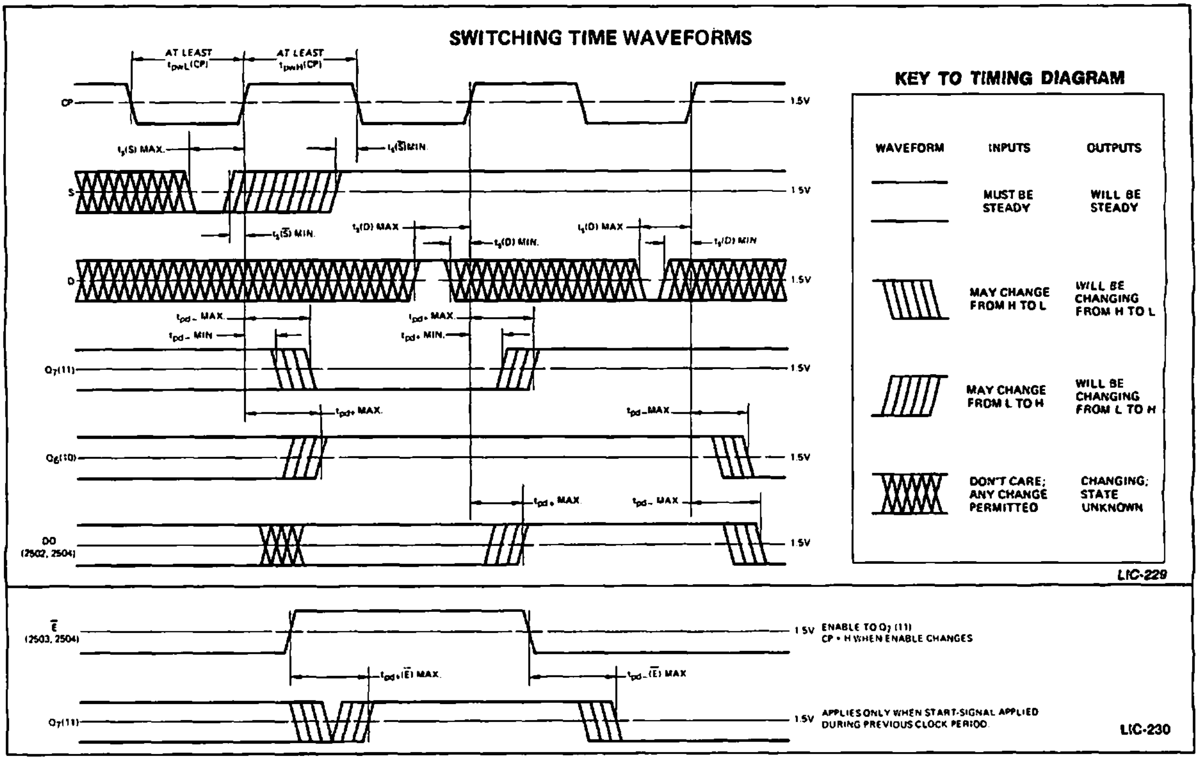
Am2502XC Am2503XC Am2504XC T_A = 0°C to +75°C V_{CC} = 5.0V ±5%
Am2502XM Am2503XM Am2504XM T_A = –55°C to +125°C V_{CC} = 5.0V ±10%

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = –0.48mA V_{IN} = V_{IH} or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage (Note 2)	V_{CC} = MIN., I_{OL} = 9.6mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	CP, D, $\overline{S}$		–1.0	–1.6	mA
			$\overline{E}$		–1.5	–2.4	
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V	CP, D		6.0	40	μA
			E, $\overline{S}$		12.0	80	
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		–10	–25	–45	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	Am2502 XM		65	85	mA
			Am2502 XC		65	95	
			Am2503 XM		60	80	mA
			Am2503 XC		60	90	
			Am2504 XM		90	110	mA
			Am2504 XC		90	124	

Notes: 1. Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. V_{OL}(MAX.) = 0.4V with total device fanout of less than 50 TTL Unit Loads (80mA). Otherwise, V_{OL}(MAX.) = 0.45V.

Switching Characteristics (T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF)

Parameters	Description		Min.	Typ.	Max.	Units
t_{pd+}	Turn Off Delay CP to Output HIGH (except Q_{11}, $\overline{Q}_{11}$)		10	29	45	ns
t_{pd+}	Turn Off Delay CP to Q_{11} or $\overline{Q}_{11}$ HIGH		10	35	50	ns
t_{pd-}	Turn On Delay CP to Output LOW		10	27	40	ns
$t_s(D)$	Set-up Time Data Input		–10	4.0	10	ns
$t_s(S)$	Set-up Time Start Input		0	9.0	16	ns
$t_{pd+}(E)$	Turn Off Delay E to $Q_7(11)$ HIGH	(Am2503/Am2504)		15	23	ns
$t_{pd-}(E)$	Turn On Delay E to $Q_7(11)$ LOW	Cp = H, $\overline{S}$ = L		20	30	ns
$t_{pwL}(CP)$	Minimum LOW Clock Pulse Width			28	46	ns
$t_{pwH}(CP)$	Minimum HIGH Clock Pulse Width			12	20	ns
$f_{max.}$	Maximum Clock Frequency		15	25		MHz



DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output

FUNCTIONAL TERMS:

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL}.

CP The clock input of the register.

$\overline{CC}$ The conversion complete output. This output remains HIGH during a conversion and goes LOW when a conversion is complete.

D The serial data input of the register.

$\bar{E}$ The register enable. This input is used to expand the length of the register and when HIGH forces the Q_7(11) register output HIGH and inhibits conversion. When not used for expansion the enable is held at a LOW logic level (Ground).

Q_7(11) The true output of the MSB of the register.

$\overline{Q}_7$(11) The complement output of the MSB of the register.

Q_i i = 7(11) to 0 The outputs of the register.

$\bar{S}$ The start input. If the start input is held LOW for at least a clock period the register will be reset to Q_7(11) LOW and all the remaining outputs HIGH. A start pulse that is LOW for a shorter period of time can be used if it meets the set-up time requirements of the $\bar{S}$ input.

DO The serial data output. (The D input delayed one bit).

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

SWITCHING TERMS: (Measured at the 1.5V logic level).

t_{pd-} The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition.

t_{pd+} The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition.

$t_{pd-}(\bar{E})$ The propagation delay from the Enable signal HIGH-LOW transition to the Q_7(11) output signal HIGH-LOW transition.

$t_{pd+}(\bar{E})$ The propagation delay from the Enable signal LOW-HIGH transition to Q_7(11) output signal LOW-HIGH transition.

t_s(D) Set-up time required for the logic level to be present at the data input prior to the clock transition from LOW to HIGH in order for the register to respond. The data input should remain steady between t_s max. and t_s min. before the clock.

$t_s(\bar{S})$ Set-up time required for a LOW level to be present at the $\bar{S}$ input prior to the clock transition from LOW to HIGH in order for the register to be reset, or time required for a HIGH level to be present on S before the HIGH to LOW clock transition to prevent resetting.

t_{pw}(CP) The minimum clock pulse width (LOW or HIGH) required for proper register operation.

Am2502/3 TRUTH TABLE

Time	Inputs			Outputs									
t_n	D	$\overline{S}$	$\overline{E}$	D_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	L	X	L	H	H	H	H	H	H	H	H
2	D_6	H	L	D_7	D_7	L	H	H	H	H	H	H	H
3	D_5	H	L	D_6	D_7	D_6	L	H	H	H	H	H	H
4	D_4	H	L	D_5	D_7	D_6	D_5	L	H	H	H	H	H
5	D_3	H	L	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H
6	D_2	H	L	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H
7	D_1	H	L	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H
8	Q_0	H	L	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H
9	X	H	L	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
10	X	X	L	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change

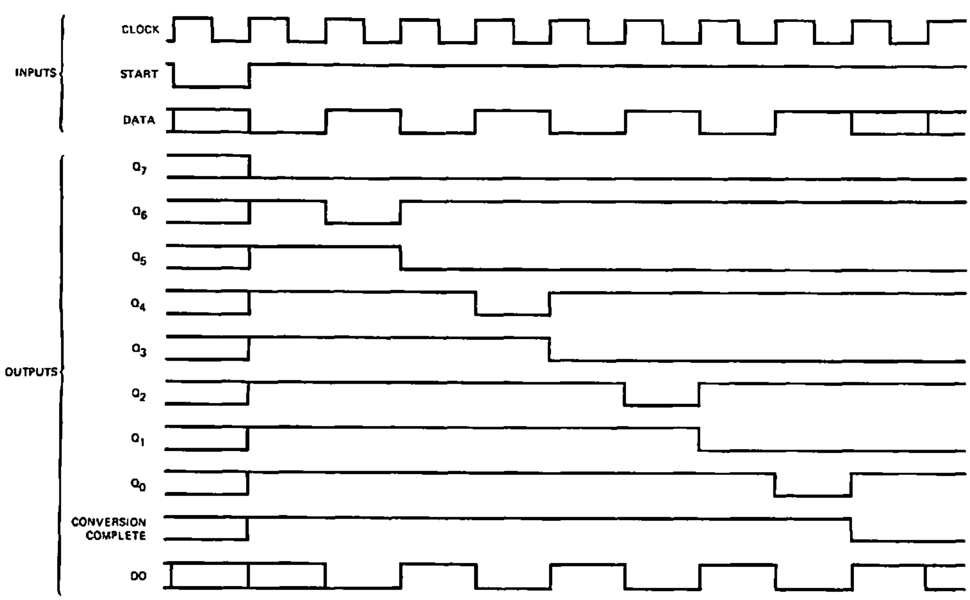
Note: Truth Table for Am2504 is extended to include 12 outputs.

USER NOTES FOR A/D CONVERSION

1. The register can be used with either current switches that require a low voltage level to turn the switch on, or current switches that require a high voltage level to turn the current switch on. If current switches are used which turn on with a low logic level the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If current switches are used that turn on with a high logic level then the digital output is active HIGH; a logic "1" is represented as a high voltage level.
2. For a maximum digital error of ±½LSB the comparator must be biased. If current switches that require a high voltage level to turn on are used, the comparator should be biased +½LSB and if the current switches require a high logic level to turn on then the comparator must be biased −½LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion. Additional data input gating should be used to eliminate the possibility of false BCD codes.
4. The register can be used to perform 2's complement conversion by offsetting the comparator ½ full range +½ LSB and using the complement of the MSB Q_7 (Q_{11}) as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the START input the OR function of $\overline{CC}$ and the appropriate register output.

3

Am2502/3 TIMING CHART



LIC-231

Am2502/3 LOADING RULES (IN UNIT LOADS)

Input/Output	Pin No.'s	Input Unit Load LOW	Input Unit Load HIGH	Fanout Output HIGH	Fanout Output LOW
$\overline{E}$ (2503)	1	1.5	2	–	–
DO (2502)	1	–	–	12	6
$\overline{CC}$	2	–	–	12	6
Q_0	3	–	–	12	6
Q_1	4	–	–	12	6
Q_2	5	–	–	12	6
Q_3	6	–	–	12	6
D	7	1	1	–	–
GND	8	–	–	–	–
CP	9	1	1	–	–
$\overline{S}$	10	1	2	–	–
Q_4	11	–	–	12	6
Q_5	12	–	–	12	6
Q_6	13	–	–	12	6
Q_7	14	–	–	12	6
$\overline{Q}_7$	15	–	–	12	6
V_{CC}	16	–	–	–	–

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	Equivalent Input Unit Load LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Am2504 LOADING RULES (IN UNIT LOADS)

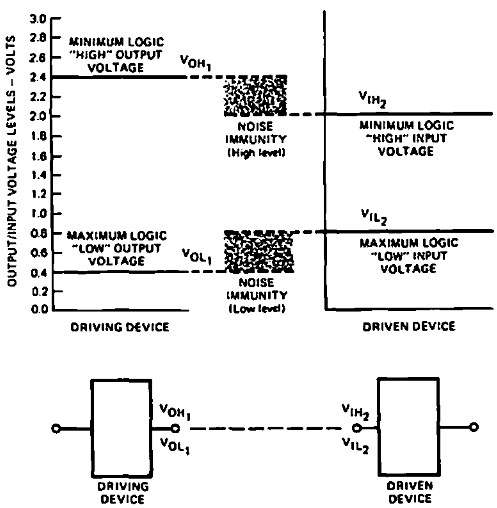
Input/Output	Pin No.'s	Input Unit Load LOW	Input Unit Load HIGH	Fanout Output HIGH	Fanout Output LOW
$\overline{E}$	1	1.5	2	–	–
DO	2	–	–	12	6
$\overline{CC}$	3	–	–	12	6
Q_0	4	–	–	12	6
Q_1	5	–	–	12	6
Q_2	6	–	–	12	6
Q_3	7	–	–	12	6
Q_4	8	–	–	12	6
Q_5	9	–	–	12	6
NC	10	–	–	–	–
D	11	1	1	–	–
GND	12	–	–	–	–
CP	13	1	1	–	–
$\overline{S}$	14	1	2	–	–
NC	15	–	–	–	–
Q_6	16	–	–	12	6
Q_7	17	–	–	12	6
Q_8	18	–	–	12	6
Q_9	19	–	–	12	6
Q_{10}	20	–	–	12	6
Q_{11}	21	–	–	12	6
NC	22	–	–	–	–
$\overline{Q}_{11}$	23	–	–	12	6
V_{CC}	24	–	–	–	–

A Standard TTL Unit Load is defined as 40μA measured at 2.4V HIGH and −1.6mA measured at 0.4V LOW.

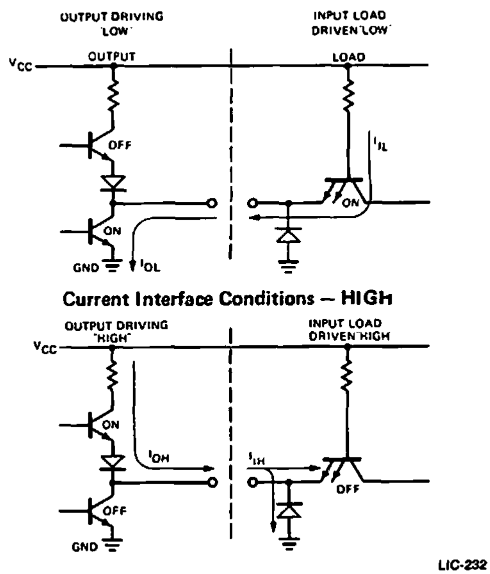
NC = No Connection

INPUT/OUTPUT INTERFACE CONDITIONS

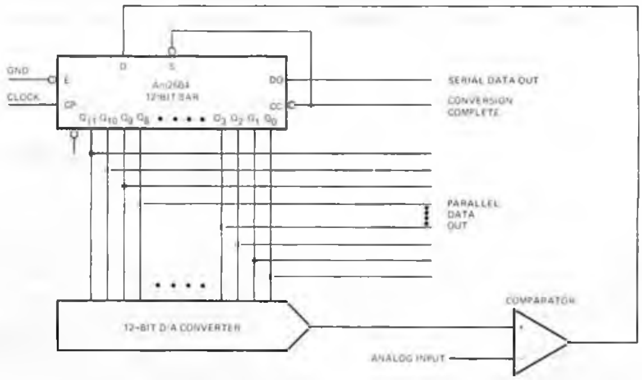
Voltage Interface Conditions – LOW & HIGH



Current Interface Conditions – LOW



Am2502/3/4 APPLICATION
Continuous Conversion Analog-to-Digital Converter



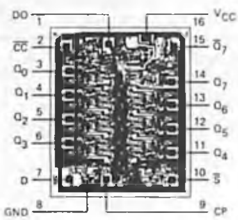
This shows how the Am2502/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a very high-speed continuous conversion Analog-to-Digital converter. Conversion time is limited mainly by the speed of the D/A converter and comparator with typical conversion rates of 100,000 conversions per second.

LIC-233

3

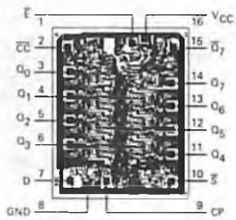
Metallization and Pad Layout

Am2502



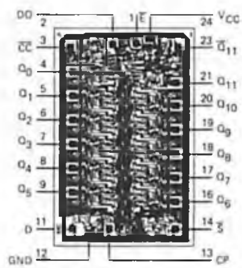
DIE SIZE 0.087" X 0.105"

Am2503



DIE SIZE 0.087" X 0.105"

Am2504



DIE SIZE 0.087" X 0.135"

Am25L02/25L03/25L04

Low-Power, Eight-Bit/Twelve-Bit Successive Approximation Registers

Distinctive Characteristics

- Contains all the storage and control for successive approximation A-to-D converters.
- Can be operated in START-STOP or continuous conversion mode.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Can be used as serial-to-parallel converter or ring counters.

FUNCTIONAL DESCRIPTION

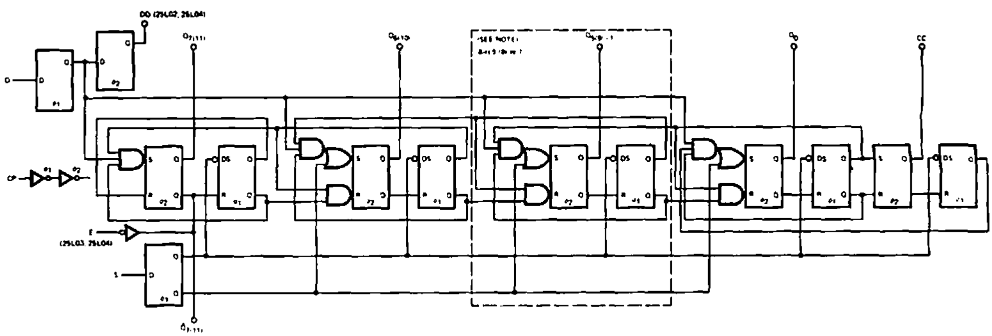
The Am25L02, Am25L03 and Am25L04 are 8-bit and 12-bit TTL Successive Approximation Registers. The registers contain all the digital control and storage necessary for successive approximation analog-to-digital conversion. They can also be used in digital systems as the control and storage element in recursive digital routines.

The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the Am25L02 and Am25L04 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state $Q_7(11)$ LOW, (Note 2) and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. The $\overline{S}$ signal should not be brought back HIGH until after the clock LOW-to-HIGH transition in order to guarantee correct resetting. After the clock has gone HIGH resetting the register, the $\overline{S}$ signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the $Q_7(11)$ register bit and the $Q_6(10)$ register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the $Q_6(10)$ register bit and $Q_5(9)$ is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q_0, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

In order to allow complementary conversion the complementary output of the most significant register bit is made available. An active LOW enable input, $\overline{E}$, on the Am25L03 and Am25L04 allows devices to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs together and connecting the $\overline{CC}$ output of one device to the $\overline{E}$ input of the next less significant device. When the Start signal resets the register, the E signal goes HIGH, forcing the $Q_7(11)$ bit HIGH and inhibiting the device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used the $\overline{E}$ input should be held at a LOW logic level (Ground). For continuous conversion the $\overline{CC}$ output is connected to the $\overline{S}$ input so that the device automatically restarts at the end of a conversion. If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the $\overline{CC}$ signal to indicate the end of conversion.

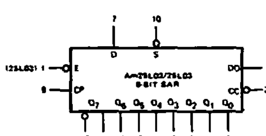
LOGIC DIAGRAMS



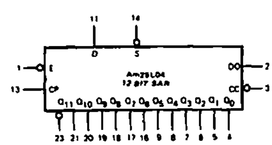
Notes: 1. Cell logic is repeated for register stages. Q_5 to Q_1 Am25L02/3, Q_9 to Q_1 Am25L04.
2. Numbers in parentheses are for Am25L04.

LIC-234

LOGIC SYMBOLS



LIC-235

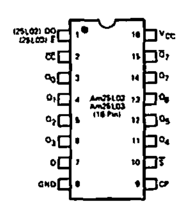


LIC-236

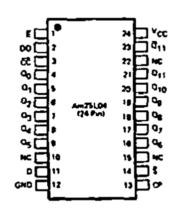
V_{CC} = Pin 16
GND = Pin 8

V_{CC} = Pin 24
GND = Pin 12
NC = Pins 10, 15 22

CONNECTION DIAGRAMS
Top Views



LIC-237



Note: Pin 1 is marked for orientation.

LIC-238

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	–0.5V to +7V
DC Voltage Applied to Outputs for High Output State	–0.5V to $+V_{CC}$ max.
DC Input Voltage	–0.5V to +5.5V
Output Current, Into Outputs	30mA
DC Input Current	–30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25L02XC	Am25L03XC	Am25L04XC	$T_A = 0°C$ to $+75°C$	$V_{CC} = 5.0V \pm 5\%$
Am25L02XM	Am25L03XM	Am25L04XM	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = –0.4mA V_{IN} = V_{IH} or V_{IL}			2.4	3.6		Volts
V_{OL}	Output LOW Voltage (Note 2)	V_{CC} = MIN., I_{OL} = 4.92mA V_{IN} = V_{IH} or V_{IL}				0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.7	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3V		CP,D,$\overline{S}$		–0.25	–0.4	mA
				$\overline{E}$		–0.4	–0.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V		CP, D		2.0	20	μA
				$\overline{E}$, $\overline{S}$		4.0	40	
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V			4.0	15	35	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	Am25L02	XM		25	33	mA
				XC		25	35	
			Am25L03	XM		22	31	mA
				XC		22	33	
			Am25L04	XM		30	42	mA
				XC		30	45	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. V_{OL}(MAX) = 0.3V with total device fanout of less than 90 Low Power TTL Unit Loads (36mA), otherwise, V_{OL}(MAX) = 0.35V.

Switching Characteristics (T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF)

Parameters	Description		Min.	Typ.	Max.	Units
t_{pd+}	Turn Off Delay CP to Output HIGH (except Q_{11}, $\overline{Q}_{11}$)		20	75	110	ns
t_{pd+}	Turn Off Delay CP to Q_{11} or $\overline{Q}_{11}$ HIGH		30	100	140	ns
t_{pd-}	Turn On Delay CP to Output LOW		20	75	100	ns
t_s(D)	Set-up Time Data Input		–15	8.0	20	ns
t_s(S)	Set-up Time Start Input		0	20	25	ns
t_{pd+}(E)	Turn Off Delay E to Q_7(11) HIGH	(Am25L03/Am25L04) Cp = H, S = L		50	75	ns
t_{pd-}(E)	Turn On Delay E to Q_7(11) LOW			60	75	ns
t_{pwL}(CP)	Minimum LOW Clock Pulse Width			100	150	ns
t_{pwH}(CP)	Minimum HIGH Clock Pulse Width			70	100	ns
$f_{max.}$	Maximum Clock Frequency		3.5	5.0		MHz

Am25L02/3 TRUTH TABLE

Time	Inputs			Outputs									
t_n	D	$\overline{S}$	$\overline{E}$	D_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	L	X	L	H	H	H	H	H	H	H	H
2	D_6	H	L	D_7	D_7	L	H	H	H	H	H	H	H
3	D_5	H	L	D_6	D_7	D_6	L	H	H	H	H	H	H
4	D_4	H	L	D_5	D_7	D_6	D_5	L	H	H	H	H	H
5	D_3	H	L	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H
6	D_2	H	L	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H
7	D_1	H	L	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H
8	D_0	H	L	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H
9	X	H	L	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
10	X	X	L	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

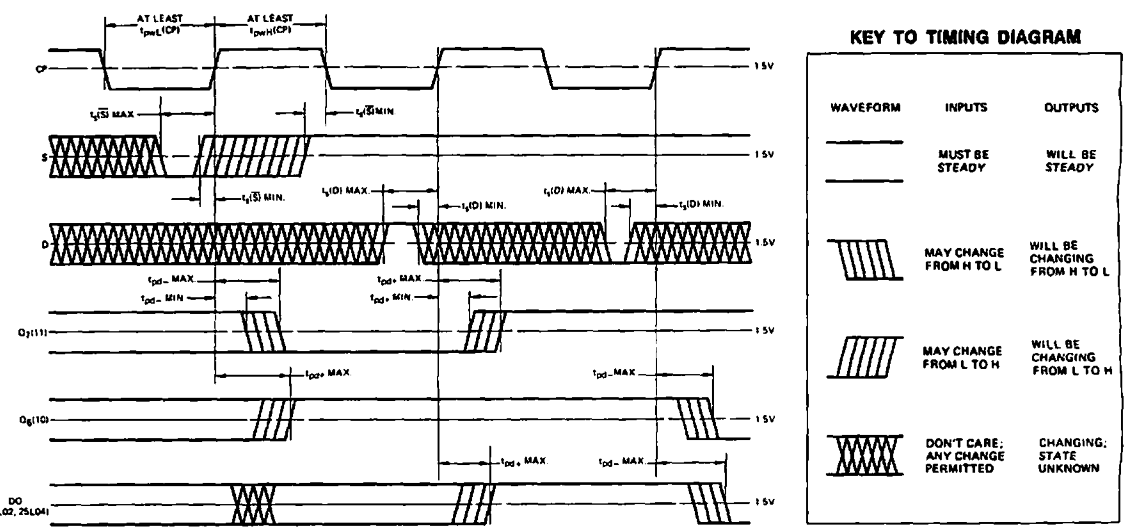
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change

Note: Truth Table for Am25L04 is extended to include 12 outputs.

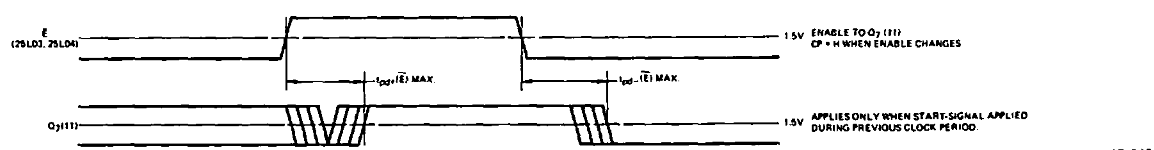
USER NOTES FOR A/D CONVERSION

1. The register can be used with either current switches that require a low voltage level to turn the switch on, or current switches that require a high voltage level to turn the current switch on. If current switches are used which turn on with a low logic level the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If current switches are used that turn on with a high logic level then the digital output is active HIGH; a logic "1" is represented as a high voltage level.
2. For a maximum digital error of ±½LSB the comparator must be biased. If current switches that require a low voltage level to turn on are used, the comparator should be biased +½LSB and if the current switches require a high logic level to turn on then the comparator must be biased –½LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion.
4. The register can be used to perform 2's complement conversion by offsetting the comparator ½ full range +½ LSB and using the complement of the MSB Q_7 (11) as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the START input the OR function of $\overline{CC}$ and the appropriate register output.

SWITCHING TIME WAVEFORMS

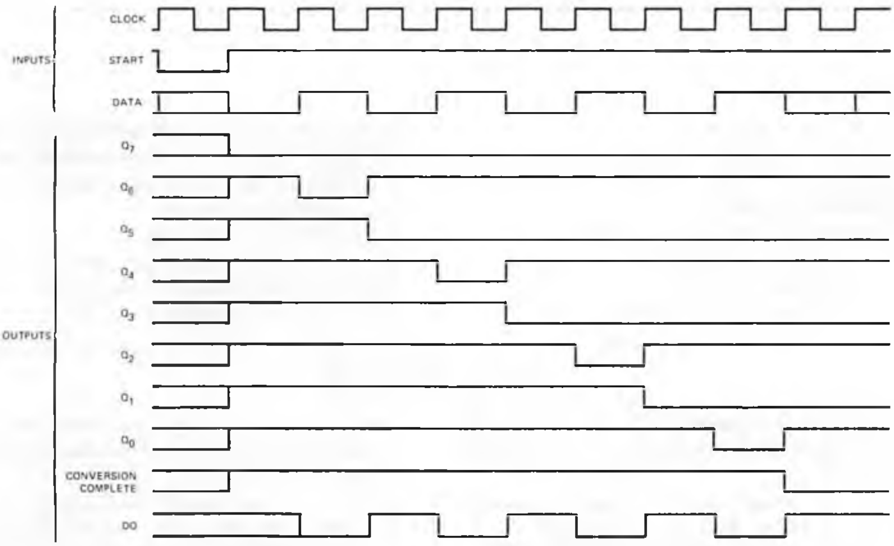


LIC-239



LIC-240

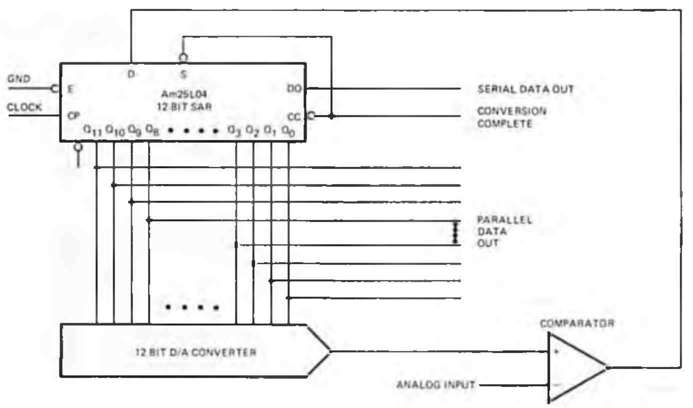
Am25L02/3 TIMING CHART



LIC-241

Am25L02/3/4 APPLICATION

Continuous Conversion Analog-to-Digital Converter

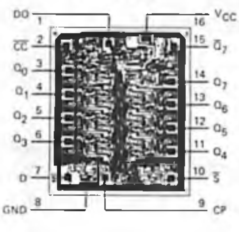


LIC-242

This shows how the Am25L02/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a very high-speed continuous conversion Analog-to-Digital converter. Conversion time is limited mainly by the speed of the D/A converter and comparator with typical conversion rates of 300,000 conversions per second. The comparator can be the Am111 precision comparator, or Am106 high-speed comparator.

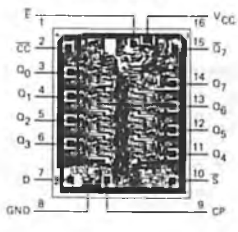
Metallization and Pad Layout

Am25L02



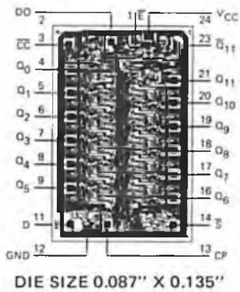
DIE SIZE 0.087" X 0.105"

Am25L03



DIE SIZE 0.087" X 0.105"

Am25L04



DIE SIZE 0.087" X 0.135"

Am6070

Companding D-to-A Converter for Control Systems

Distinctive Characteristics

- Tested to μ-255 companding law
- Absolute accuracy specified – includes all errors over temperature range
- Settling time 300ns typical
- Ideal for multiplexed PCM, audio, and 8-bit μ-P systems
- Output dynamic range of 72 dB
- 12-bit accuracy and resolution around zero
- Sign plus 12-bit range with sign plus 7-bit coding
- Improved pin-for-pin replacement for DAC-76
- Microprocessor controlled operations
- Multiplying operation
- Negligible output noise
- Monotonicity guaranteed over entire dynamic range
- Wide output voltage compliance
- Low power consumption

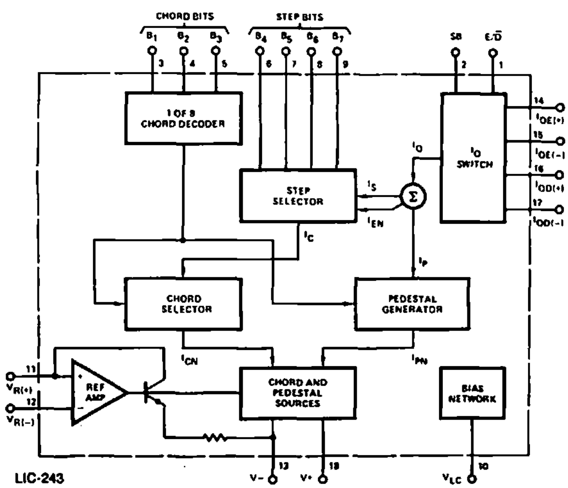
GENERAL DESCRIPTION

The Am6070 monolithic companding D/A converter achieves a 72dB dynamic range which is equivalent to that achieved by a 12-bit converter.

The transfer function of the Am6070 complies with the Bell system μ-255 companding law, and consists of 15 linear segments or chords. A particular chord is identified with the sign bit input, (SB) and three chord select input bits. Each chord contains 16 uniformly spaced linear steps which are determined by four step select input bits. Accuracy and monotonicity are assured by the internal circuit design and are guaranteed over the full temperature range.

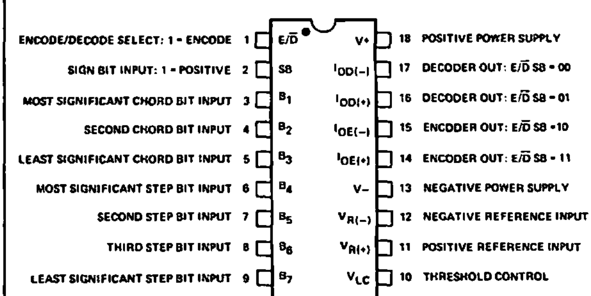
Applications for the Am6070 include digital audio recording, servo-motor controls, electromechanical positioning, voice synthesis, secure communications, microprocessor controlled sound and voice systems, log sweep generators and various data acquisition systems.

FUNCTIONAL BLOCK DIAGRAM



LIC-243

CONNECTION DIAGRAM
Am6070



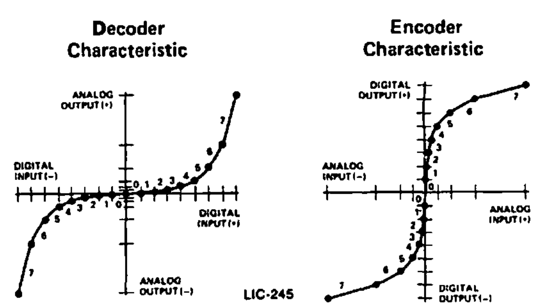
Top View
Pin 1 is marked for orientation.

LIC-244

ORDERING INFORMATION

Part Number	Temperature	Accuracy
Am6070ADM	−55°C to +125°C	±1/2 step
Am6070DM	−55°C to +125°C	±1 step
Am6070ADC	0°C to +70°C	±1/2 step
Am6070DC	0°C to +70°C	±1 step

SIMPLIFIED CONVERSION TRANSFER FUNCTIONS



LIC-245

MAXIMUM RATINGS above which useful life may be impaired

V+ Supply to V− Supply	36V	Operating Temperature	
V_{LC} Swing	V− plus 8V to V+	MIL Grade	−55°C to +125°C
Output Voltage Swing	V− plus 8V to V− plus 36V	COM'L Grade	0°C to +70°C
Reference Inputs	V− to V+	Storage Temperature	−65°C to +150°C
Reference Input Differential Voltage	±18V	Power Dissipation $T_A \leq 100°C$	500mW
Reference Input Current	1.25mA	For $T_A > 100°C$ derate at	10mW/°C
Logic Inputs	V− plus 8V to V− plus 36V	Lead Soldering Temperature	300°C (60 sec)

GUARANTEED FUNCTIONAL SPECIFICATIONS

Resolution	±128 Steps
Monotonicity	For both groups of 128 steps and over full operating temperature range
Dynamic Range	72 dB, (20 log $(I_{7,15}/I_{0,1})$)

ELECTRICAL CHARACTERISTICS

These specifications apply for V+ = +15V, V− = −15V, I_{REF} = 528μA, 0°C ≤ T_A ≤ +70°C, for the commercial grade, −55°C ≤ T_A ≤ +125C, for the military grade, and for all 4 outputs unless otherwise specified.

Parameter	Description	Test Conditions	Am6070ADM / Am6070ADC Min.	Typ.	Max.	Am6070DM / Am6070DC Min.	Typ.	Max.	Units
t_s	Settling Time	To within ±1/2 step at T_A = 25°C output switched from I_{ZS} to I_{FS}		300	500		300	500	ns
	Chord Endpoint Accuracy	Guaranteed by output current error specified below.			±1/2			±1	Step
	Step Nonlinearity				±1/2			±1	Step
$I_{FS(D)}$	Full Scale Current Deviation				±1/2			±1	
$I_{FS(E)}$	From Ideal				±1/2			±1	
ΔI_O	Output Current Error	V_{REF} = 10.000V R_{REF+} = 18.94kΩ R_{REF-} = 20kΩ −5.0V ≤ V_{OUT} ≤ +18V Error referred to nominal values in Table 1.			±1/2			±1	Step
$I_{O(+)}-I_{O(-)}$	Full Scale Symmetry Error	V_{REF} = 10.000V R_{REF+} = 18.94kΩ R_{REF} = 20kΩ −5.0V ≤ V_{OUT} ≤ +18V Error referred to nominal values in Table 1		1/40 1/40	1/8 1/8		1/20 1/20	1/4 1/4	Step Step
I_{EN}	Encode Current	Additional output Encode/Decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	Step
I_{ZS}	Zero Scale Current	Measured at selected output with 000 0000 input		1/40	1/4		1/20	1/2	Step
ΔI_{FS}	Full Scale Drift	Operating temperature range		±1/20	±1/4		±1/10	±1/2	Step
V_{OC}	Output Voltage Compliance	Full scale current change ≤1/2 step	−5.0		+18	−5.0		+18	Volts
I_{DIS}	Disable Current	Output leakage Output disabled by E/$\overline{D}$ and SB		5.0	50		5.0	50	nA
I_{FSR}	Output Current Range		0	2.0	4.2	0	2.0	4.2	mA
V_{IL}	Logic Input Levels — Logic "0"	V_{LC} = 0V			0.8			0.8	Volts
V_{IH}	Logic Input Levels — Logic "1"		2.0			2.0			Volts
I_{IN}	Logic Input Current	V_{IN} = −5.0V to +18V			40			40	μA
V_{IS}	Logic Input Swing	V− = −15V	−5.0		+18	−5.0		+18	Volts
$I_{B\ REF-}$	Reference Bias Current			−1.0	−4.0		−1.0	−4.0	μA
di/dt	Reference Input Slew Rate		0.12	0.25		0.12	0.25		mA/μs
$PSSI_{FS+}$ $PSSI_{FS-}$	Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	V+ = 4.5 to 18V, V− = −15V V− = 10.8 + −18V, V+ = 15V	±1/20 ±1/10	±1/2 ±1/2		±1/20 ±1/10	±1/2 ±1/2		Step Step
I+ I−	Power Supply Current	V+ = +5.0 to +15V, V− = −15V I_{FS} = 2.0mA		2.7 −6.7	4.0 −8.8		2.7 −6.7	4.0 −8.8	mA
P_D	Power Dissipation	V− = −15V, V_{OUT}=0, I_{FS} = 2.0mA; V+ = 5.0V		114	152		114	152	mW
		V− = −15V, V_{OUT}=0, I_{FS} = 2.0mA; V+ = +15V		141	192		141	192	mW

ELECTRICAL CHARACTERISTICS (Cont.)

TABLE 1
NOMINAL DECODER OUTPUT CURRENT LEVELS IN μA

STEP	CHORD 0	1	2	3	4	5	6	7
0	.000	8.250	24.750	57.750	123.75	255.75	519.75	1047.75
1	.500	9.250	26.750	61.750	131.75	271.75	551.75	1111.75
2	1.000	10.250	28.750	65.750	139.75	287.75	583.75	1175.75
3	1.500	11.250	30.750	69.750	147.75	303.75	615.75	1239.75
4	2.000	12.250	32.750	73.750	155.75	319.75	647.75	1303.75
5	2.500	13.250	34.750	77.750	163.75	335.75	679.75	1367.75
6	3.000	14.250	36.750	81.750	171.75	351.75	711.75	1431.75
7	3.500	15.250	38.750	85.750	179.75	367.75	743.75	1495.75
8	4.000	16.250	40.750	89.750	187.75	383.75	775.75	1559.75
9	4.500	17.250	42.750	93.750	195.75	399.75	807.75	1623.75
10	5.000	18.250	44.750	97.750	203.75	415.75	839.75	1687.75
11	5.500	19.250	46.750	101.750	211.75	431.75	871.75	1751.75
12	6.000	20.250	48.750	105.750	219.75	447.75	903.75	1815.75
13	6.500	21.250	50.750	109.750	227.75	463.75	935.75	1879.75
14	7.000	22.250	52.750	113.750	235.75	479.75	967.75	1943.75
15	7.500	23.250	54.750	117.750	243.75	495.75	999.75	2007.75
STEP SIZE	.5	1	2	4	8	16	32	64

TABLE 2
IDEAL DECODER OUTPUT VALUES EXPRESSED IN dB DOWN FROM FULL SCALE

STEP	CHORD 0	1	2	3	4	5	6	7
0	–	−47.73	−38.18	−30.82	−24.20	−17.90	−11.74	−5.65
1	−72.07	−46.73	−37.51	−30.24	−23.66	−17.37	−11.22	−5.13
2	−66.05	−45.84	−36.88	−29.70	−23.15	−16.87	−10.73	−4.65
3	−62.53	−45.03	−36.30	−29.18	−22.66	−16.40	−10.27	−4.19
4	−60.03	−44.29	−35.75	−28.70	−22.21	−15.96	−9.83	−3.75
5	−58.10	−43.61	−35.24	−28.24	−21.77	−15.53	−9.41	−3.33
6	−56.51	−42.98	−34.75	−27.80	−21.36	−15.13	−9.01	−2.94
7	−55.17	−42.39	−34.29	−27.39	−20.96	−14.74	−8.63	−2.56
8	−54.01	−41.84	−33.85	−26.99	−20.58	−14.37	−8.26	−2.19
9	−52.99	−41.32	−33.44	−26.61	−20.22	−14.02	−7.91	−1.84
10	−52.07	−40.83	−33.04	−26.25	−19.87	−13.68	−7.57	−1.51
11	−51.25	−40.37	−32.66	−25.90	−19.54	−13.35	−7.25	−1.18
12	−50.49	−39.93	−32.29	−25.57	−19.22	−13.03	−6.93	−0.87
13	−49.80	−39.51	−31.95	−25.25	−18.91	−12.73	−6.63	−0.57
14	−49.15	−39.11	−31.61	−24.94	−18.61	−12.43	−6.34	−0.28
15	−48.55	−38.73	−31.29	−24.63	−18.32	−12.15	−6.06	0.00

THEORY OF OPERATION

Functional Description

The Am6070 is an 8-bit, nonlinear, digital-to-analog converter with high impedance current outputs. The output current value is proportional to the product of the digital inputs and the input reference current. The full scale output current, I_{FS}, is specified by the input binary code 111 1111, and is a linear function of the reference current, I_{REF}. There are two operating modes, encode and decode, which are controlled by the *Encode/Decode*, ($E/\overline{D}$), input signal. A logic 1 applied to the $E/\overline{D}$ input places the Am6072 in the encode mode and current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output, depending on the state of the Sign Bit (SB) input. A logic 0 at the $E/\overline{D}$ input places the Am6070 in the decode mode.

The transfer characteristic is a piece-wise linear approximation to the Bell System μ-225 logarithmic law which can be written as follows:

$$Y = 0.18\ell n\,(1 + \mu\ |X|)\ \mathrm{sgn}\ (X)$$

where: X = analog signal level normalized to unity (encoder input or decoder output)
Y = digital signal level normalized to unity (encoder output or decoder input)
$\mu = 255$

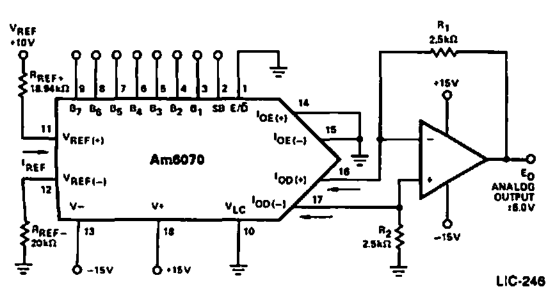
The current flows from the external circuit into one of four possible analog outputs determined by the SB and $E/\overline{D}$ inputs. The output current transfer function can be represented by a total of 16 segments or chords addressable through the SB input and three chord select bits. Each chord can be further divided into 16 steps, all of the same size. The step size changes from one chord to another, with the smallest step of 0.5μA found in the first chord near zero output current, and the largest step of 64μA found in the last chord near full scale output current. This nonlinear feature provides exceptional accuracy for small signal levels near zero output current. The accuracy for signal amplitudes corresponding to chord 0 is equivalent to that of a 12-bit linear, binary D/A converter. However, the ratio (in dB) between the chord endpoint current, (Step 15), and the current which corresponds to the preceding step, (Step 14), is maintained at about 0.3dB over most of the dynamic range. The difference between the ratios of full scale current to chord endpoint currents of adjacent chords is similarly maintained at approximately 6dB over most of the dynamic range. Resulting signal-to-quantizing distortions due to non-uniform quantizing levels maintain an acceptably low value over a 40dB range of input speech signals. Note that the 72dB output dynamic range for the Am6070 corresponds to the dynamic range of a sign plus 12-bit linear, binary D/A converter.

In order to achieve a smoother transition between adjacent chords, the step size between these chord end points is equal to 1.5 times the step size of the lower chord. Monotonic operation is guaranteed by the internal device design over the entire output dynamic range by specifying and maintaining the chord end points and step size deviations within the allowable limits.

Operating Modes

The basic converter function is conversion of digital input data into a corresponding analog current signal, i.e., the basic function is digital-to-analog decoding. The basic decoder connection for a sign plus 7-bit input configuration is shown in Figure 1. The corresponding dynamic range is 72dB, and input-output characteristics conform to the standard decoder transfer function with output current values specified in Table 1. The $E/\overline{D}$ input enables switching between the encode, $I_{OE(+)}$ or $I_{OE(-)}$, and the decode, $I_{OD(+)}$ or $I_{OD(-)}$, outputs. A typical encode/decode test circuit is shown in Figure 2. This circuit is used for output current measurements. When the $E/\overline{D}$ input is high, (a logic 1), the converter will assume the encode operating mode and the output current will flow into one of the I_{OE} outputs (as determined by the SB input). When operating in the encode mode as shown in Figure 3, an offset current equal to a half step in each chord is required to obtain the correct encoder transfer characteristic. Since the size of this step varies from one chord to another, it cannot easily be added externally. As indicated in the block diagram this required half step of encode current,

3

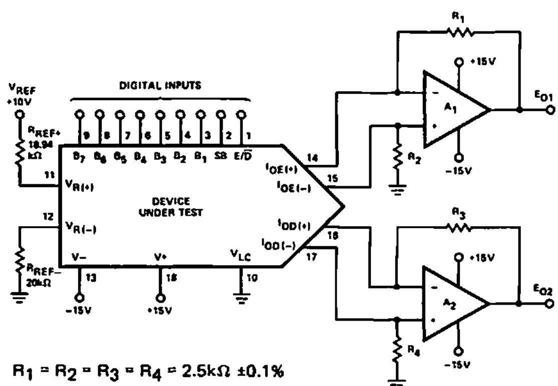


$I_{REF} = V_{REF}/R_{REF}$

IDEAL VALUES: $I_{REF} = 528\mu A$, $I_{FS} = 2007.75\mu A$

	$E/\overline{D}$	SB	B_1	B_2	B_3	B_4	B_5	B_6	B_7	E_O
POSITIVE FULL SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012V
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0V
(−) ZERO SCALE	0	0	0	0	0	0	0	0	0	0V
(−) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	−0.0012V
NEGATIVE FULL SCALE	0	0	1	1	1	1	1	1	1	−5.019V

Figure 1. Detailed Decoder Connections.



$R_1 = R_2 = R_3 = R_4 = 2.5k\Omega \pm 0.1\%$

LINE SELECTION TABLE

TEST GROUP	$E/\overline{D}$	SB	OUTPUT MEASUREMENT	
1	1	1	$I_{OE}(+)$	(E_{O1}/R_1)
2	1	0	$I_{OE}(-)$	(E_{O1}/R_2)
3	0	1	$I_{OD}(+)$	(E_{O2}/R_3)
4	0	0	$I_{OD}(-)$	(E_{O2}/R_4)

Figure 2. Output Current DC Test Circuit.

I_{EN}, is automatically added to the I_{OE} output through the internal chip design. This additional current will, for example, make the ideal full scale current in the encode mode larger than the same current in the decode mode by 32μA. Similarly, the current levels in the first chord near the origin will be offset by 0.25μA, which will bring the ideal encode current value for step 0 on chord 0 to $\pm$0.25μA with respect to the corresponding decode current value of 0.0μA. This additional encode half step of current can be used for extension of the output dynamic range from 72dB to 78dB, when the converter is performing only the decode function. The corresponding decoder connection utilizes the E/$\overline{D}$ input as a ninth digital input and has the outputs $I_{OD(+)}$ and $I_{OE(+)}$ and the outputs $I_{OD(-)}$ and $I_{OE(-)}$ tied together, respectively.

When encoding or compression of an analog signal is required, the Am6070 can be used together with a Successive Approximation Register (SAR), comparator, and additional SSI logic elements to perform the A/D data conversion, as shown in Figure 3. The encoder transfer function, shown on page 1, characterizes this A/D converter system. The first task of this system is to determine the polarity of the incoming analog signal and to generate a corresponding SB input value. When the proper Start, $\overline{S}$, and Conversion Complete, $\overline{CC}$, signal levels are set, the first clock pulse sets the MSB output of the SAR, Am2502, to a logic 0 and sets all other parallel digital outputs to logic 1 levels. At the same time, the flip-flop is triggered, and its output provides the E/$\overline{D}$ input with a logic 0 level. No current flows into the I_{OE} outputs. This disconnects the converter from the comparator inputs, and the incoming analog signal can be compared with the ground applied to the opposite comparator input. The resulting comparator output is fed to the Am2502 serial data input, D, through an exclusive-or gate. At the same time, the second input to the same exclusive-or gate is held at a logic 0 level by the additional successive approximation logic shown in Figure 3. This exclusive-or gate inverts the comparator's outputs whenever a negative signal polarity is detected. This maintains the proper output current coding, i.e., all ones for full scale and all zeros for zero scale.

The second clock pulse changes the E/$\overline{D}$ input back to a logic 1 level because the $\overline{CC}$ signal changed. It also clocks the D input signal of the Am2502 to its MSB output, and transfers it to the SB input of the Am6070. Depending upon the SB input level, current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output of the Am6070.

Nine total clock pulses are required to obtain a digital binary representation of the incoming analog signal at the eight Am2502 digital outputs. The resulting Am6070 analog output signal is compared with the analog input signal *after* each of the nine successive clock pulses. The analog signal should not be allowed to change its value during the data conversion time. In high speed systems, fast changes of the analog signals at the A/D system input are usually prevented by using sample and hold circuitry.

Additional Considerations and Recommendations

In Figure 1, an optional operational amplifier converts the Am6070 output current to a bipolar voltage output. When the SB input is a logic 1, sink current appears at the amplifier's negative input, and the amplifier acts as a current to voltage converter, yielding a positive voltage output. With the SB value at a logic 0, sink current appears at the amplifier's positive input. The amplifier behaves as a voltage follower, and the true current outputs will swing below ground with essentially no change in output current. The SB input steers current into the appropriate (+) or (−) output of the Am6070. The resulting operational amplifier's output in Figure 1 should ideally be symmetrical with resistors R1 and R2 matched.

In Figure 2, two operational amplifiers measure the currents of each of the four Am6070 analog outputs. Resistor tolerances of 0.1% give 0.1% output measurement error (approximately 2μA at full scale). The input offset currents of the A1 and A2 devices also increase output measurement error and this error is most significant near zero scale. The Am101A and 308 devices, for example, may be used for A1 and A2 since their maximum offset currents, which would add directly to the measurement error, are only 10nA and 1nA, respectively. The input offset voltages of the A1 and A2 devices, with output resistor values of

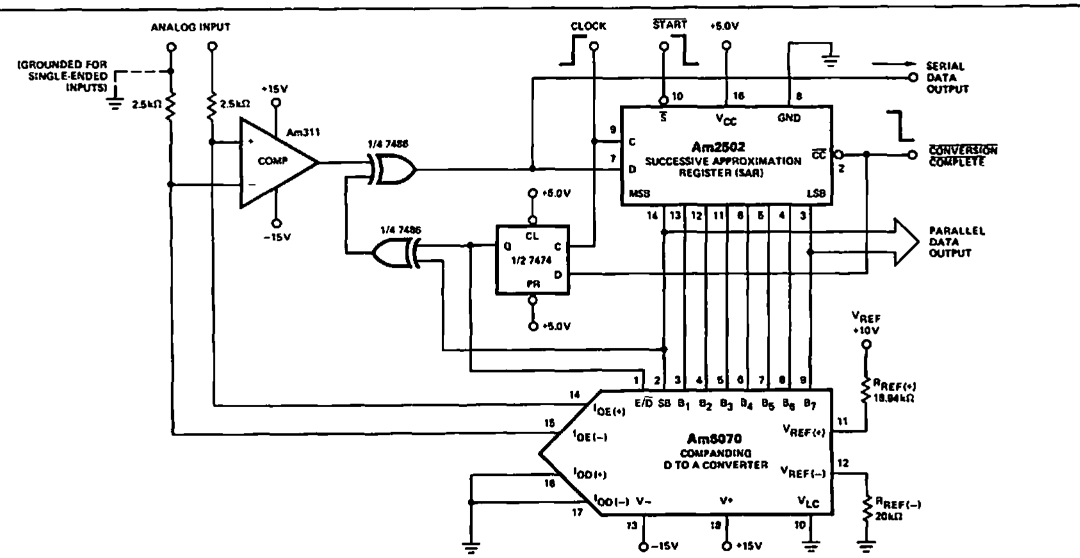


Figure 3. Detailed Encoder Connections.

LIC-248

2.5kΩ, also contribute to the output measurement error by a factor of 400nA for every mV of offset at the A1 and A2 outputs. Therefore, to minimize error, the offset voltages of A1 and A2 should be nulled.

The recommended operating range for the reference current I_{REF} is from 0.1mA to 1.0mA. The full scale output current, I_{FS}, is a linear function of the reference current, and may be calculated from the equation $I_{FS} = 3.8\ I_{REF}$. This tight relationship between I_{REF} and I_{FS} alleviates the requirement for trimming the I_{REF} current if the R_{REF} resistors values are within ±1% of the calculated value. Lower values of I_{REF} will reduce the negative power supply current, (I−), and will increase the reference amplifier negative common mode input voltage range.

The ideal value for the reference current $I_{REF} = V_{REF}/R_{REF}$ is 528μA. The corresponding ideal full scale decode and encode current values are 2007.75μA and 2039.75μA, respectively. A percentage change from the ideal I_{REF} value produced by changes in V_{REF} or R_{REF} values produces the same percentage change in decode and encode output current values. The positive voltage supply, V+, may be used, with certain precautions, for the positive reference voltage V_{REF}. In this case, the reference resistor $R_{REF(+)}$ should be split into two resistors and their junction bypassed to ground with a capacitor of 0.01μF. The total resistor value should provide the reference current I_{REF} = 528μA. The resistor $R_{REF(-)}$ value should be approximately equal to the $R_{REF(+)}$ value in order to compensate for the errors caused by the reference amplifier's input offset current.

An alternative to the positive reference voltage applications shown in Figures 1, 2 and 3 is the application of a negative voltage to the $V_{R(-)}$ terminal through the resistor $R_{REF(-)}$ with the $R_{REF(+)}$ resistor tied to ground. The advantage of this arrangement is the presence of very high impedance at the $V_{R(-)}$ terminal while the reference current flows from ground through $R_{REF(+)}$ into the $V_{R(+)}$ terminal.

The Am6070 has a wide output voltage compliance suitable for driving a variety of loads. With I_{REF} = 528μA and V− = −15V, positive voltage compliance is +18V and negative voltage compliance is −5.0V. For other values of I_{REF} and V−, the negative voltage compliance, $V_{OC(-)}$, may be calculated as follows:

$$V_{OC(-)} = (V-) + (2 \cdot I_{REF} \cdot 1.5k\Omega) + 8.4V.$$

The following table contains $V_{OC(-)}$ values for some specific V−, I_{REF}, and I_{FS} values.

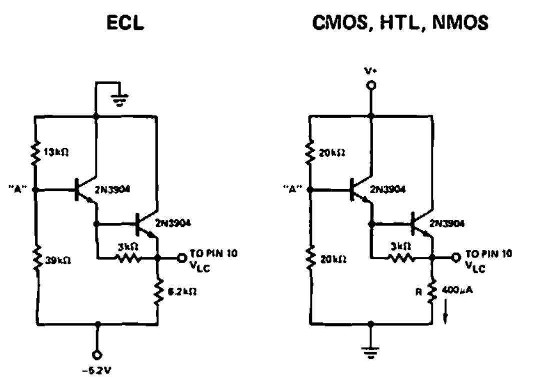
Negative Output Voltage Compliance $V_{OC(-)}$

V− \ I_{REF} (I_{FS})	264μA (1mA)	528μA (2mA)	1056μA (4mA)
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

The V_{LC} input can accommodate various logic input switching threshold voltages allowing the Am6070 to interface with various logic families. This input should be placed at a potential which is 1.4V below the desired logic input switching threshold. Two external discrete circuits which provide this function for non-TTL driven inputs are shown in Figure 4. For TTL-driven logic inputs, the V_{LC} input should be grounded. If negative voltages are applied at the digital logic inputs, they must have a value which is more positive than the sum of the chosen V− value and +10V.

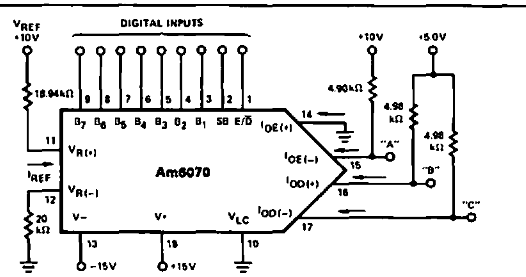
With a V− value chosen between −15V and −11V, the $V_{OC(-)}$, the input reference common mode voltage range, and the logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− value chosen.

With a V+ value chosen between +5V and +15V, the reference amplifier common mode positive voltage range and the V_{LC} input values are reduced by an amount equivalent to the difference between +15V and the V+ value chosen.



(See Notes 2 and 3)

Figure 4. Interfacing Circuits for ECL, CMOS, HTL, and NMOS Logic Inputs. LIC-249



INPUT CODE (E/D̄, SB, B_1, . . . , B_7)	OUTPUT VOLTAGE (V) "A"	"B"	"C"	DIFF
10 111 1111	0	N/A	N/A	N/A
10 110 1111	+5.02			
10 000 0000	+10.00			
01 111 1111	N/A	−5.00	+5.00	−10.00
01 110 1111		+0.02	+5.00	−4.98
01 000 0000		+5.00	+5.00	0
00 000 0000		+5.00	+5.00	0
00 110 1111		+5.00	+0.02	+4.98
00 111 1111		+5.00	−5.00	+10.00

Figure 5. Resistive Output Connections. LIC-250

Notes: 2. Set the voltage "A" to the desired logic input switching threshold.
3. Allowable range of logic threshold is typically −5V to +13.5V when operating the companding DAC on ±15V supplies.

ADDITIONAL DECODE OUTPUT CURRENT TABLES

Table 3
Normalized Decoder Output (Sign Bit Excluded)

Step (S)	Chord (C)	0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
Step Size		2	4	8	16	32	64	128	256

The normalized decode current, ($I_{C,S}$), is calculated using:
$I_{C,S} = 2(2^C(S + 16.5) - 16.5)$
where C = chord number; S = step number. The ideal decode current, (I_{OD}), in μA is calculated using:
$I_{OD} = (I_{C,S}/I_{7,15(norm.)}) \cdot I_{FS}\ (\mu A)$
where $I_{C,S}$ is the corresponding normalized current. To obtain normalized encode current values the corresponding normalized half-step value should be added to all entries in Table 3.

Table 4
Normalized Encode Level (Sign Bit Excluded)

STEP	CHORD	0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
Step Size		2	4	8	16	32	64	128	256

$I_{C,S} = 2[2^C (S+17) - 16.5]$
C = chord no. (0 through 7)
S = step no. (0 through 15)

ADDITIONAL DECODE OUTPUT CURRENT TABLES (Cont.)

Table 5
Decoder Step Size Summary

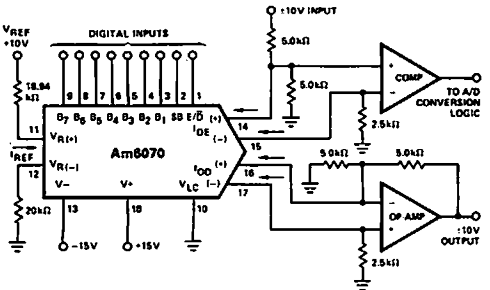
Chord	Step Size Normalized to Full Scale	Step Size in μA with 2007.75μA FS	Step Size as a % of Full Scale	Step Size in dB at Chord Endpoints	Step Size as a % of Reading at Chord Endpoints	Resolution & Accuracy of Equivalent Binary DAC
0	2	0.5	0.025%	0.60	6.67%	Sign + 12 Bits
1	4	1.0	0.05%	0.38	4.30%	Sign + 11 Bits
2	8	2.0	0.1%	0.32	3.65%	Sign + 10 Bits
3	16	4.0	0.2%	0.31	3.40%	Sign + 9 Bits
4	32	8.0	0.4%	0.29	3.28%	Sign + 8 Bits
5	64	16.0	0.8%	0.28	3.23%	Sign + 7 Bits
6	128	32.0	1.6%	0.28	3.20%	Sign + 6 Bits
7	256	64.0	3.2%	0.28	3.19%	Sign + 5 Bits

Table 6
Decoder Chord Size Summary

Chord	Chord Endpoints Normalized to Full Scale	Chord Endpoints in μA with 2007.75μA FS	Chord Endpoints as a % of Full Scale	Chord Endpoints in dB Down from Full Scale
0	30	7.5	0.37%	–48.55
1	93	23.25	1.16%	–38.73
2	219	54.75	2.73%	–31.29
3	471	117.75	5.86%	–24.63
4	975	243.75	12.1%	–18.32
5	1983	495.75	24.7%	–12.15
6	3999	999.75	49.8%	–6.06
7	8031	2007.75	100%	0

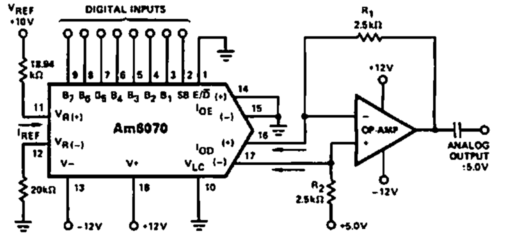
BASIC CIRCUIT CONNECTIONS

±10V RANGE ENCODER/DECODER CONNECTIONS



LIC-251

COMPLIANCE EXTENSION USING AC COUPLED OUTPUT



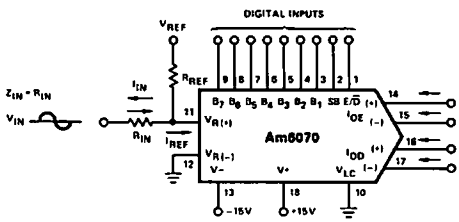
IDEAL VALUES:

$I_{REF} = 528\mu A$

$I_{FS} = 2007.75\mu A$

LIC-252

LOW INPUT IMPEDANCE CONNECTION

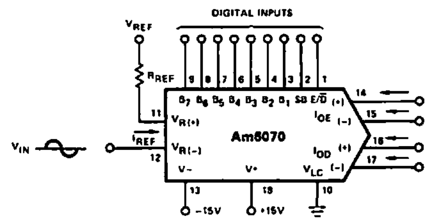


$I_{REF} = V_{IN}/R_{IN} + V_{REF}/R_{REF}$

$I_{FS} \approx 4 \cdot I_{REF}$

LIC-253

HIGH INPUT IMPEDANCE CONNECTION

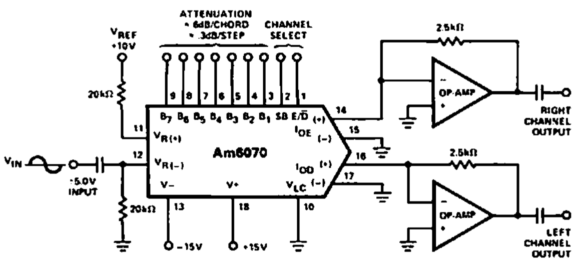


$I_{REF} = (V_{REF} - V_{IN})/R_{REF}$

$I_{FS} \approx 4 \cdot I_{REF}$

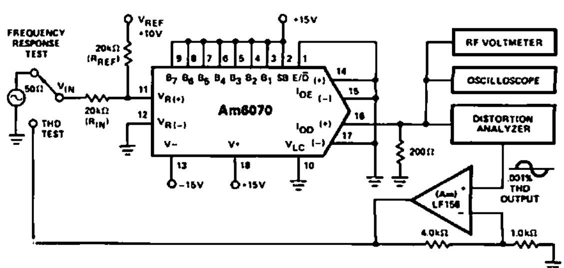
LIC-254

LOGARITHMIC DIGITAL GAIN CONTROL (Notes 4 & 5)



LIC-255

REFERENCE AMPLIFIER DYNAMIC TEST CIRCUIT



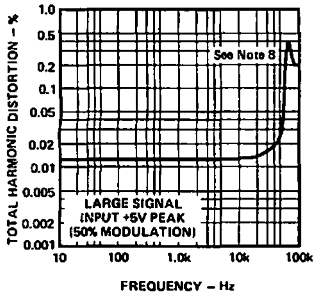
LIC-256

Notes: 4. Low distortion outputs are provided over a 72dB range.

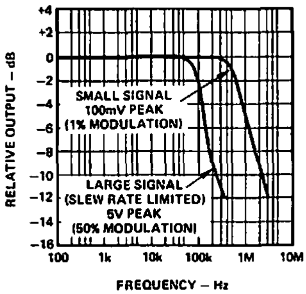
5. Up to 4 channels of output may be selected by E/$\overline{D}$ and SB logic inputs.

TYPICAL PERFORMANCE CURVES

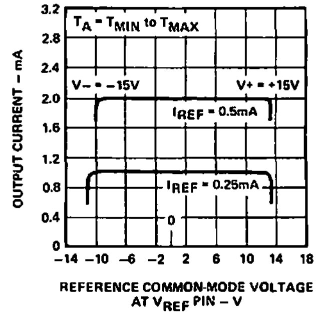
Reference Amplifier Total Harmonic Distortion Versus Frequency (80kHz Filter) (Notes 6, 7, 8)



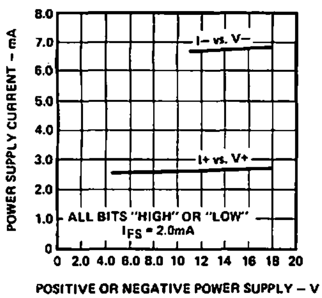
Reference Amplifier Input Frequency Response



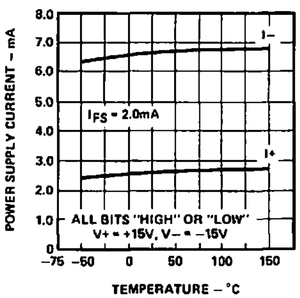
Reference Amplifier Input Common-Mode Range (Note 9)



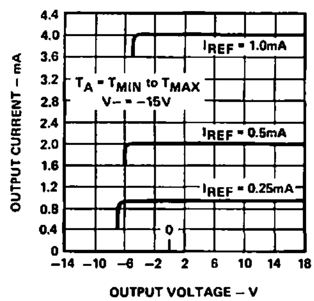
Power Supply Currents Versus Power Supply Voltages



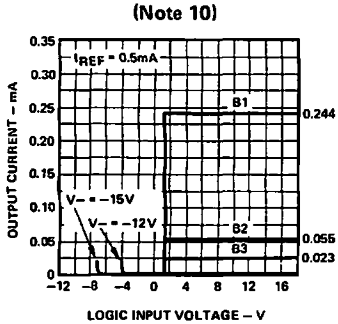
Power Supply Currents Versus Temperature



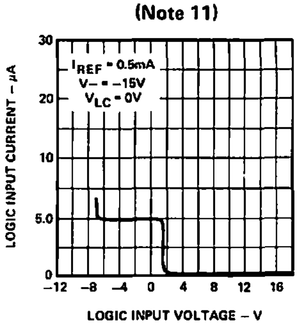
Output Current Versus Output Voltage (Output Voltage Compliance)



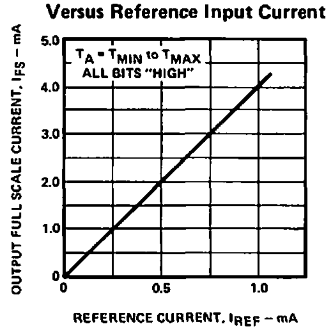
Bit Transfer Characteristics (Note 10)



Logic Input Current Versus Input Voltage and Logic Input Range (Note 11)



Output Full Scale Current Versus Reference Input Current



LIC-257

Notes:
6. THD is nearly independent of the logic input code.
7. Similar results are obtained for a high input impedance connection using $V_{R(-)}$ as an input.
8. Increased distortion above 50kHz is due to a slew rate limiting effect which determines the large signal bandwidth. For an input of ±2.5V peak (25% modulation), the bandwidth is 100kHz.
9. Positive common mode range is always (V+) –1.5V.
10. All bits are fully switched with less than a half step error at switching points which are guaranteed to lie between 0.8V and 2.0V over the operating temperature range.
11. The logic input voltage range is independent of the positive power supply and logic inputs may swing above the supply.

APPLICATIONS

The companding D/A converter is particularly suited for applications requiring a wide dynamic range.

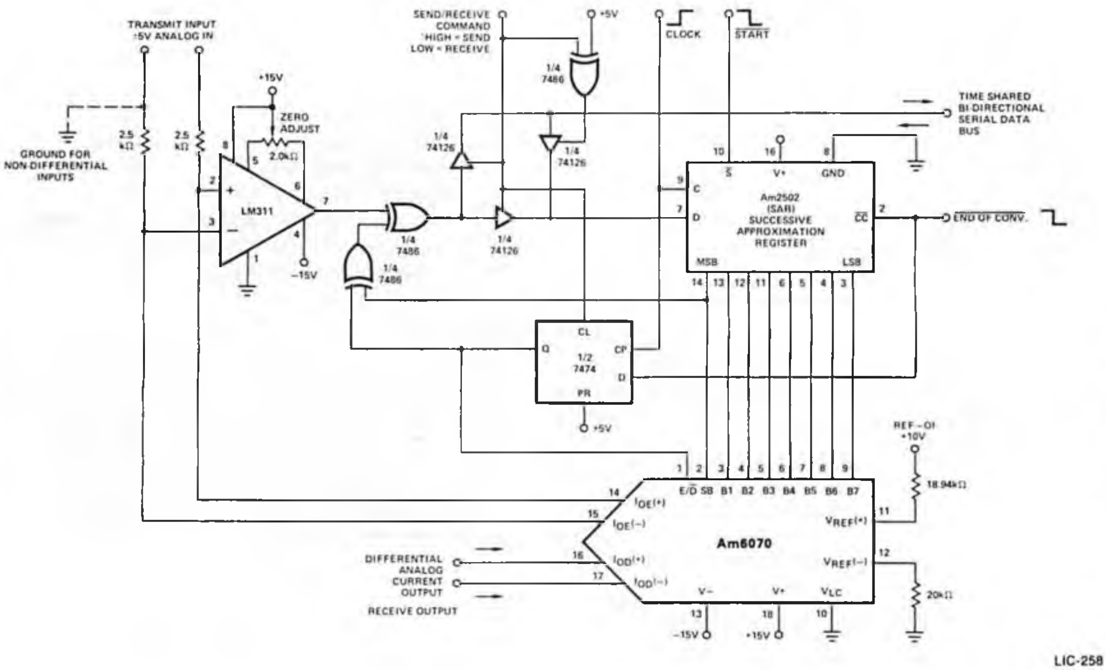
Systems requiring fine control resulting in a constant rate of change or set point controls are economically achieved using these devices.

Instrumentation, Control and μ-Processor based applications include:
- Digital data recording
- PCM telemetry systems
- Servo systems
- Function generation
- Data acquisition systems

Telecommunications applications include:
- PCM Codec telephone systems
- Intercom systems
- Military voice communication systems
- Radar systems
- Voice Encryption

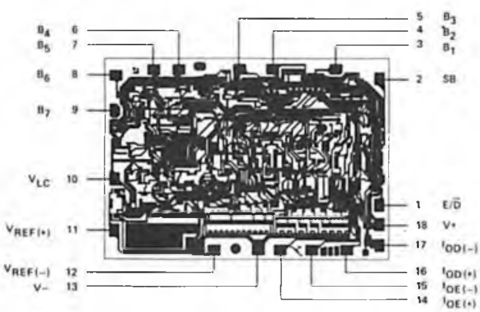
Audio Applications:
- Recording
- Multiplexing of analog signals
- Voice synthesis

SERIAL DATA TRANSCEIVING CONVERTER
(1/2 OF SYSTEM SHOWN)



Notes:
1. Complementary send/receive commands are required for the two ends.
2. START must be held low for one clock cycle to begin a send or receive cycle.
3. The SAR is used as a serial-in/parallel out register in the receive mode.
4. CLOCK and START may be connected in parallel at both ends.
5. Conversion is completed in 9 clock cycles.
6. Receive output is available for one full clock cycle.

Metallization and Pad Layout



80 X 114 Mils

Am6071

Companding D-to-A Converter for Control Systems

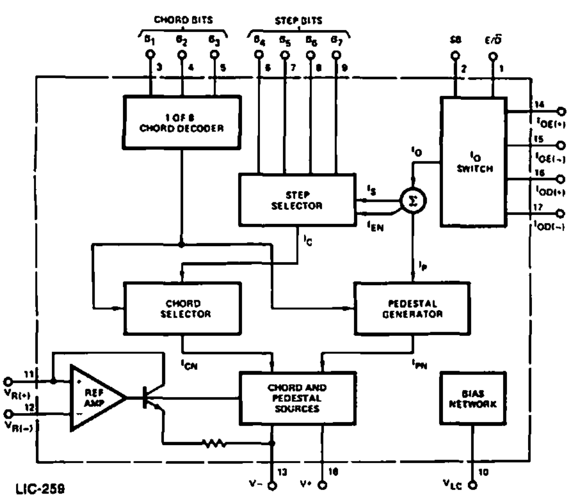
Distinctive Characteristics

- Tested to A-law tracking specification
- Absolute accuracy specified – includes all errors over temperature range
- Settling time 300ns typical
- Ideal for multiplexed PCM, audio, and 8-bit μ-P systems
- Output dynamic range of 62 dB
- Microprocessor controlled operations
- Multiplying operation
- Negligible output noise
- Monotonicity guaranteed over entire dynamic range
- Wide output voltage compliance
- Low power consumption

GENERAL DESCRIPTION

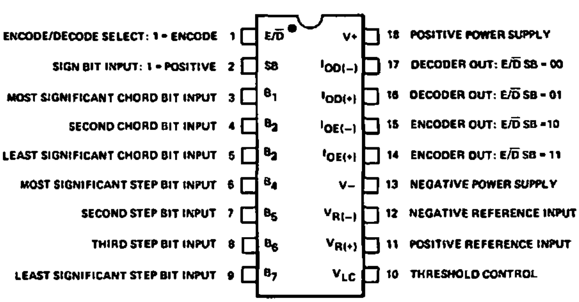
The Am6071 is a monolithic 8-bit, companding digital-to-analog (D/A) converter with true current outputs and large output voltage compliance for fast driving a variety of loads. The transfer function of the Am6071 consists of 13 linear segments or chords. A particular chord is identified with the sign bit input, (SB) and three chord select input bits. Each chord contains 16 uniformly spaced linear steps which are determined by four step select input bits. The resulting dynamic range achieved with this format is 62 dB. Accuracy and monotonicity are assured by the internal circuit design and are guaranteed over the full temperature range. The Am6071 is tested to the A-law tracking specification. Applications for the Am6071 include digital audio recording, servo motor controls, electro-mechanical positioning, voice synthesis, secure communications, microprocessor controlled sound and voice systems, log sweep generators, and various data acquisition systems.

FUNCTIONAL BLOCK DIAGRAM



LIC-259

CONNECTION DIAGRAM
Am6072



Top View

Pin 1 is marked for orientation.

LIC-260

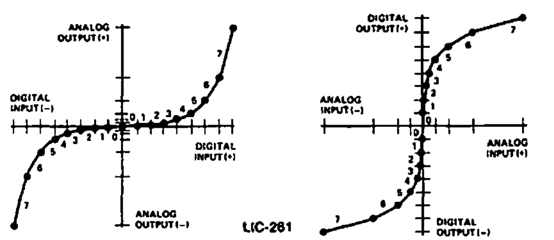
ORDERING INFORMATION

Part Number	Temperature	Accuracy
Am6071ADM	–55°C to +125°C	±1/2 step
Am6071DM	–55°C to +125°C	±1 step
Am6071ADC	0°C to +70°C	±1/2 step
Am6071DC	0°C to +70°C	±1 step

SIMPLIFIED CONVERSION TRANSFER FUNCTIONS

Decoder Characteristic

Encoder Characteristic



LIC-261

MAXIMUM RATINGS above which useful life may be impaired

V+ Supply to V− Supply	36V	Operating Temperature	
V_{LC} Swing	V− plus 8V to V+	MIL Grade	−55°C to +125°C
Output Voltage Swing	V− plus 8V to V− plus 36V	COM'L Grade	0°C to +70°C
Reference Inputs	V− to V+	Storage Temperature	−65°C to +150°C
Reference Input Differential Voltage	±18V	Power Dissipation $T_A \leq 100°C$	500mW
Reference Input Current	1.25mA	For $T_A > 100°C$ derate at	10mW/°C
Logic Inputs	V− plus 8V to V− plus 36V	Lead Soldering Temperature	300°C (60 sec)

GUARANTEED FUNCTIONAL SPECIFICATIONS

Resolution	±128 Steps
Monotonicity	For both groups of 128 steps and over full operating temperature range
Dynamic Range	62dB, (20 log ($I_{7,15}/I_{0,1}$))

ELECTRICAL CHARACTERISTICS

These specifications apply for V+ = +15V, V− = −15V, I_{REF} = 512μA, 0°C ≤ T_A ≤ +70°C, for the commercial grade, −55°C ≤ T_A ≤ +125C, for the military grade, and for all 4 outputs unless otherwise specified.

Parameter	Description	Test Conditions	Am6071ADM Am6071ADC Min.	Typ.	Max.	Am6071DM Am6071DC Min.	Typ.	Max.	Units
t_s	Settling Time	To within ±1/2 step at T_A = 25°C output switched from I_{ZS} to I_{FS}		300	500		300	500	ns
	Chord Endpoint Accuracy	Guaranteed by output current error specified below.			±1/2			±1	Step
	Step Nonlinearity				±1/2			±1	Step
$I_{FS(D)}$ $I_{FS(E)}$	Full Scale Current Deviation From Ideal				±1/2			±1	
					±1/2			±1	
ΔI_O	Output Current Error	V_{REF} = 10.000V R_{REF+} = 19.53k R_{REF-} = 20kΩ −5.0V ≤ V_{OUT} ≤ +18V Error referred to nominal values in Table 1.			±1/2			±1	Step
$I_{O(+)}-I_{O(-)}$	Full Scale Symmetry Error	V_{REF} = 10.000V R_{REF-} = 19.53k R_{REF} = 20kΩ −5.0V ≤ V_{OUT} ≤ +18V Error referred to nominal values in Table 1		1/40 1/40	1/8 1/8		1/20 1/20	1/4 1/4	Step Step
I_{EN}	Encode Current	Additional output Encode/Decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	Step
I_{ZS}	Zero Scale Current	Measured at selected output with 000 0000 input		1/40	1/4		1/20	1/2	Step
ΔI_{FS}	Full Scale Drift	Operating temperature range		±1/20	±1/4		±1/10	±1/2	Step
V_{OC}	Output Voltage Compliance	Full scale current change ≤1/2 step	−5.0		+18	−5.0		+18	Volts
I_{DIS}	Disable Current	Output leakage Output disabled by E/$\overline{D}$ and SB		5.0	50		5.0	50	nA
I_{FSR}	Output Current Range		0	2.0	4.2	0	2.0	4.2	mA
V_{IL}	Logic Input Levels, Logic "0"	V_{LC} = 0V			0.8			0.8	Volts
V_{IH}	Logic Input Levels, Logic "1"		2.0			2.0			Volts
I_{IN}	Logic Input Current	V_{IN} = −5.0V to +18V			40			40	μA
V_{IS}	Logic Input Swing	V− = −15V	−5.0		+18	−5.0		+18	Volts
$I_{B\ REF-}$	Reference Bias Current			−1.0	−4.0		−1.0	−4.0	μA
di/dt	Reference Input Slew Rate		0.12	0.25		0.12	0.25		mA/μs
$PSSI_{FS+}$ $PSSI_{FS-}$	Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	V+ = 4.5 to 18V, V− = −15V V− = −10.8 to −18V, V+ = 15V	±1/20 ±1/10	±1/2 ±1/2		±1/20 ±1/10	±1/2 ±1/2		Step Step
I+ I−	Power Supply Current	V+ = +5.0 to +15V, V− = −15V I_{FS} = 2.0mA		2.7 −6.7	4.0 −8.8		2.7 −6.7	4.0 −8.8	mA
P_D	Power Dissipation	V− = −15V, V_{OUT} = 0, I_{FS} = 2.0mA; V+ = 5.0V		114	152		114	152	mW
		V− = −15V, V_{OUT} = 0, I_{FS} = 2.0mA; V+ = +15V		141	192		141	192	mW

3

ELECTRICAL CHARACTERISTICS (Cont.)

TABLE I
NOMINAL DECODER OUTPUT CURRENT LEVELS IN μA

STEP	CHORD							
	0	1	2	3	4	5	6	7
0	.500	16.500	33.000	66.000	132.00	264.00	528.00	1056.00
1	1.500	17.500	35.000	70.000	140.00	280.00	560.00	1120.00
2	2.500	18.500	37.000	74.000	148.00	296.00	592.00	1184.00
3	3.500	19.500	39.000	78.000	156.00	312.00	624.00	1248.00
4	4.500	20.500	41.000	82.000	164.00	328.00	656.00	1312.00
5	5.500	21.500	43.000	86.000	172.00	344.00	688.00	1376.00
6	6.500	22.500	45.000	90.000	180.00	360.00	720.00	1440.00
7	7.500	23.500	47.000	94.000	188.00	376.00	752.00	1504.00
8	8.500	24.500	49.000	98.000	196.00	392.00	784.00	1568.00
9	9.500	25.500	51.000	102.000	204.00	408.00	816.00	1632.00
10	10.500	26.500	53.000	106.000	212.00	424.00	848.00	1696.00
11	11.500	27.500	55.000	110.000	220.00	440.00	880.00	1760.00
12	12.500	28.500	57.000	114.000	228.00	456.00	912.00	1824.00
13	13.500	29.500	59.000	118.000	236.00	472.00	944.00	1888.00
14	14.500	30.500	61.000	122.000	244.00	488.00	976.00	1952.00
15	15.500	31.500	63.000	126.000	252.00	504.00	1008.00	2016.00
STEP SIZE	1	1	2	4	8	16	32	64

TABLE 2
IDEAL DECODER OUTPUT VALUES EXPRESSED IN dB DOWN FROM OVERLOAD LEVEL (+ 3dBmo)

STEP	CHORD							
	0	1	2	3	4	5	6	7
0	72.11	41.74	35.72	29.70	23.68	17.66	11.64	5.62
1	62.57	41.23	35.21	29.19	23.17	17.15	11.13	5.11
2	58.13	40.75	34.73	28.71	22.68	16.66	10.64	4.62
3	55.21	40.29	34.27	28.25	22.23	16.21	10.19	4.17
4	53.03	39.85	33.83	27.81	21.79	15.77	9.75	3.73
5	51.28	39.44	33.42	27.40	21.38	15.36	9.34	3.32
6	49.83	39.05	33.03	27.00	20.98	14.96	8.94	2.92
7	48.59	38.67	32.65	26.63	20.61	14.59	8.57	2.54
8	47.50	38.31	32.29	26.27	20.24	14.22	8.20	2.18
9	46.54	37.96	31.94	25.92	19.90	13.88	7.86	1.84
10	45.67	37.62	31.60	25.58	19.56	13.54	7.52	1.50
11	44.88	37.30	31.28	25.26	19.24	13.22	7.20	1.18
12	44.15	36.99	30.97	24.95	18.93	12.91	6.89	0.87
13	43.48	36.69	30.67	24.65	18.63	12.61	6.59	0.57
14	42.86	36.40	30.38	24.38	18.34	12.32	6.30	0.28
15	42.28	36.12	30.10	24.08	18.06	12.04	6.02	0.00

THEORY OF OPERATION

Functional Description

The Am6071 is an 8-bit, nonlinear, digital-to-analog converter with high impedance current outputs. The output current value is proportional to the product of the digital inputs and the input reference current. The full scale output current, I_{FS}, is specified by the input binary code 111 1111, and is a linear function of the reference current, I_{REF}. There are two operating modes, encode and decode, which are controlled by the Encode/Decode, ($E/\overline{D}$), input signal. A logic 1 applied to the $E/\overline{D}$ input places the Am6073 in the encode mode and current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output, depending on the state of the Sign Bit (SB) input. A logic 0 at the $E/\overline{D}$ input places the Am6073 in the decode mode.

The transfer characteristic is a piece-wise linear approximation to the CCITT A-87.6 logarithmic law which can be written as follows:

$$Y = 0.18\,(1 + \ln(A\,|X|))\ \mathrm{sgn}\,(X), \quad 1/A \leq |X| \leq 1$$
$$Y = 0.18\,(A\,|X|)\ \mathrm{sgn}\,(X), \quad 0 \leq |X| \leq 1/A$$

where: X = analog signal level normalized to unity (encoder input or decoder output)
Y = digital signal level normalized to unity (encoder output or decoder input)
A = 87.6

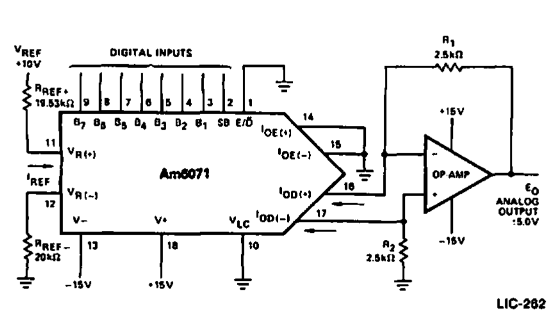
The current flows from the external circuit into one of four possible analog outputs determined by the SB and $E/\overline{D}$ inputs. The output current transfer function can be represented by a total of 16 segments or chords addressable through the SB input and three chord select bits. The two chords closest to the origin of the transfer function, chord 0 and chord 1, are made colinear and contiguous. The beginning of chord 0, specified by the input binary code 000 0000, is offset by $+0.5\mu A$. Each chord can be further divided into 16 steps, all of the same size. The step size changes from one chord to another, with the smallest step of $1.0\mu A$ found in the first two chords near zero output current, and the largest step of $64\mu A$ found in the last chord near full scale output current. This nonlinear feature provides exceptional accuracy for small signal levels. The accuracy for signal amplitudes corresponding to chords 0 and 1 is very close to that of an 11-bit linear, binary D/A converter. The ratio (in dB) between the chord endpoint current, (Step 15), and the current which corresponds to the preceding step, (Step 14), is maintained at about 0.3dB over the entire dynamic range, with the exception of chord 0. The difference between the ratios of full scale current to chord endpoint currents of adjacent chords is similarly maintained at 6dB over the entire dynamic range. Resulting signal-to-quantizing distortions due to non-uniform quantizing levels maintain an acceptably low value over a 40dB range of input speech signals. Note that the 62dB output dynamic range for the Am6071 is very close to the dynamic range of a sign plus 11-bit linear, binary D/A converter.

In order to achieve a smoother transition between adjacent chords, the step size between these chord end points is equal to 1.5 times the step size of the lower chord. Note that this does not apply to chord 0 and chord 1 where adjacent end points differ by only one step, because these two chords are colinear and have the same step sizes. Monotonic operation is guaranteed by the internal device design over the entire output dynamic range by specifying and maintaining the chord end points and step size deviations within the allowable limits.

3

Operating Modes

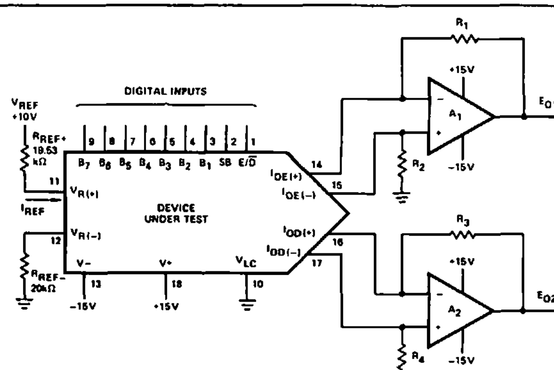
The basic converter function is conversion of digital input data into a corresponding analog current signal, i.e., the basic function is digital-to-analog decoding. The basic decoder connection for a sign plus 7-bit input configuration is shown in Figure 1. The corresponding dynamic range is 62dB, and input-output characteristics conform to the standard decoder transfer function with output current values specified in Table 1. The $E/\overline{D}$ input enables switching between the encode, $I_{OE(+)}$ or $I_{OE(-)}$, and the decode, $I_{OD(+)}$ or $I_{OD(-)}$, outputs. A typical encode/decode test circuit is shown in Figure 2. This circuit is used for output current measurements. When the $E/\overline{D}$ input is high, (a logic 1), the converter will assume the encode operating mode and the output current will flow into one of the I_{OE} outputs (as determined by the SB input). When operating in the encode mode as shown



$I_{REF} = V_{REF}/R_{REF}$
IDEAL VALUES: $I_{REF} = 512\mu A$, $I_{FS} = 2016\mu A$

	$E/\overline{D}$	SB	B_1	B_2	B_3	B_4	B_5	B_6	B_7	E_O
POSITIVE FULL SCALE	0	1	1	1	1	1	1	1	1	5.040V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.004V
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0.0012V
(−) ZERO SCALE	0	0	0	0	0	0	0	0	0	−0.0012V
(−) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	−0.004V
NEGATIVE FULL SCALE	0	0	1	1	1	1	1	1	1	−5.040V

Figure 1. Detailed Decoder Connections.



$R_1 = R_2 = R_3 = R_4 = 2.5k\Omega \pm 0.1\%$

LINE SELECTION TABLE

TEST GROUP	$E/\overline{D}$	SB	OUTPUT MEASUREMENT	
1	1	1	$I_{OE}(+)$	(E_{O1}/R_1)
2	1	0	$I_{OE}(-)$	(E_{O1}/R_2)
3	0	1	$I_{OD}(+)$	(E_{O2}/R_3)
4	0	0	$I_{OD}(-)$	(E_{O2}/R_4)

Figure 2. Output Current DC Test Circuit.

in Figure 3, an offset current equal to a half step in each chord is required to obtain the correct encoder transfer characteristic. Since the size of this step varies from one chord to another, it cannot easily be added externally. As indicated in the block diagram this required half step of encode current, I_{EN}, is automatically added to the I_{OE} output through the internal chip design. This additional current will, for example, make the ideal full scale current in the encode mode larger than the same current in the decode mode by 32μA. Similarly, the current levels in the first chord near the origin will be offset by 0.5μA, which will bring the ideal encode current value for step 0 on chord 0 to 1.0μA with respect to the corresponding decode current value of 0.5μA. This additional encode half step of current can be used for extension of the output dynamic range from 62dB to 66dB, when the converter is performing only the decode function. The corresponding decoder connection utilizes the $E/\overline{D}$ input as a ninth digital input and has the outputs $I_{OD(+)}$ and $I_{OE(+)}$ and the outputs $I_{OD(-)}$ and $I_{OE(-)}$ tied together, respectively.

When encoding or compression of an analog signal is required, the Am6071 can be used together with a Successive Approximation Register (SAR), comparator, and additional SSI logic elements to perform the A/D data conversion, as shown in Figure 3. The encoder transfer function, shown on page 1, characterizes this A/D converter system. The first task of this system is to determine the polarity of the incoming analog signal and to generate a corresponding SB input value. When the proper $\overline{\text{START}}$, ($\overline{\text{S}}$), and $\overline{\text{CONVERSION COMPLETE}}$, ($\overline{\text{CC}}$), signal levels are set, the first clock pulse sets the MSB output of the SAR, Am2502, to a logic 0 and sets all other parallel digital outputs to logic 1 levels. At the same time, the flip-flop is triggered, and its output provides the $E/\overline{D}$ input with a logic 0 level. No current flows into the I_{OE} outputs. This disconnects the converter from the comparator inputs, and the incoming analog signal can be compared with the ground applied to the opposite comparator input. The resulting comparator output is fed to the Am2502 serial data input, D, through an exclusive-or gate. At the same time, the second input to the same exclusive-or gate is held at a logic 0 level by the additional successive approximation logic shown in Figure 3. This exclusive-or gate inverts the comparator's outputs whenever a negative signal polarity is detected. This maintains the proper output current coding, i.e., all ones for full scale and all zeros for zero scale.

The second clock pulse changes the $E/\overline{D}$ input back to a logic 1 level because the $\overline{\text{CC}}$ signal changed. It also clocks the D input signal of the Am2502 to *its* MSB output, and transfers it to the SB input of the Am6071. Depending upon the SB input level, current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output of the Am6071.

Nine clock pulses are required to obtain a digital binary representation of the incoming analog signal at the eight Am2502 digital outputs. The resulting Am6071 analog output signal is compared with the analog input signal after each of the nine successive clock pulses. The analog signal should not be allowed to change its value during the data conversion time. In high speed systems, fast changes of the analog signals at the A/D system input are usually prevented by using sample and hold circuitry.

Additional Considerations and Recommendations

In Figure 1, an optional operational amplifier converts the Am6071 output current to a bipolar voltage output. When the SB input is a logic 1, sink current appears at the amplifier's negative input, and the amplifier acts as a current to voltage converter, yielding a positive voltage output. With the SB value at a logic 0, sink current appears at the amplifier's positive input. The amplifier behaves as a voltage follower, and the true current outputs will swing below ground with essentially no change in output current. The SB input steers current into the appropriate (+) or (−) output of the Am6071. The resulting operational amplifier's output in Figure 1 should ideally be symmetrical with resistors R1 and R2 matched.

In Figure 2, two operational amplifiers measure the currents of each of the four Am6071 analog outputs. Resistor tolerances of 0.1% give 0.1% output measurement error (approximately 2μA at full scale). The input offset currents of the A1 and A2 devices also increase output measurement error and this error is most significant near zero scale. The Am101A and 308 devices, for example, may be used for A1 and A2 since their maximum offset currents, which would add directly to the measurement error, are only 10nA and 1nA respectively. The input offset voltages of the A1 and A2 devices, with output resistor values of 2.5kΩ, also contribute to the output measurement error by a factor of 400nA for

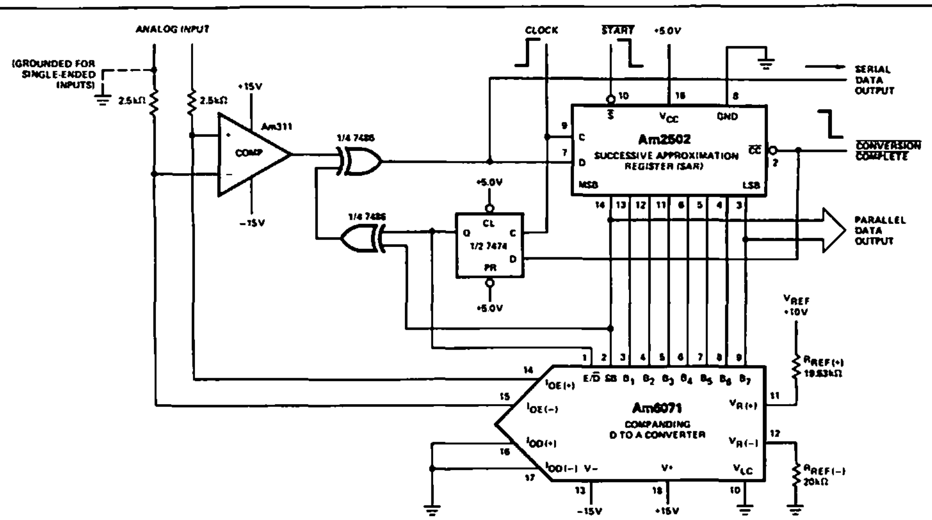


Figure 3. Detailed Encoder Connections.

LIC-264

every mV of offset. Therefore, to minimize error, the offset voltages of A1 and A2 should be nulled.

The recommended operating range for the reference current I_{REF} is from 0.1mA to 1.0mA. The full scale output current, I_{FS}, is a linear function of the reference current, and may be calculated from the equation $I_{FS} = 3.94\ I_{REF}$. This tight relationship between I_{REF} and I_{FS} alleviates the requirement for trimming the I_{REF} current if the R_{REF} resistor values are within ±1% of the calculated value. Lower values of I_{REF} will reduce the negative power supply current, (I−), and will increase the reference amplifier negative common mode input voltage range.

The ideal value for the reference current $I_{REF} = V_{REF}/R_{REF}$ is 512µA. The corresponding ideal full scale decode and encode current values are 2016µA and 2048µA, respectively. A percentage change from the ideal I_{REF} value produced by changes in V_{REF} or R_{REF} values produces the same percentage change in decode and encode output current values. The positive voltage supply, V+, may be used, with certain precautions, for the positive reference voltage V_{REF}. In this case, the reference resistor $R_{REF(+)}$ should be split into two resistors and their junction bypassed to ground with a capacitor of 0.01µF. The total resistor value should provide the reference current I_{REF} = 512µA. The resistor $R_{REF(-)}$ value should be approximately equal to the $R_{REF(+)}$ value in order to compensate for the errors caused by the reference amplifier's input offset current.

An alternative to the positive reference voltage applications shown in Figures 1, 2 and 3 is the application of a negative voltage to the $V_{R(-)}$ terminal through the resistor $R_{REF(-)}$ with the $R_{REF(+)}$ resistor tied to ground. The advantage of this arrangement is the presence of very high impedance at the $V_{R(-)}$ terminal while the reference current flows from ground through $R_{REF(+)}$ into the $V_{R(+)}$ terminal.

The Am6071 has a wide output voltage compliance suitable for driving a variety of loads. With I_{REF} = 512µA and V− = −15V, positive voltage compliance is +18V and negative voltage compliance is −5.0V. For other values of I_{REF} and V−, the negative voltage compliance, $V_{OC(-)}$, may be calculated as follows:

$$V_{OC(-)} = (V-) + 2(I_{REF} \cdot 1.55k\Omega) + 8.4V,$$

where 1.55kΩ and 8.4V are equivalent worst case values for the Am6071.

The following table contains $V_{OC(-)}$ values for some specific V−, I_{REF}, and I_{FS} values.

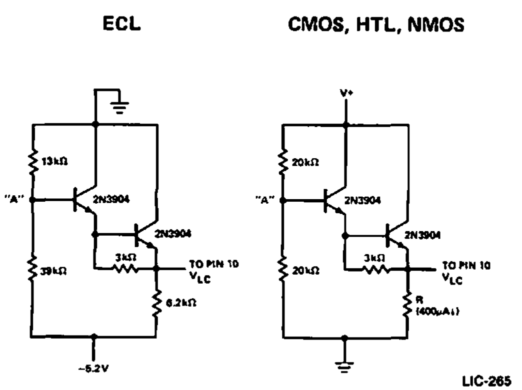
Negative Output Voltage Compliance $V_{OC(-)}$

V−	I_{REF} (I_{FS})		
	256µA (1mA)	512µA (2mA)	1024µA (4mA)
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

The V_{LC} input can accommodate various logic input switching threshold voltages allowing the Am6071 to interface with various logic families. This input should be placed at a potential which is 1.4V below the desired logic input switching threshold. Two external discrete circuits which provide this function for non-TTL driven inputs are shown in Figure 4. For TTL-driven logic inputs, the V_{LC} input should be grounded. If negative voltages are applied at the digital logic inputs, they must have a value which is more positive than the sum of the chosen V− value and +10V.

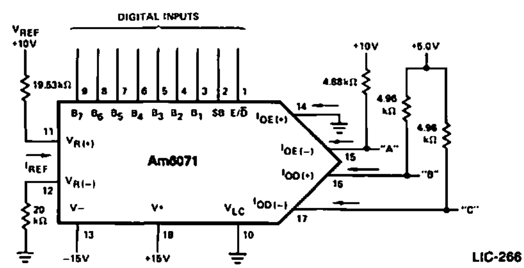
With a V− value chosen between −15V and −11V, the $V_{OC(-)}$, the input reference common mode voltage range, and the logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− value chosen.

With a V+ value chosen between +5V and +15V, the reference amplifier common mode positive voltage range and the V_{LC} input values are reduced by an amount equivalent to the difference between +15V and the V+ value chosen.



(See Notes 2 and 3)

Figure 4. Interfacing Circuits for ECL, CMOS, HTL, and NMOS Logic Inputs.



INPUT CODE (E/D̄, SB, B_1, ..., B_7)	OUTPUT VOLTAGE (V) "A"	"B"	"C"	DIFF
10 111 1111	0			
10 110 1111	+5.00	N/A	N/A	N/A
10 000 0000	+10.00			
01 111 1111		−5.00	+5.00	−10.00
01 110 1111		+0.00	+5.00	−5.00
01 000 0000	N/A	+5.00	+5.00	0
00 000 0000		+5.00	+5.00	0
00 110 1111		+5.00	+0.00	+5.00
00 111 1111		+5.00	−5.00	+10.00

Figure 5. Resistive Output Connections.

ADDITIONAL DECODE OUTPUT CURRENT TABLES

Table 3
Normalized Decoder Output (Sign Bit Excluded)

		CHORD (C)							
		0	1	2	3	4	5	6	7
STEP (S)		000	001	010	011	100	101	110	111
0	0000	1	33	66	132	264	528	1056	2112
1	0001	3	35	70	140	280	560	1120	2240
2	0010	5	37	74	148	296	592	1184	2368
3	0011	7	39	78	156	312	624	1248	2496
4	0100	9	41	82	164	328	656	1312	2624
5	0101	11	43	86	172	344	688	1376	2752
6	0110	13	45	90	180	360	720	1440	2880
7	0111	15	47	94	188	376	752	1504	3008
8	1000	17	49	98	196	392	784	1568	3136
9	1001	19	51	102	204	408	816	1632	3264
10	1010	21	53	106	212	424	848	1696	3392
11	1011	23	55	110	220	440	880	1760	3520
12	1100	25	57	114	228	456	912	1824	3648
13	1101	27	59	118	236	462	944	1888	3776
14	1110	29	61	122	244	488	976	1952	3904
15	1111	31	63	126	252	504	1008	2016	4032
STEP SIZE		2	2	4	8	16	32	64	128

The normalized decode current, ($I_{C,S}$), where C is chord number and S is step number, is calculated using: $I_{CS} = 2^C(S + 16.5)$ for $C \geq 1$, and $I_{C,S} = 2S + 1$ for $C = 0$. The ideal decode current, (I_{OD}), in μA is calculated using: $I_{OO} = (I_{C,S}/I_{7,15(norm.)}) \cdot I_{FS}(\mu A)$, where $I_{C,S}$ is the corresponding normalized current.

Table 4
Normalized Encoder Output (Sign Bit Excluded)

		CHORD (C)							
		0	1	2	3	4	5	6	7
STEP (S)		000	001	010	011	100	101	110	111
0	0000	2	34	68	136	272	544	1088	2176
1	0001	4	36	72	144	288	576	1152	2304
2	0010	6	38	76	152	304	608	1216	2432
3	0011	8	40	80	160	320	640	1280	2560
4	0100	10	42	84	168	336	672	1344	2688
5	0101	12	44	88	176	352	704	1408	2816
6	0110	14	46	92	184	368	736	1472	2944
7	0111	16	48	96	192	384	768	1536	3072
8	1000	18	50	100	200	400	800	1600	3200
9	1001	20	52	104	208	416	832	1664	3328
10	1010	22	54	108	216	432	864	1728	3456
11	1011	24	56	112	224	448	896	1792	3584
12	1100	26	58	116	232	464	928	1856	3712
13	1101	28	60	120	240	480	960	1920	3840
14	1110	30	62	124	248	496	992	1984	3968
15	1111	32	64	128	256	512	1024	2048	4096
STEP SIZE		2	2	4	8	16	32	64	128

ADDITIONAL DECODE OUTPUT CURRENT TABLES (Cont.)

Table 5
Decoder Step Size Summary

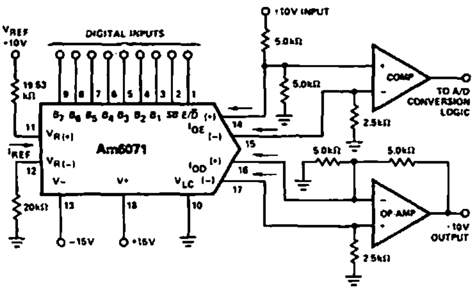
Chord	Step Size Normalized to Full Scale	Step Size in μA with 2016μA F. S.	Step Size as a % of Full Scale	Step Size in dB at Chord Endpoints	Step Size as a % of Reading at Chord Endpoints	Resolution & Accuracy of Equivalent Binary DAC
0	2	1.0	0.05%	0.58	6.45%	Sign + 11 Bits
1	2	1.0	0.05%	0.28	3.17%	Sign + 11 Bits
2	4	2.0	0.1%	0.28	3.17%	Sign + 10 Bits
3	8	4.0	0.2%	0.28	3.17%	Sign + 9 Bits
4	16	8.0	0.4%	0.28	3.17%	Sign + 8 Bits
5	32	16.0	0.8%	0.28	3.17%	Sign + 7 Bits
6	64	32.0	1.6%	0.28	3.17%	Sign + 6 Bits
7	128	64.0	3.2%	0.28	3.17%	Sign + 5 Bits

Table 6
Decoder Chord Size Summary

Chord	Chord Endpoints Normalized to Full Scale	Chord Endpoints in μA with 2016μA F. S.	Chord Endpoints as a % of Full Scale	Chord Endpoints in dB Down from Full Scale
0	31	15.5	0.77%	−42.28
1	63	31.5	1.56%	−36.12
2	126	63.0	3.13%	−30.10
3	252	126.0	6.25%	−24.08
4	504	252.0	12.5%	−18.06
5	1008	504.0	25.0%	−12.04
6	2016	1008.0	50.0%	−6.02
7	4032	2016.0	100%	0

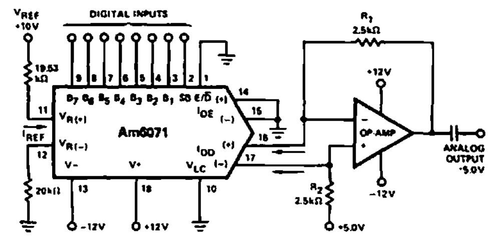
BASIC CIRCUIT CONNECTIONS

±10V RANGE ENCODER/DECODER CONNECTIONS



LIC-267

COMPLIANCE EXTENSION USING AC COUPLED OUTPUT



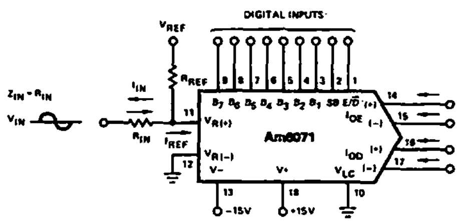
IDEAL VALUES:

$I_{REF} = 512\mu A$

$I_{FS} = 2016\mu A$

LIC-268

LOW INPUT IMPEDANCE CONNECTION

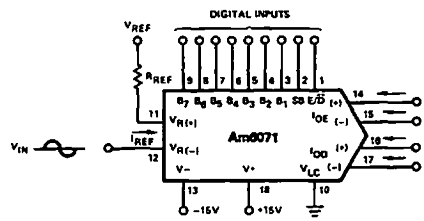


$I_{REF} = V_{IN}/R_{IN} + V_{REF}/R_{REF}$

$I_{FS} \approx 4 \cdot I_{REF}$

LIC-269

HIGH INPUT IMPEDANCE CONNECTION

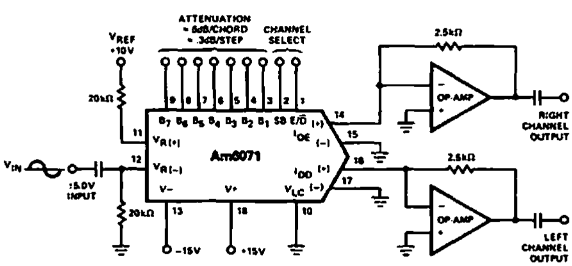


$I_{REF} = (V_{REF} - V_{IN})/R_{REF}$

$I_{FS} \approx 4 \cdot I_{REF}$

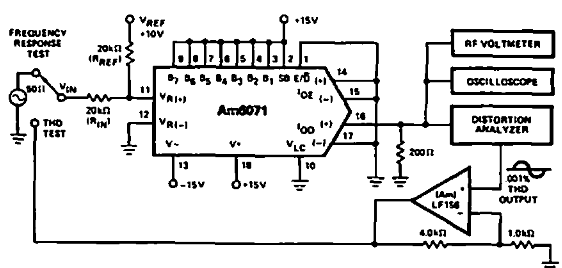
LIC-270

LOGARITHMIC DIGITAL GAIN CONTROL (Notes 4 & 5)



LIC-271

REFERENCE AMPLIFIER DYNAMIC TEST CIRCUIT

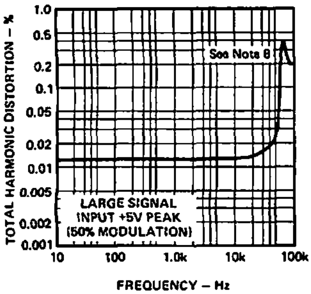


LIC-272

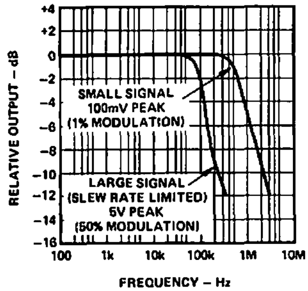
Notes: 4. Low distortion outputs are provided over a 72dB range.
5. Up to 4 channels of output may be selected by E/$\overline{D}$ and SB logic inputs.

TYPICAL PERFORMANCE CURVES

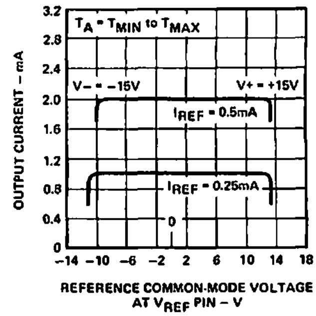
Reference Amplifier Total Harmonic Distortion Versus Frequency (80kHz Filter) (Notes 6, 7, 8)



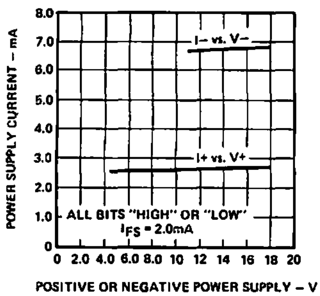
Reference Amplifier Input Frequency Response



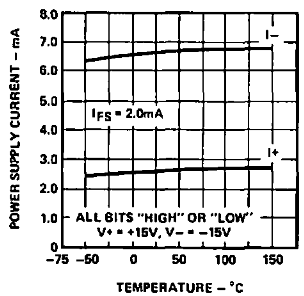
Reference Amplifier Input Common-Mode Range (Note 9)



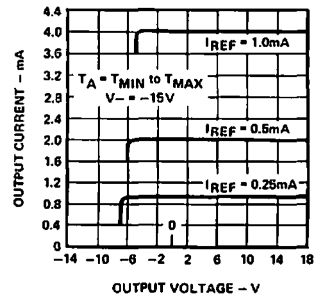
Power Supply Currents Versus Power Supply Voltages



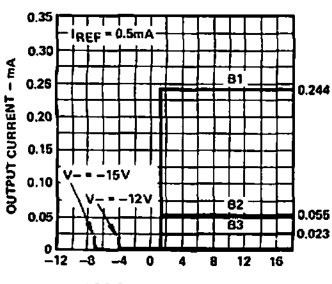
Power Supply Currents Versus Temperature



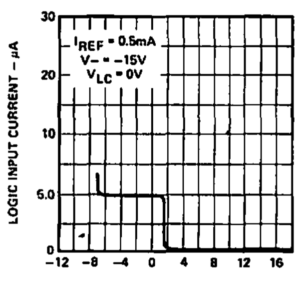
Output Current Versus Output Voltage (Output Voltage Compliance)



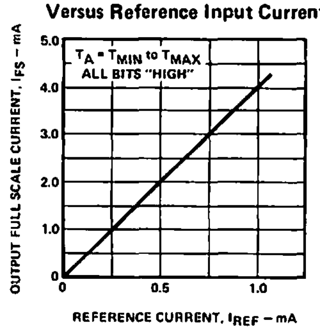
Bit Transfer Characteristics (Note 10)



Logic Input Current Versus Input Voltage and Logic Input Range (Note 11)



Output Full Scale Current Versus Reference Input Current



LIC-273

Notes:
6. THD is nearly independent of the logic input code.
7. Similar results are obtained for a high input impedance connection using $V_{R(-)}$ as an input.
8. Increased distortion above 50kHz is due to a slew rate limiting effect which determines the large signal bandwidth. For an input of ±2.5V peak (25% modulation), the bandwidth is 100kHz.
9. Positive common mode range is always (V+) –1.5V.
10. All bits are fully switched with less than a half step error at switching points which are guaranteed to lie between 0.8V and 2.0V over the operating temperature range.
11. The logic input voltage range is independent of the positive power supply and logic inputs may swing above the supply.

APPLICATIONS

The companding D/A converter is particularly suited for applications requiring a wide dynamic range.

Systems requiring fine control resulting in a constant rate of change or set point controls are economically achieved using these devices.

Instrumentation, Control and μ-Processor based applications include:

Digital data recording
PCM telemetry systems
Servo systems
Function generation
Data acquisition systems

Telecommunications applications include:

PCM Codec telephone systems
Intercom systems
Military voice communication systems
Radar systems
Voice Encryption

Audio Applications:

Recording
Multiplexing of analog signals
Voice synthesis

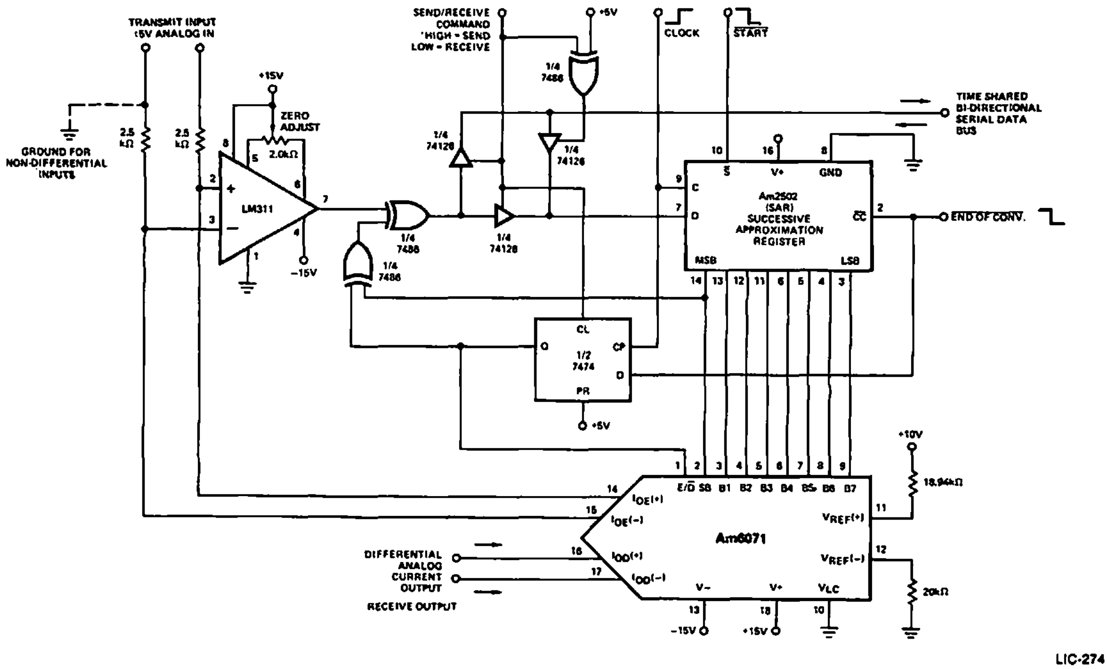
Other companding converters offered by Advanced Micro Devices:

If particular interest lies in a companding D/A converter operating to the D3 compandor tracking specification and meeting the Bell System μ-255 companding law, see the Am6072 data sheet.

For a CCITT unit having an A-law characteristic see the Am6073 data sheet.

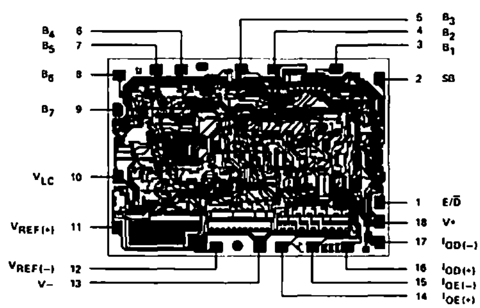
μ-law applications other than telecommunications systems are described in the Am6070 data sheet.

SERIAL DATA TRANSCEIVING CONVERTER
(1/2 OF SYSTEM SHOWN)



Notes:
1. Complementary send/receive commands are required for the two ends.
2. $\overline{\text{START}}$ must be held low for one clock cycle to begin a send or receive cycle.
3. The SAR is used as a serial-in/parallel out register in the receive mode.
4. CLOCK and $\overline{\text{START}}$ may be connected in parallel at both ends.
5. Conversion is completed in 9 clock cycles.
6. Receive output is available for one full clock cycle.

Metallization and Pad Layout



80 X 114 Mils

Am6072

Companding D-to-A Converter for PCM Communication Systems

PRELIMINARY INFORMATION

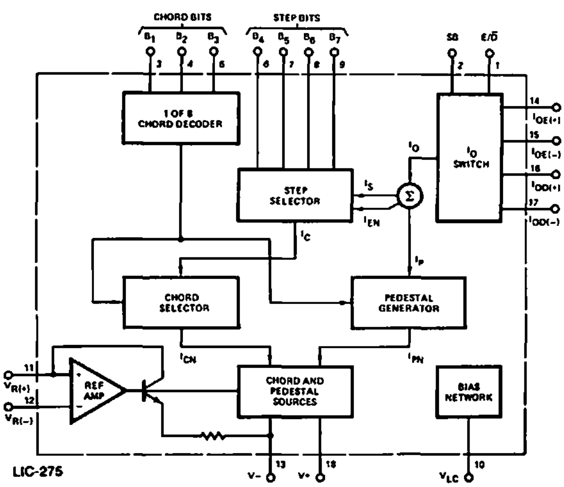
Distinctive Characteristics

- Tested to D3 compandor tracking specification
- Absolute accuracy specified – includes all errors over temperature range
- Settling time 300ns typical
- Ideal for multiplexed PCM systems
- Output dynamic range of 72 dB
- Improved pin-for-pin replacement for DAC-86
- Microprocessor controlled operations
- Multiplying operation
- Negligible output noise
- Monotonicity guaranteed over entire dynamic range
- Wide output voltage compliance
- Low power consumption

GENERAL DESCRIPTION

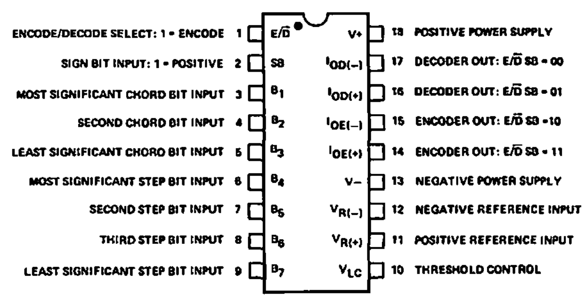
The Am6072 is a monolithic 8-bit, companding digital-to-analog (D/A) data converter with true current outputs and large output voltage compliance for fast driving a variety of loads. The transfer function of the Am6072 complies with the Bell System μ-255 companding law, $Y = 0.18 \ln(1 + \mu x)$, and consists of 15 linear segments or chords. A particular chord is identified with the sign bit input, (SB), and three chord select input bits. Each chord contains 16 uniformly spaced linear steps which are determined by four step select input bits. The resulting dynamic range achieved with this 8-bit format is 72dB. Accuracy and monoticity are assured by the internal circuit design and are guaranteed over the full temperature range. The Am6072 is tested to the Bell D3 channel bank compandor tracking specification for pulse code modulation (PCM) transmission systems. The application of the Am6072 in communication systems provides an increased signal-to-noise ratio, reduces system signal distortion, and stimulates wider usage of computerized channel switching. Other application areas include digital audio recording, voice synthesis, and secure communications. When used in PCM communication systems, the Am6072 functions as a complete PCM decoder with additional encoding capabilities which make it ideal for implementation in CODEC circuits.

FUNCTIONAL BLOCK DIAGRAM



LIC-275

CONNECTION DIAGRAM
Am6072



Top View

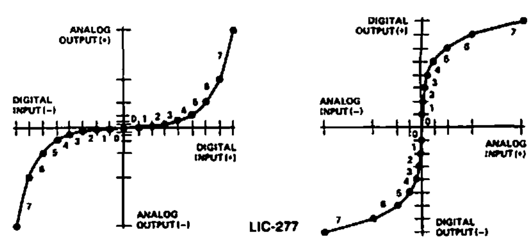
Pin 1 is marked for orientation. LIC-276

ORDERING INFORMATION

Part Number	Temperature	Accuracy
Am6072DM	–55°C to +125°C	Conforms to D3 Spec.
Am6072DC	0°C to +70°C	Conforms to D3 Spec.

SIMPLIFIED CONVERSION TRANSFER FUNCTIONS

Decoder Characteristic | Encoder Characteristic



LIC-277

MAXIMUM RATINGS above which useful life may be impaired

V+ Supply to V– Supply	36V	Operating Temperature	
V_{LC} Swing	V– plus 8V to V+	MIL Grade	–55°C to +125°C
Output Voltage Swing	V– plus 8V to V– plus 36V	COM'L Grade	0°C to +70°C
Reference Inputs	V– to V+	Storage Temperature	–65°C to +150°C
Reference Input Differential Voltage	±18V	Power Dissipation $T_A \leq 100°C$	500mW
Reference Input Current	1.25mA	For $T_A > 100°C$ derate at	10mW/°C
Logic Inputs	V– plus 8V to V– plus 36V	Lead Soldering Temperature	300°C (60 sec)

GUARANTEED FUNCTIONAL SPECIFICATIONS

Resolution	±128 Steps
Monotonicity	For both groups of 128 steps and over full operating temperature range
Dynamic Range	72 dB, $(20 \log (I_{7,15}/I_{0,1}))$

ELECTRICAL CHARACTERISTICS (Note 1)

These specifications apply for V+ = +15V, V– = –15V, I_{REF} = 528µA, 0°C ≤ T_A ≤ +70°C, for the commercial grade, –55°C ≤ T_A ≤ +125°C, for the military grade, and for all 4 outputs unless otherwise specified.

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_s	Settling Time	To within ±1/2 step at T_A = 25°C, Output switched from I_{ZS} to I_{FS}	–	300	500	ns
	Chord Endpoint Accuracy	V_{REF} = +10.000V, R_{REF+} = 18.94kΩ, R_{REF-} = 20kΩ, –5V < V_{OUT} < +18V	See Table 1 for absolute accuracy limits which cover all errors related to the transfer characteristic.			
	Step Nonlinearity					
I_{EN}	Encode Current					
$I_{FS}(D)$ $I_{FS}(E)$	Full Scale Current Deviation from Ideal					
$I_O(+)-I_O(-)$	Full Scale Current Symmetry Error					
I_{ZS}	Zero Scale Current					
ΔI_{FS}	Full Scale Current Drift					
V_{OC}	Output Voltage Compliance	Output within limits specified by Table 1	–5	–	+18	Volts
I_{DIS}	Disable Current	Leakage of output disabled by E/$\overline{D}$ or SB	–	5.0	50	nA
I_{FSR}	Output Current Range		0	2.0	4.2	mA
V_{IL}	Logic Input Levels — Logic "0"	V_{LC} = 0V	–	–	0.8	Volts
V_{IH}	Logic Input Levels — Logic "1"		2.0	–	–	Volts
I_{IN}	Logic Input Current	V_{IN} = –5V to +18V	–	–	40	µA
V_{IS}	Logic Input Swing	V– = –15V	–5	–	+18	Volts
I_{BREF-}	Reference Bias Current		–	–1.0	–4.0	µA
di/dt	Reference Input Slew Rate		0.12	0.25	–	mA/µs
$PSSI_{FS+}$	Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	V+ = +4.5 to +18V, V– = –15V	–	0.005	0.1	dB
$PSSI_{FS-}$		V– = –10.8V to –18V, V+ = +15V	–	0.01	0.1	dB
I+	Power Supply Current	V+ = +5V to +15V, V– = –15V, I_{PS} = 2.0mA	–	2.7	4.0	mA
I–			–	–6.7	–8.8	mA
P_D	Power Dissipation	V– = –15V, V_{OUT} = 0V, I_{FS} = 2.0mA; V+ = +5V	–	114	152	mW
		V+ = +15V	–	141	192	mW

Note 1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) the step size is 0.5µA, while in the last chord near full scale (C_7) the step size is 64µA.

ELECTRICAL CHARACTERISTICS (Cont.)

TABLE 1
ABSOLUTE DECODER OUTPUT CURRENT LEVELS IN μA

STEP NO.	CHORD NO. 0	1	2	3	4	5	6	7
0	−.250 .000 .250	7.789 8.250 8.739	24.048 24.750 25.473	56.112 57.750 59.436	120.24 123.75 127.36	248.49 255.75 263.22	505.00 519.75 534.93	1018.02 1047.75 1078.34
1	.250 .500 .750	8.733 9.250 9.798	25.991 26.750 27.531	59.998 61.750 63.553	128.01 131.75 135.60	264.04 271.75 279.69	536.10 551.75 567.86	1080.21 1111.75 1144.21
2	.750 1.000 1.250	9.677 10.250 10.857	27.934 28.750 29.590	63.885 65.750 67.670	135.79 139.75 143.83	279.59 287.75 296.15	567.19 583.75 600.80	1142.39 1175.75 1210.08
3	1.250 1.500 1.750	10.621 11.250 11.917	29.878 30.750 31.648	67.771 69.750 71.787	143.56 147.75 152.06	295.13 303.75 312.62	598.28 615.75 633.73	1204.58 1239.75 1275.95
4	1.750 2.000 2.250	11.565 12.250 12.976	31.821 32.750 33.706	71.858 73.750 75.904	151.33 155.75 160.30	310.68 319.75 329.09	629.37 647.75 666.66	1266.76 1303.75 1341.82
5	2.250 2.500 2.750	12.509 13.250 14.035	33.764 34.750 35.765	75.544 77.750 80.020	159.10 163.75 168.53	326.22 335.75 345.55	660.46 679.75 699.60	1328.94 1367.75 1407.69
6	2.750 3.000 3.250	13.453 14.250 15.094	35.707 36.750 37.823	79.431 81.750 84.137	166.88 171.75 176.77	341.77 351.75 362.02	691.56 711.75 732.53	1391.13 1431.75 1473.56
7	3.250 3.500 3.750	14.397 15.250 16.154	37.651 38.750 39.882	83.317 85.750 88.254	174.65 179.75 185.00	357.32 367.75 378.49	722.65 743.75 765.47	1453.31 1495.75 1539.43
8	3.750 4.000 4.250	15.341 16.250 17.213	39.594 40.780 41.940	87.204 89.750 92.371	182.42 187.75 193.23	372.86 383.75 394.96	753.74 775.75 798.40	1515.60 1559.75 1605.30
9	4.248 4.500 4.767	16.285 17.250 18.272	41.537 42.750 43.998	91.090 93.750 96.488	190.20 195.75 201.47	388.41 399.75 411.42	784.63 807.75 831.34	1577.68 1623.75 1671.16
10	4.720 5.000 5.296	17.229 18.250 19.331	43.480 44.750 46.057	94.977 97.750 100.604	197.97 203.75 209.70	403.95 415.75 427.89	815.02 839.75 864.27	1639.87 1687.75 1737.03
11	5.192 5.500 5.826	18.173 19.250 19.612	46.424 46.750 48.115	98.863 101.750 104.721	205.74 211.75 217.93	419.50 431.75 444.36	847.02 871.75 897.21	1702.05 1751.75 1802.90
12	5.664 6.000 6.356	19.875 20.250 20.841	47.367 48.750 50.174	102.750 105.750 108.838	213.52 219.75 226.17	435.05 447.75 460.82	878.11 903.75 930.14	1764.23 1815.75 1868.77
13	6.136 6.500 6.885	20.647 21.250 21.871	49.310 50.750 52.232	106.636 109.750 112.955	221.29 227.75 234.40	450.59 463.75 477.29	909.20 935.75 963.07	1826.42 1879.75 1934.64
14	6.608 7.000 7.415	21.619 22.250 22.900	51.263 52.750 54.290	110.523 113.750 117.072	229.06 235.75 242.63	466.14 479.75 493.76	940.29 967.75 996.01	1888.60 1943.75 2000.51
15	7.080 7.500 7.944	22.590 23.250 23.929	53.197 54.750 56.349	114.409 117.750 121.188	236.83 243.75 250.87	481.68 495.75 510.23	971.39 999.75 1028.94	1950.79 2007.75 2066.38
STEP SIZE	.5	1	2	4	8	16	32	64

Minimum, ideal and maximum values are specified for each step. The minimum and maximum values are specified to comply with the Bell D3 compandor tracking requirements. All four outputs are guaranteed, the encode outputs being specified to limits a half step higher than those shown above. This takes into account the combined effects of chord endpoint accuracy, step nonlinearity, encode current error, full scale current deviation from ideal, full scale symmetry error, zero scale current, full scale drift, and output impedance over the specified output voltage compliance range. Note that the guaranteed monotonicity ensures that adjacent step current levels will not overlap as might otherwise be implied from the minimum and maximum values shown in the above table.

TABLE 2
IDEAL DECODER OUTPUT VALUES EXPRESSED IN dB DOWN FROM OVERLOAD LEVEL (+3dBmo)

STEP \ CHORD	0	1	2	3	4	5	6	7
0	–	−44.73	−35.18	−27.82	−21.20	−14.90	−8.74	−2.65
1	−69.07	−43.73	−34.51	−27.24	−20.66	−14.37	−8.22	−2.13
2	−63.05	−42.84	−33.88	−26.70	−20.15	−13.87	−7.73	−1.66
3	−59.53	−42.03	−33.30	−26.18	−19.66	−13.40	−7.27	−1.19
4	−57.03	−41.29	−32.75	−25.70	−19.21	−12.96	−6.83	−0.75
5	−55.10	−40.61	−32.24	−25.24	−18.77	−12.53	−6.41	−0.33
6	−53.51	−39.98	−31.75	−24.80	−18.36	−12.13	−6.01	+0.06
7	−52.17	−39.39	−31.29	−24.39	−17.96	−11.74	−5.63	+0.44
8	−51.01	−38.84	−30.85	−23.99	−17.58	−11.37	−5.26	+0.81
9	−49.99	−38.32	−30.44	−23.61	−17.22	−11.02	−4.91	+1.16
10	−49.07	−37.83	−30.04	−23.25	−16.87	−10.68	−4.57	+1.49
11	−48.25	−37.37	−29.66	−22.90	−16.54	−10.35	−4.25	+1.82
12	−47.49	−36.93	−29.29	−22.57	−16.22	−10.03	−3.93	+2.13
13	−46.80	−36.51	−28.95	−22.25	−15.81	−9.73	−3.63	+2.43
14	−46.15	−36.11	−28.61	−21.94	−15.61	−9.43	−3.34	+2.72
15	−45.55	−35.73	−28.29	−21.63	−15.32	−9.15	−3.06	+3.00

The −37 dBmo and −50 dBmo output points significant for the Bell D3 system specification can be found between steps 11 and 12 on chord 1, and steps 8 and 9 on chord 0, respectively. Outputs corresponding to points below −50dB are specified in Table 1 for an accuracy of ± a half step.

THEORY OF OPERATION

Functional Description

The Am6072 is an 8-bit, nonlinear, digital-to-analog converter with high impedance current outputs. The output current value is proportional to the product of the digital inputs and the input reference current. The full scale output current, I_{FS}, is specified by the input binary code 111 1111, and is a linear function of the reference current, I_{REF}. There are two operating modes, encode and decode, which are controlled by the Encode/Decode, (E/$\overline{D}$), input signal. A logic 1 applied to the E/$\overline{D}$ input places the Am6072 in the encode mode and current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output, depending on the state of the Sign Bit (SB) input. A logic 0 at the E/$\overline{D}$ input places the Am6072 in the decode mode.

The transfer characteristic is a piece-wise linear approximation to the Bell System μ-225 logarithmic law which can be written as follows:

$$Y = 0.18\ell n\,(1 + \mu\ |X|)\ \mathrm{sgn}\,(X)$$

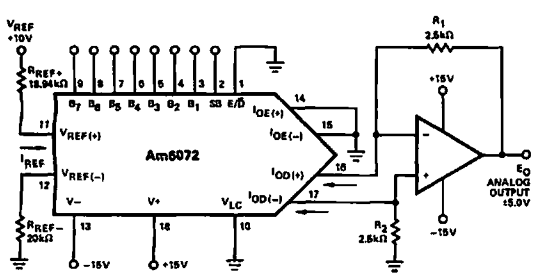
where: X = analog signal level normalized to unity (encoder input or decoder output)
Y = digital signal level normalized to unity (encoder output or decoder input)
$\mu = 255$

The current flows from the external circuit into one of four possible analog outputs determined by the SB and E/$\overline{D}$ inputs. The output current transfer function can be represented by a total of 16 segments or chords addressable through the SB input and three chord select bits. Each chord can be further divided into 16 steps, all of the same size. The step size changes from one chord to another, with the smallest step of 0.5μA found in the first chord near zero output current, and the largest step of 64μA found in the last chord near full scale output current. This nonlinear feature provides exceptional accuracy for small signal levels near zero output current. The accuracy for signal amplitudes corresponding to chord 0 is equivalent to that of a 12-bit linear, binary D/A converter. However, the ratio (in dB) between the chord endpoint current, (Step 15), and the current which corresponds to the preceding step, (Step 14), is maintained at about 0.3dB over most of the dynamic range. The difference between the ratios of full scale current to chord endpoint currents of adjacent chords is similarly maintained at approximately 6dB over most of the dynamic range. Resulting signal-to-quantizing distortions due to non-uniform quantizing levels maintain an acceptably low value over a 40dB range of input speech signals. Note that the 72dB output dynamic range for the Am6072 corresponds to the dynamic range of a sign plus 12-bit linear, binary D/A converter.

In order to achieve a smoother transition between adjacent chords, the step size between these chord end points is equal to 1.5 times the step size of the lower chord. Monotonic operation is guaranteed by the internal device design over the entire output dynamic range by specifying and maintaining the chord end points and step size deviations within the allowable limits.

Operating Modes

The basic converter function is conversion of digital input data into a corresponding analog current signal, i.e., the basic function is digital-to-analog decoding. The basic decoder connection for a sign plus 7-bit input configuration is shown in Figure 1. The corresponding dynamic range is 72dB, and input-output characteristics conform to the standard decoder transfer function with output current values specified in Table 1. The E/$\overline{D}$ input enables switching between the encode, $I_{OE(+)}$ or $I_{OE(-)}$, and the decode, $I_{OD(+)}$ or $I_{OD(-)}$, outputs. A typical encode/decode test circuit is shown in Figure 2. This circuit is used for output current measurements. When the E/$\overline{D}$ input is high, (a logic 1), the converter will assume the encode operating mode and the output current will flow into one of the I_{OE} outputs (as determined by the SB input). When operating in the encode mode as shown in Figure 3, an offset current equal to a half step in each chord is required to obtain the correct encoder transfer characteristic. Since the size of this step varies from one chord to another, it cannot easily be added externally. As indicated in the block diagram this required half step of encode current,

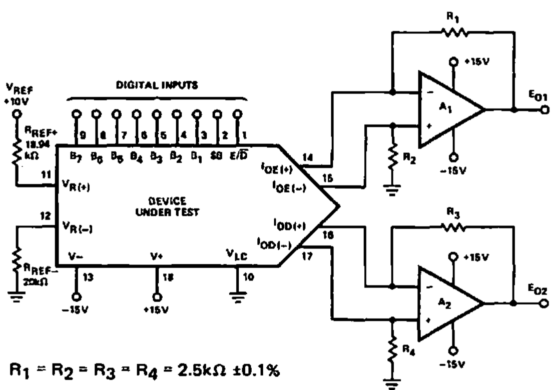


$I_{REF} = V_{REF}/R_{REF}$ LIC-278

IDEAL VALUES: I_{REF} = 528μA, I_{FS} = 2007.75μA

	E/$\overline{D}$	SB	B_1	B_2	B_3	B_4	B_5	B_6	B_7	E_O
POSITIVE FULL SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012V
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0V
(−) ZERO SCALE	0	0	0	0	0	0	0	0	0	0V
(−) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	−0.0012V
NEGATIVE FULL SCALE	0	0	1	1	1	1	1	1	1	−5.019V

Figure 1. Detailed Decoder Connections.



$R_1 = R_2 = R_3 = R_4$ = 2.5kΩ ±0.1%

LIC-279

LINE SELECTION TABLE

TEST GROUP	E/$\overline{D}$	SB	OUTPUT MEASUREMENT	
1	1	1	$I_{OE(+)}$	(E_{O1}/R_1)
2	1	0	$I_{OE(-)}$	(E_{O1}/R_2)
3	0	1	$I_{OD(+)}$	(E_{O2}/R_3)
4	0	0	$I_{OD(-)}$	(E_{O2}/R_4)

Figure 2. Output Current DC Test Circuit.

I_{EN}, is automatically added to the I_{OE} output through the internal chip design. This additional current will, for example, make the ideal full scale current in the encode mode larger than the same current in the decode mode by 32μA. Similarly, the current levels in the first chord near the origin will be offset by 0.25μA, which will bring the ideal encode current value for step 0 on chord 0 to $\pm$0.25μA with respect to the corresponding decode current value of 0.0μA. This additional encode half step of current can be used for extension of the output dynamic range from 72dB to 78dB, when the converter is performing only the decode function. The corresponding decoder connection utilizes the $E/\overline{D}$ input as a ninth digital input and has the outputs $I_{OD(+)}$ and $I_{OE(+)}$ and the outputs $I_{OD(-)}$ and $I_{OE(-)}$ tied together, respectively.

When encoding or compression of an analog signal is required, the Am6072 can be used together with a Successive Approximation Register (SAR), comparator, and additional SSI logic elements to perform the A/D data conversion, as shown in Figure 3. The encoder transfer function, shown on page 1, characterizes this A/D converter system. The first task of this system is to determine the polarity of the incoming analog signal and to generate a corresponding SB input value. When the proper Start, $\overline{S}$, and Conversion Complete, $\overline{CC}$, signal levels are set, the first clock pulse sets the MSB output of the SAR, Am2502, to a logic 0 and sets all other parallel digital outputs to logic 1 levels. At the same time, the flip-flop is triggered, and its output provides the $E/\overline{D}$ input with a logic 0 level. No current flows into the I_{OE} outputs. This disconnects the converter from the comparator inputs, and the incoming analog signal can be compared with the ground applied to the opposite comparator input. The resulting comparator output is fed to the Am2502 serial data input, D, through an exclusive-or gate. At the same time, the second input to the same exclusive-or gate is held at a logic 0 level by the additional successive approximation logic shown in Figure 3. This exclusive-or gate inverts the comparator's outputs whenever a negative signal polarity is detected. This maintains the proper output current coding, i.e., all ones for full scale and all zeros for zero scale.

The second clock pulse changes the $E/\overline{D}$ input back to a logic 1 level because the $\overline{CC}$ signal changed. It also clocks the D input signal of the Am2502 to its MSB output, and transfers it to the SB input of the Am6072. Depending upon the SB input level, current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output of the Am6072.

Nine total clock pulses are required to obtain a digital binary representation of the incoming analog signal at the eight Am2502 digital outputs. The resulting Am6072 analog output signal is compared with the analog input signal after each of the nine successive clock pulses. The analog signal should not be allowed to change its value during the data conversion time. In high speed systems, fast changes of the analog signals at the A/D system input are usually prevented by using sample and hold circuitry.

Additional Considerations and Recommendations

In Figure 1, an optional operational amplifier converts the Am6072 output current to a bipolar voltage output. When the SB input is a logic 1, sink current appears at the amplifier's negative input, and the amplifier acts as a current to voltage converter, yielding a positive voltage output. With the SB value at a logic 0, sink current appears at the amplifier's positive input. The amplifier behaves as a voltage follower, and the true current outputs will swing below ground with essentially no change in output current. The SB input steers current into the appropriate (+) or (−) output of the Am6072. The resulting operational amplifier's output in Figure 2 should ideally be symmetrical with resistors R1 and R2 matched.

In Figure 2, two operational amplifiers measure the currents of each of the four Am6072 analog outputs. Resistor tolerances of 0.1% give 0.1% output measurement error (approximately 2μA at full scale). The input offset currents of the A1 and A2 devices also increase output measurement error and this error is most significant near zero scale. The Am101A and 308 devices, for example, may be used for A1 and A2 since their maximum offset currents, which would add directly to the measurement error, are only 10nA and 1nA, respectively. The input offset voltages of the A1 and A2 devices, with output resistor values of

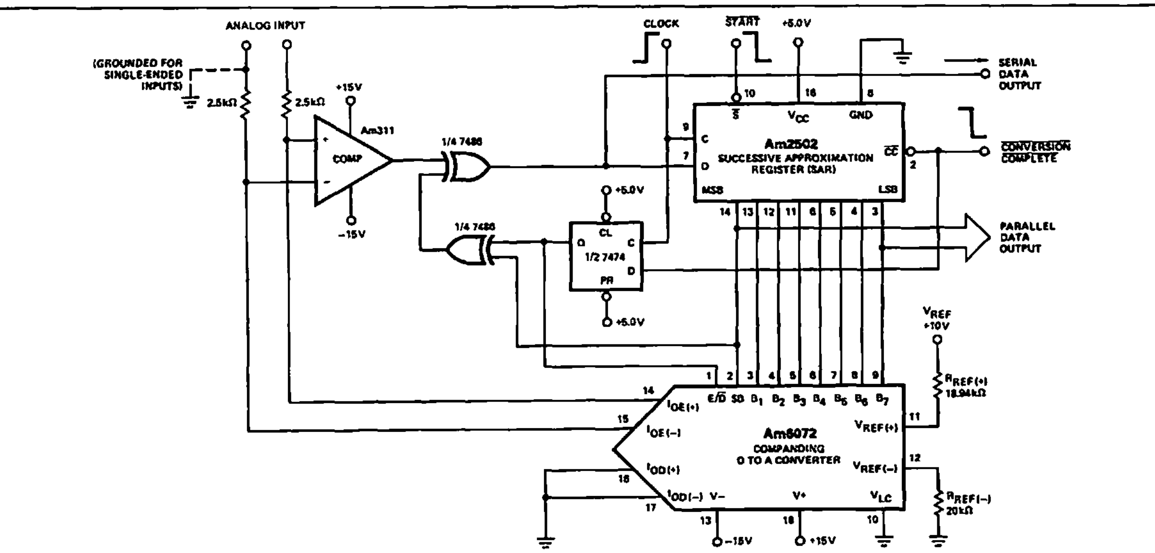


Figure 3. Detailed Encoder Connections.

2.5kΩ, also contribute to the output measurement error by a factor of 400nA for every mV of offset at the A1 and A2 outputs. Therefore, to minimize error, the offset voltages of A1 and A2 should be nulled.

The recommended operating range for the reference current I_{REF} is from 0.1mA to 1.0mA. The full scale output current, I_{FS}, is a linear function of the reference current, and may be calculated from the equation $I_{FS} = 3.8\ I_{REF}$. This tight relationship between I_{REF} and I_{FS} alleviates the requirement for trimming the I_{REF} current if the R_{REF} resistors values are within ±1% of the calculated value. Lower values of I_{REF} will reduce the negative power supply current, (I−), and will increase the reference amplifier negative common mode input voltage range.

The ideal value for the reference current $I_{REF} = V_{REF}/R_{REF}$ is 528μA. The corresponding ideal full scale decode and encode current values are 2007.75μA and 2039.75μA, respectively. A percentage change from the ideal I_{REF} value produced by changes in V_{REF} or R_{REF} values produces the same percentage change in decode and encode output current values. The positive voltage supply, V+, may be used, with certain precautions, for the positive reference voltage V_{REF}. In this case, the reference resistor $R_{REF(+)}$ should be split into two resistors and their junction bypassed to ground with a capacitor of 0.01μF. The total resistor value should provide the reference current I_{REF} = 528μA. The resistor $R_{REF(-)}$ value should be approximately equal to the $R_{REF(+)}$ value in order to compensate for the errors caused by the reference amplifier's input offset current.

An alternative to the positive reference voltage applications shown in Figures 1, 2 and 3 is the application of a negative voltage to the $V_{R(-)}$ terminal through the resistor $R_{REF(-)}$ with the $R_{REF(+)}$ resistor tied to ground. The advantage of this arrangement is the presence of very high impedance at the $V_{R(-)}$ terminal while the reference current flows from ground through $R_{REF(+)}$ into the $V_{R(+)}$ terminal.

The Am6072 has a wide output voltage compliance suitable for driving a variety of loads. With I_{REF} = 528μA and V− = −15V, positive voltage compliance is +18V and negative voltage compliance is −5.0V. For other values of I_{REF} and V−, the negative voltage compliance, $V_{OC(-)}$, may be calculated as follows:

$$V_{OC(-)} = (V-) + (2 \cdot I_{REF} \cdot 1.5k\Omega) + 8.4V.$$

The following table contains $V_{OC(-)}$ values for some specific V−, I_{REF}, and I_{FS} values.

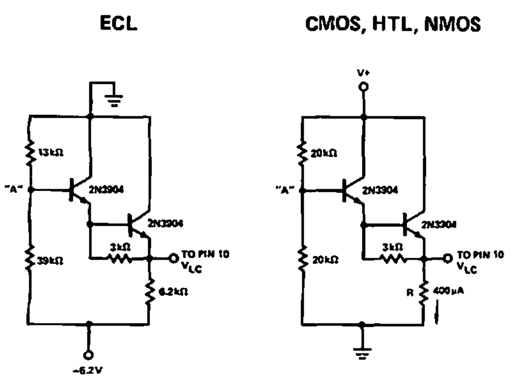
Negative Output Voltage Compliance $V_{OC(-)}$

V− \ I_{REF} (I_{FS})	264μA (1mA)	528μA (2mA)	1056μA (4mA)
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

The V_{LC} input can accommodate various logic input switching threshold voltages allowing the Am6072 to interface with various logic families. This input should be placed at a potential which is 1.4V below the desired logic input switching threshold. Two external discrete circuits which provide this function for non-TTL driven inputs are shown in Figure 4. For TTL-driven logic inputs, the V_{LC} input should be grounded. If negative voltages are applied at the digital logic inputs, they must have a value which is more positive than the sum of the chosen V− value and +10V.

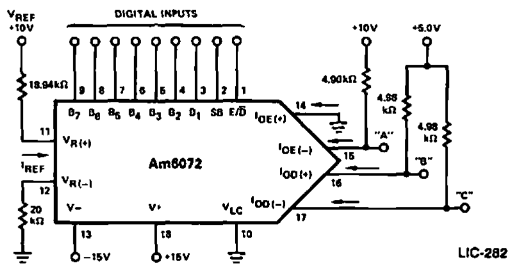
With a V− value chosen between −15V and −11V, the $V_{OC(-)}$, the input reference common mode voltage range, and the logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− value chosen.

With a V+ value chosen between +5V and +15V, the reference amplifier common mode positive voltage range and the V_{LC} input values are reduced by an amount equivalent to the difference between +15V and the V+ value chosen.



(See Notes 2 and 3)

Figure 4. Interfacing Circuits for ECL, CMOS, HTL, and NMOS Logic Inputs.



INPUT CODE (E/D̄, SB, B1, . . ., B7)	OUTPUT VOLTAGE (V) "A"	"B"	"C"	DIFF
10 111 1111	0	N/A	N/A	N/A
10 110 1111	+5.02			
10 000 0000	+10.00			
01 111 1111	N/A	−5.00	+5.00	−10.00
01 110 1111		+0.02	+5.00	−4.98
01 000 0000		+5.00	+5.00	0
00 000 0000		+5.00	+5.00	0
00 110 1111		+5.00	+0.02	+4.98
00 111 1111		+5.00	−5.00	+10.00

Figure 5. Resistive Output Connections.

Notes: 2. Set the voltage "A" to the desired logic input switching threshold.
3. Allowable range of logic threshold is typically −5V to +13.5V when operating the companding DAC on ±15V supplies.

ADDITIONAL DECODE OUTPUT CURRENT TABLES

Table 3
Normalized Decoder Output (Sign Bit Excluded)

Step (S) \ Chord (C)		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
Step Size		2	4	8	16	32	64	128	256

The normalized decode current, ($I_{C,S}$), is calculated using:

$$I_{C,S} = 2(2^C(S + 16.5) - 16.5)$$

where C = chord number; S = step number. The ideal decode current, (I_{OD}), in μA is calculated using:

$$I_{OD} = (I_{C,S}/I_{7,15(norm.)}) \cdot I_{FS}\ (\mu A)$$

where $I_{C,S}$ is the corresponding normalized current. To obtain normalized encode current values the corresponding normalized half-step value should be added to all entries in Table 3.

Table 4
Decoder Step Size Summary

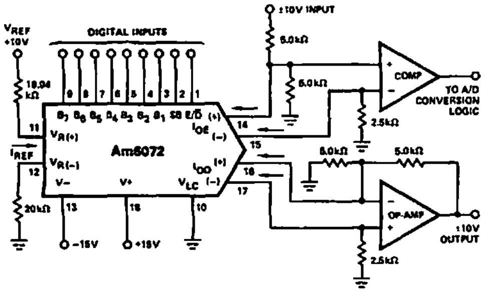
Chord	Step Size Normalized to Full Scale	Step Size in μA with 2007.75μA FS	Step Size as a % of Full Scale	Step Size in dB at Chord Endpoints	Step Size as a % of Reading at Chord Endpoints	Resolution & Accuracy of Equivalent Binary DAC
0	2	0.5	0.025%	0.60	6.67%	Sign + 12 Bits
1	4	1.0	0.05%	0.38	4.30%	Sign + 11 Bits
2	8	2.0	0.1%	0.32	3.65%	Sign + 10 Bits
3	16	4.0	0.2%	0.31	3.40%	Sign + 9 Bits
4	32	8.0	0.4%	0.29	3.28%	Sign + 8 Bits
5	64	16.0	0.8%	0.28	3.23%	Sign + 7 Bits
6	128	32.0	1.6%	0.28	3.20%	Sign + 6 Bits
7	256	64.0	3.2%	0.28	3.19%	Sign + 5 Bits

Table 5
Decoder Chord Size Summary

Chord	Chord Endpoints Normalized to Full Scale	Chord Endpoints in μA with 2007.75μA FS	Chord Endpoints as a % of Full Scale	Chord Endpoints in dB Down from Full Scale
0	30	7.5	0.37%	−48.55
1	93	23.25	1.16%	−38.73
2	219	54.75	2.73%	−31.29
3	471	117.75	5.86%	−24.63
4	975	243.75	12.1%	−18.32
5	1983	495.75	24.7%	−12.15
6	3999	999.75	49.8%	−6.06
7	8031	2007.75	100%	0

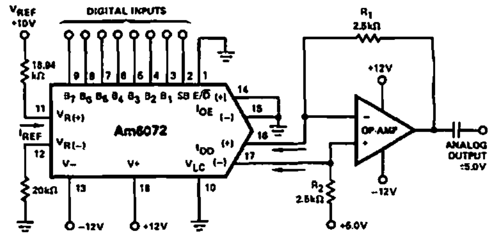
BASIC CIRCUIT CONNECTIONS

±10V RANGE ENCODER/DECODER CONNECTIONS



LIC-283

COMPLIANCE EXTENSION USING AC COUPLED OUTPUT



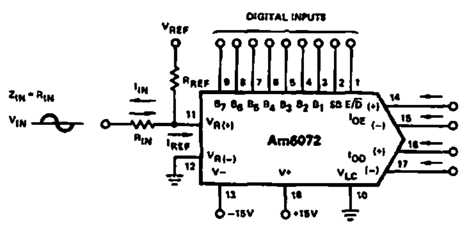
IDEAL VALUES:

$I_{REF} = 528\mu A$

$I_{FS} = 2007.75\mu A$

LIC-284

LOW INPUT IMPEDANCE CONNECTION

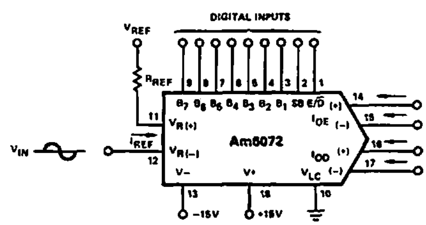


$I_{REF} = V_{IN}/R_{IN} + V_{REF}/R_{REF}$

$I_{FS} \approx 4 \bullet I_{REF}$

LIC-285

HIGH INPUT IMPEDANCE CONNECTION

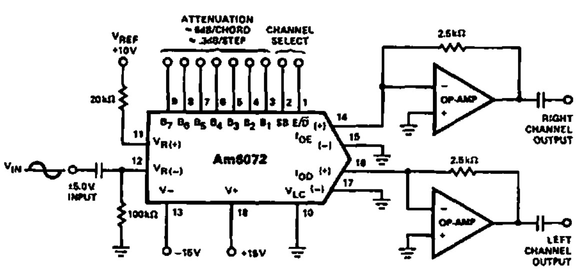


$I_{REF} = (V_{REF} - V_{IN})/R_{REF}$

$I_{FS} \approx 4 \bullet I_{REF}$

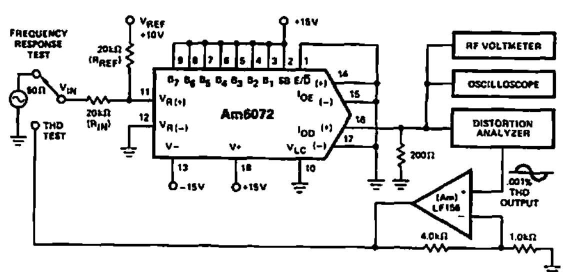
LIC-286

LOGARITHMIC DIGITAL GAIN CONTROL (Notes 4 & 5)



LIC-287

REFERENCE AMPLIFIER DYNAMIC TEST CIRCUIT

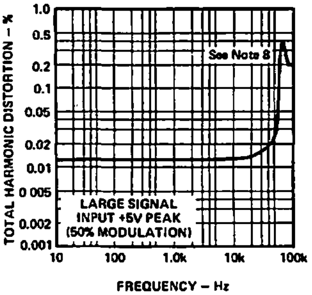


LIC-288

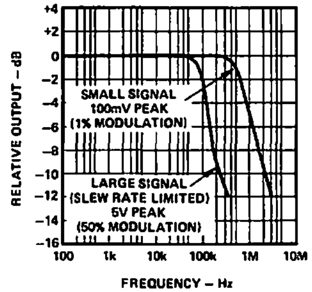
Notes: 4. Low distortion outputs are provided over a 72dB range.
5. Up to 4 channels of output may be selected by E/$\overline{D}$ and SB logic inputs.

TYPICAL PERFORMANCE CURVES

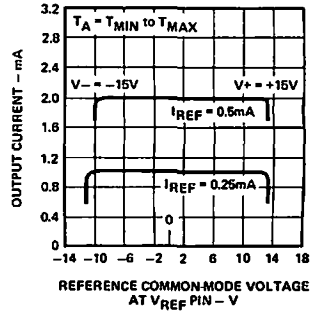
Reference Amplifier Total Harmonic Distortion Versus Frequency (80kHz Filter) (Notes 6, 7, 8)



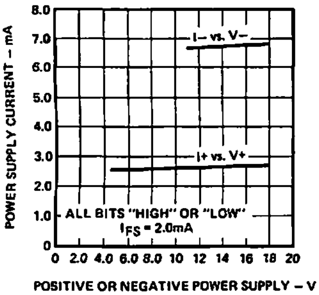
Reference Amplifier Input Frequency Response



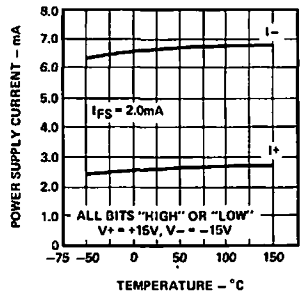
Reference Amplifier Input Common-Mode Range (Note 9)



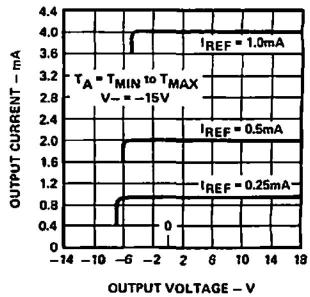
Power Supply Currents Versus Power Supply Voltages



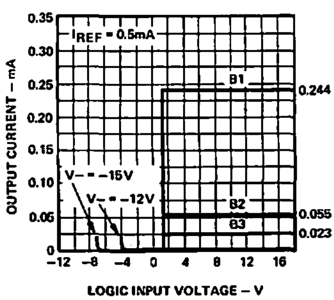
Power Supply Currents Versus Temperature



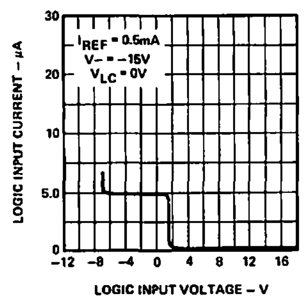
Output Current Versus Output Voltage (Output Voltage Compliance)



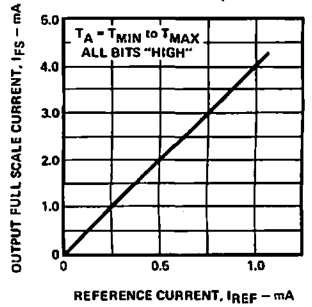
Bit Transfer Characteristics (Note 10)



Logic Input Current Versus Input Voltage and Logic Input Range (Note 11)



Output Full Scale Current Versus Reference Input Current

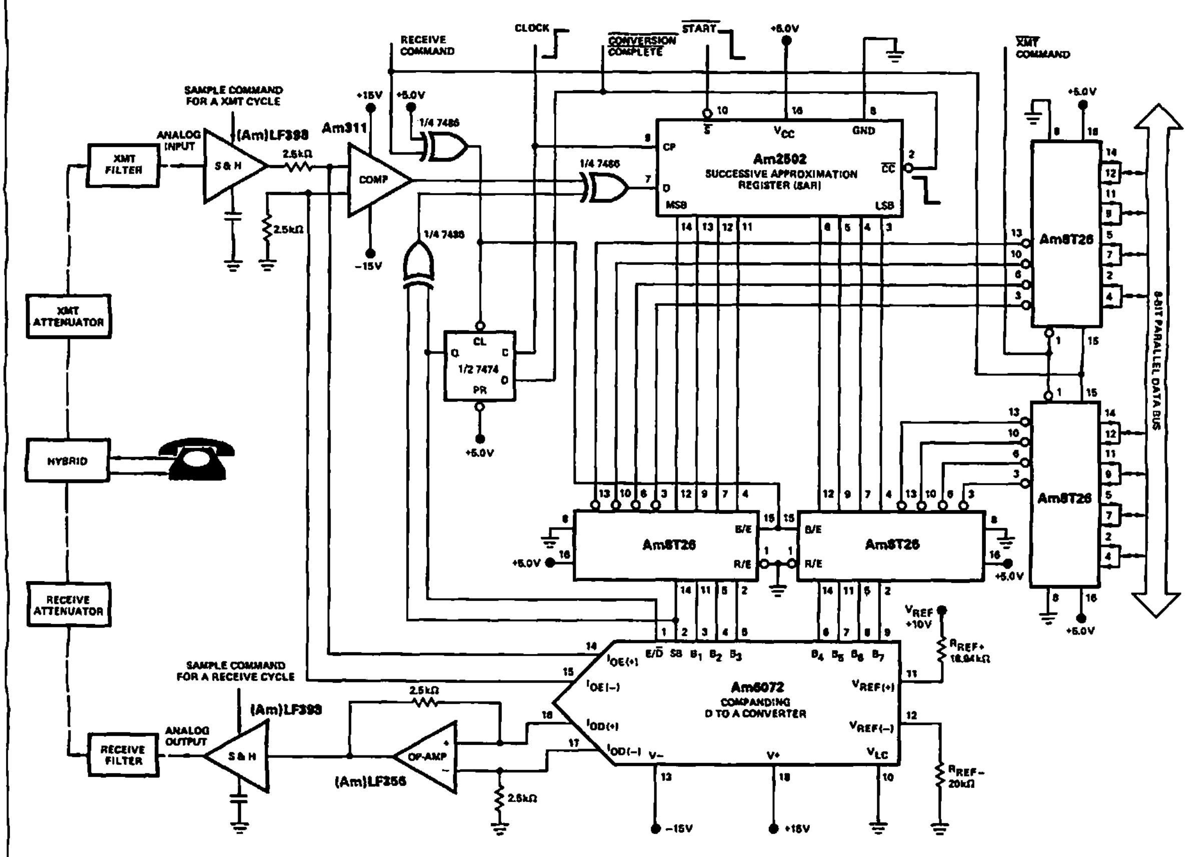


LIC-289

Notes:
6. THD is nearly independent of the logic input code.
7. Similar results are obtained for a high input impedance connection using $V_{R(-)}$ as an input.
8. Increased distortion above 50kHz is due to a slew rate limiting effect which determines the large signal bandwidth. For an input of ±2.5V peak (25% modulation), the bandwidth is 100kHz.
9. Positive common mode range is always (V+) –1.5V.
10. All bits are fully switched with less than a half step error at switching points which are guaranteed to lie between 0.8V and 2.0V over the operating temperature range.
11. The logic input voltage range is independent of the positive power supply and logic inputs may swing above the supply.

TIME SHARED CONVERTER CONNECTIONS

SINGLE CHANNEL PCM CODEC – PARALLEL DATA I/O



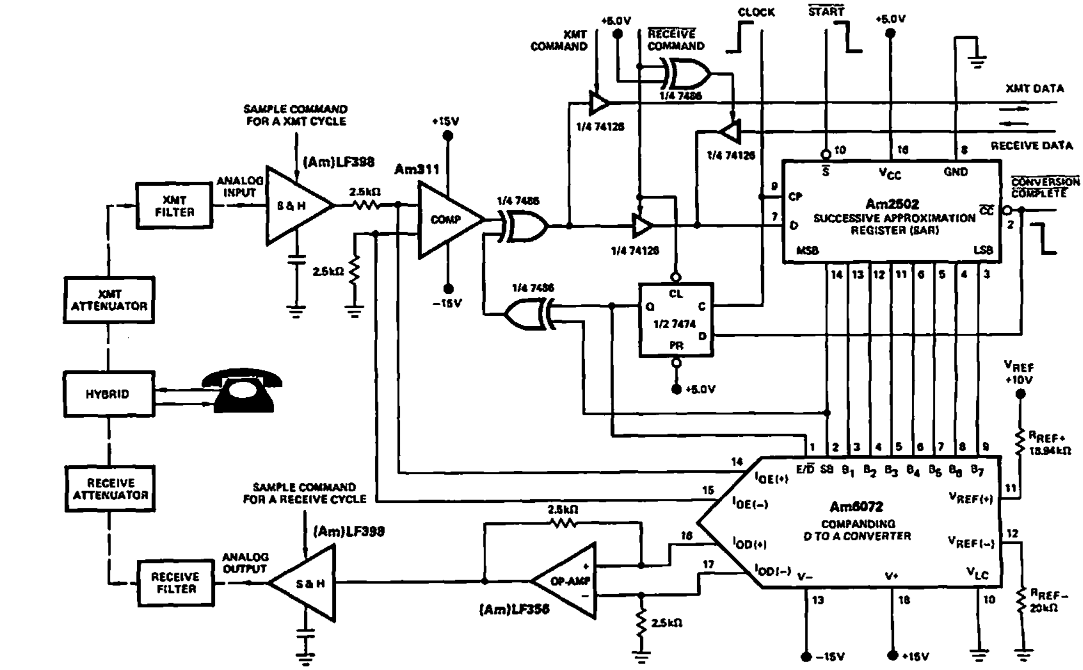
LIC-290

APPLICATION INFORMATION

1. To perform a transmit operation cycle the $\overline{\text{START}}$ pulse must be held low for one clock cycle; the receive operation is performed without the successive approximation register, SAR.
2. $\overline{\text{XMT}}$ and RECEIVE command signals are mutually exclusive.
3. Duration of the RECEIVE command signal must accommodate the Am6072 settling time plus the sampling time required by the sample and hold, (S & H), circuit used at the CODEC's analog output. The receiving data must not change during this time.
4. A $\overline{\text{XMT}}$ command signal must be issued after a high-to-low transition of the $\overline{\text{CONVERSION COMPLETE}}$, $\overline{\text{CC}}$, signal. Its duration depends on the time required by the digital time division switch circuitry to sample the 8-bit parallel transmit data bus.
5. Data conversion for a transmit operation is completed in 9 clock cycles because the SAR must be initialized before every new conversion. Data conversion for a receive operation corresponds to the Am6072 settling time; the receiving and transmit data transfers can be done simultaneously by employing separate transmit and receive data buses and utilizing data storage devices for the receive data.
6. A sample command pulse for a transmit operation can coincide with the $\overline{\text{START}}$ pulse; its duration depends on the sample and hold circuit used at the CODEC's analog input.
7. A sample command pulse for a receive operation must be delayed from a low-to-high transition of the RECEIVE command signal by an amount equal to the Am6072 settling time. Its termination can coincide with a high-to-low transition of the RECEIVE command signal.

TIME SHARED CONVERTER CONNECTIONS (Cont.)

SINGLE CHANNEL PCM CODEC – SERIAL DATA I/O

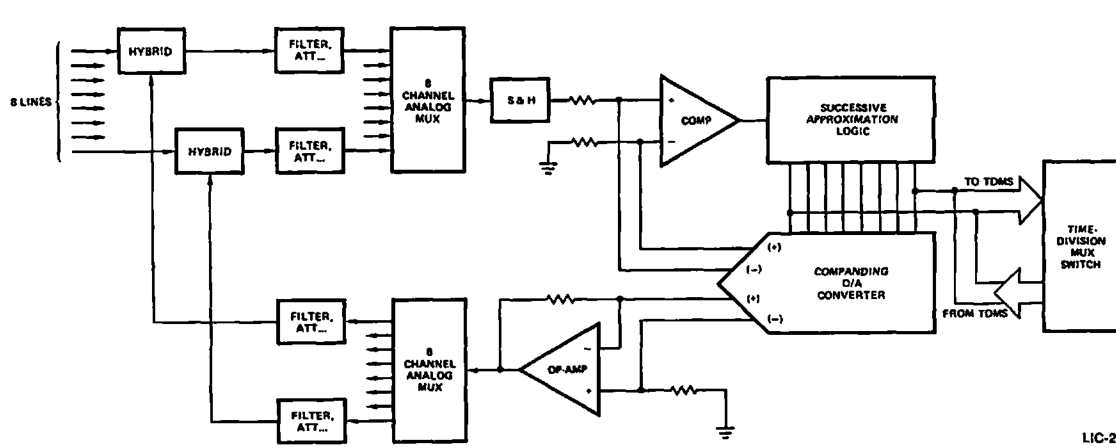


LIC-291

APPLICATION INFORMATION

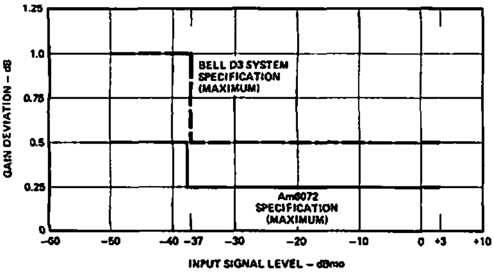
1. Before beginning either a transmit or a receive operation, the $\overline{\text{START}}$ signal must be held low for one complete clock cycle.
2. XMT and $\overline{\text{RECEIVE}}$ command signals are mutually exclusive. Their durations must accommodate the time required for conversion of an outgoing or an incoming series of 8 digital bits, respectively.
3. Data conversion for either operation, transmit or receive, is completed in 9 clock cycles.
4. During the receive cycle the successive approximation register, SAR, is acting as a serial-in to parallel-out shift register, with data supplied from data storage devices.
5. A sample command pulse for a transmit cycle must be issued before a XMT command signal; its duration depends on the sample and hold, S & H, circuit used.
6. A sample command pulse for a receive cycle must be delayed by a time equal to the Am6072 settling time after a high-to-low transition of the CONVERSION COMPLETE, $\overline{\text{CC}}$, signal occurs.

8 LINE CODEC TDM PCM/PABX SYSTEM – BLOCK DIAGRAM



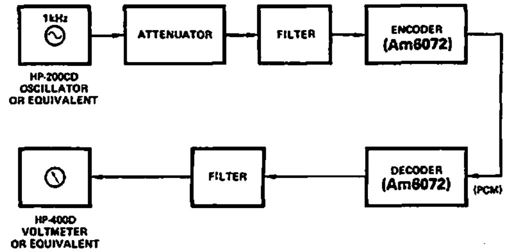
LIC-292

COMPANDOR TRACKING SPECIFICATION



LIC-293

COMPANDOR TRACKING TEST BLOCK DIAGRAM



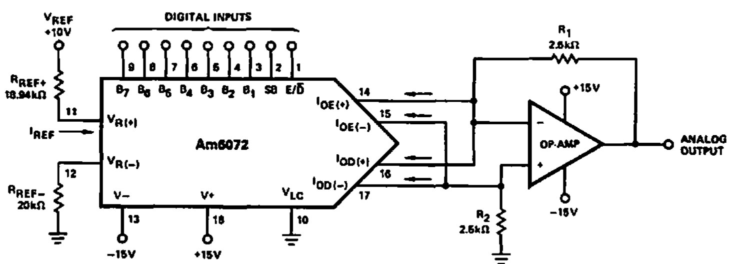
LIC-294

D3 NOISE AND DISTORTION SPECIFICATION

The Am6072 has a negligible idle channel noise contribution. Signal-to-quantizing-distortion ratio, (S/D), is guaranteed to exceed the minimum values specified for D3 channels as follows:

Input Level 1020 Hz Sinewave	S/D, C-Message Weighting
0 to –30 dBmo	33 dB
At –40 dBmo	27 dB
At –45 dBmo	22 dB

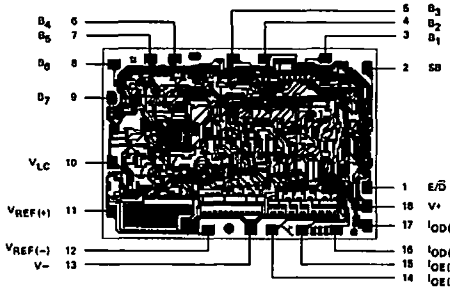
DECODER OPERATION DURING SIGNALLING FRAME



LIC-295

The Am6072 can perform the decoding function in a D3 channel bank system. During signalling frames the least significant bit, B7, of each 8-bit word is used for signalling messages and only seven bits are used for sample coding. In order to minimize the quantizing error during these signalling frames, the Am6072 output is increased by a half step from its corresponding decode output value by switching the E/D̄ input from a logic level 0 to a logic 1.

Metallization and Pad Layout



80 X 114 Mils

Am6073

Companding D-to-A Converter for PCM Communication Systems

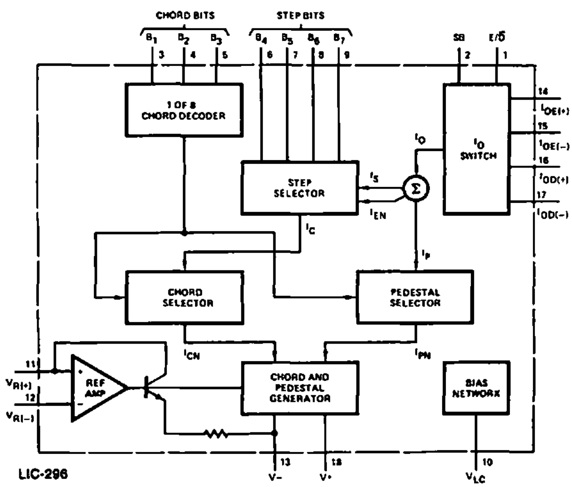
Distinctive Characteristics

- Tested to CCITT A-law tracking specification
- Absolute accuracy specified – includes all errors over temperature range
- Settling time 300ns typical
- Ideal for multiplexed PCM systems
- Output dynamic range of 62 dB
- Improved pin-for-pin replacement for DAC-87
- Microprocessor controlled operations
- Multiplying operation
- Negligible output noise
- Monotonicity guaranteed over entire dynamic range
- Wide output voltage compliance
- Low power consumption

GENERAL DESCRIPTION

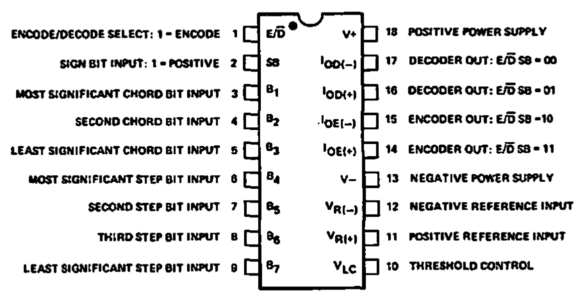
The Am6073 is a monolithic 8-bit, companding digital-to-analog (D/A) data converter with true current outputs and large output voltage compliance for fast driving a variety of loads. The transfer function of the Am6073 complies with the CCITT A-87.6 companding law, and consists of 13 linear segments or chords. A particular chord is identified with the sign bit input, (SB), and three chord select input bits. Each chord contains 16 uniformly spaced linear steps which are determined by four step select input bits. The resulting dynamic range achieved with this 8-bit format is 62dB. Accuracy and monoticity are assured by the internal circuit design and are guaranteed over the full temperature range. The Am6073 is tested to the CCITT A-law compandor tracking specification for pulse code modulation (PCM) transmission systems. The application of the Am6073 in communication systems provides an increased signal-to-noise ratio, reduces system signal distortion, and stimulates wider usage of computerized channel switching. Other application areas include digital audio recording, voice synthesis, and secure communications. When used in PCM communication systems, the Am6073 functions as a complete PCM decoder with additional encoding capabilities which make it ideal for implementation in CODEC circuits.

FUNCTIONAL BLOCK DIAGRAM



LIC-296

CONNECTION DIAGRAM
Am6073



Top View

Pin 1 is marked for orientation.

LIC-297

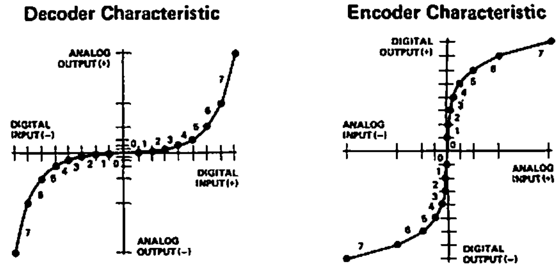
ORDERING INFORMATION

Part Number	Temperature	Accuracy
Am6073DM	−55°C to +125°C	Conforms to CCITT
Am6073DC	0°C to +70°C	A-law specification

Other AMD Companding D/A Converters	
Am6070DM, DC	Conforms to industrial μ-law spec.
Am6071DM, DC	Conforms to industrial A-law spec.
AM6072DM, DC	Conforms to Bell D3 spec.

SIMPLIFIED CONVERSION TRANSFER FUNCTIONS

Decoder Characteristic | Encoder Characteristic



LIC-298

MAXIMUM RATINGS above which useful life may be impaired

V+ Supply to V− Supply	36V	Operating Temperature	
V_{LC} Swing	V− plus 8V to V+	MIL Grade	−55°C to +125°C
Output Voltage Swing	V− plus 8V to V− plus 36V	COM'L Grade	0°C to +70°C
Reference Inputs	V− to V+	Storage Temperature	−65°C to +150°C
Reference Input Differential Voltage	±18V	Power Dissipation $T_A \leq 100°C$	500mW
Reference Input Current	1.25mA	For $T_A > 100°C$ derate at	10mW/°C
Logic Inputs	V− plus 8V to V− plus 36V	Lead Soldering Temperature	300°C (60 sec)

GUARANTEED FUNCTIONAL SPECIFICATIONS

Resolution	±128 Steps
Monotonicity	For both groups of 128 steps and over full operating temperature range
Dynamic Range	62 dB, (20 log ($I_{7,15}/I_{0,1}$))

ELECTRICAL CHARACTERISTICS (Note 1)

These specifications apply for $V_+ = +15V$, $V_- = -15V$, $I_{REF} = 512\mu A$, $0°C \leq T_A \leq +70°C$, for the commercial grade, $-55°C \leq T_A \leq +125°C$, *for the military grade*, and for all 4 outputs unless otherwise specified.

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_s	Settling Time	To within ±1/2 step at $T_A = 25°C$, Output switched from I_{ZS} to I_{FS}	–	300	500	ns
	Chord Endpoint Accuracy	$V_{REF} = +10.000V$ $R_{REF+} = 19.53k\Omega$ $R_{REF-} = 20k\Omega$ $-5V \leq V_{OUT} \leq +18V$	See Table 1 for absolute accuracy limits which cover all errors related to the transfer characteristic.			
	Step Nonlinearity					
I_{EN}	Encode Current					
$I_{FS}(D)$ $I_{FS}(E)$	Full Scale Current Deviation from Ideal					
$I_O(+) - I_O(-)$	Full Scale Current Symmetry Error Decode or Encode Pair					
I_{ZS}	Zero Scale Current					
ΔI_{FS}	Full Scale Current Drift					
V_{OC}	Output Voltage Compliance	Output within limits specified by Table 1	−5	–	+18	Volts
I_{DIS}	Disable Current	Leakage of output disabled by E/$\overline{D}$ or SB	–	5.0	50	nA
I_{FSR}	Output Current Range		0	2.0	4.2	mA
V_{IL}	Logic Input Levels, Logic "0"	$V_{LC} = 0V$	–	–	0.8	Volts
V_{IH}	Logic Input Levels, Logic "1"		2.0	–	–	Volts
I_{IN}	Logic Input Current	$V_{IN} = -5V$ to $+18V$	–	–	40	μA
V_{IS}	Logic Input Swing	$V- = -15V$	−5	–	+18	Volts
I_{BREF-}	Reference Bias Current		–	−1.0	−4.0	μA
dI/dt	Reference Input Slew Rate		0.12	0.25	–	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$V+ = +4.5$ to $+18V$, $V- = -15V$	–	0.005	0.1	dB
$PSSI_{FS-}$		$V- = -10.8V$ to $-18V$, $V+ = +15V$	–	0.01	0.1	
I+	Power Supply Current	$V+ = +5V$ to $+15V$, $V- = -15V$, $I_{PS} = 2.0mA$	–	2.7	4.0	mA
I−			–	−6.7	−8.8	
P_D	Power Dissipation	$V- = -15V$, $V_{OUT} = 0V$, $I_{FS} = 2.0mA$, $V+ = +5V$	–	114	152	mW
		$V+ = +15V$	–	141	192	

Note 1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) the step size is 1.0μA, while in the last chord near full scale (C_7) the step size is 64μA.

ELECTRICAL CHARACTERISTICS (Cont.)

TABLE I
ABSOLUTE DECODER OUTPUT CURRENT LEVELS IN μA

STEP	CHORD 0	1	2	3	4	5	6	7
0	.000 .500 1.000	16.032 16.500 16.982	32.064 33.000 33.964	64.127 66.000 67.927	128.25 132.00 135.85	256.51 264.00 271.71	513.02 528.00 543.42	1026.04 1056.00 1086.84
1	1.000 1.500 2.000	17.003 17.500 18.011	34.007 35.000 36.022	68.014 70.000 72.044	136.03 140.00 144.09	272.06 280.00 288.18	544.11 560.00 576.35	1088.22 1120.00 1152.70
2	2.103 2.500 2.971	17.975 18.500 19.040	35.950 37.000 38.080	71.900 74.000 76.161	143.80 148.00 152.32	287.60 296.00 304.64	575.20 592.00 609.29	1150.41 1184.00 1218.57
3	2.945 3.500 4.160	18.947 19.500 20.069	37.893 39.000 40.139	75.787 78.000 80.278	151.57 156.00 160.56	303.15 312.00 321.11	606.30 624.00 642.22	1212.59 1248.00 1284.44
4	4.248 4.500 4.767	19.918 20.500 21.099	39.837 41.000 42.197	79.673 82.000 84.394	159.35 164.00 168.79	318.69 328.00 337.58	637.39 656.00 675.16	1274.78 1312.00 1350.31
5	5.192 5.500 5.828	20.890 21.500 22.128	41.780 43.000 44.256	83.560 86.000 88.511	167.12 172.00 177.02	334.24 344.00 354.04	668.48 688.00 708.09	1336.96 1376.00 1416.18
6	6.136 6.500 6.885	21.862 22.500 23.157	43.723 45.000 46.314	87.447 90.000 92.628	174.89 180.00 185.26	349.79 360.00 370.51	699.57 720.00 741.02	1399.14 1440.00 1482.05
7	7.080 7.500 7.944	22.833 23.500 24.186	45.667 47.000 48.372	91.333 94.000 96.745	182.67 188.00 193.49	365.33 376.00 386.98	730.66 752.00 773.96	1461.33 1504.00 1547.92
8	8.025 8.500 9.004	23.805 24.500 25.215	47.610 49.000 50.431	95.220 98.000 100.862	190.44 196.00 201.72	380.88 392.00 403.45	761.76 784.00 806.89	1523.61 1568.00 1613.79
9	8.969 9.500 10.063	24.777 25.500 26.245	49.553 51.000 52.489	99.106 102.000 104.978	198.21 204.00 209.96	396.42 408.00 419.91	792.85 816.00 839.83	1585.70 1632.00 1679.66
10	9.913 10.500 11.122	25.748 26.500 27.274	51.496 53.000 54.548	102.993 106.000 109.095	205.99 212.00 218.19	411.97 424.00 436.38	823.94 848.00 872.76	1647.88 1696.00 1745.52
11	10.857 11.500 12.181	26.720 27.500 28.303	53.440 55.000 56.606	106.879 110.000 113.212	213.76 220.00 226.42	427.52 440.00 452.85	855.03 880.00 905.70	1710.07 1760.00 1811.39
12	11.801 12.500 13.241	27.691 28.500 29.332	55.383 57.000 58.664	110.766 114.000 117.329	221.53 228.00 234.66	443.06 456.00 469.32	886.12 912.00 938.63	1722.26 1824.00 1877.26
13	12.745 13.500 13.894	28.663 29.500 30.361	57.326 59.000 60.723	114.652 118.000 121.446	229.30 236.00 242.89	458.61 472.00 485.78	917.22 944.00 971.57	1834.43 1888.00 1943.13
14	14.069 14.500 14.923	29.635 30.500 31.391	59.269 61.000 62.781	118.539 122.000 125.562	237.08 244.00 251.12	474.15 488.00 502.25	948.31 976.00 1004.50	1896.62 1952.00 2009.00
15	15.060 15.500 15.953	30.608 31.500 32.420	61.231 63.000 64.840	122.425 126.000 129.679	244.85 252.00 259.36	489.70 504.00 518.72	979.40 1008.00 1037.43	1958.80 2016.00 2074.87
STEP SIZE	1	1	2	4	8	16	32	64

Minimum, ideal and maximum values are specified for each step. The minimum and maximum values are specified to comply with the CCITT A-law compandor tracking requirements. All four outputs are guaranteed, the encode outputs being specified to limits a half step higher than those shown above. This takes into account the combined effects of chord endpoint accuracy, step nonlinearity, encode current error, full scale current deviation from ideal, full scale symmetry error, zero scale current, full scale drift, and output impedance over the specified output voltage compliance range. Note that the guaranteed monotonicity ensures that adjacent step current levels will not overlap as might otherwise be implied from the minimum and maximum values shown in the above table.

TABLE 2
IDEAL DECODER OUTPUT VALUES EXPRESSED IN dB DOWN FROM OVERLOAD LEVEL (+3dBmo)

STEP	CHORD 0	1	2	3	4	5	6	7
0	−69.11	−38.74	−35.72	−26.70	−20.68	−14.66	−8.64	−2.62
1	−59.57	−38.23	−32.21	−26.19	−20.17	−14.15	−8.13	−2.11
2	−55.13	−37.75	−31.73	−25.71	−19.68	−13.66	−7.64	−1.62
3	−52.21	−37.29	−31.27	−25.25	−19.23	−13.21	−7.19	−1.17
4	−50.03	−36.85	−30.83	−24.81	−18.79	−12.77	−6.75	−0.73
5	−48.28	−36.44	−30.42	−24.40	−18.38	−12.36	−6.34	−0.32
6	−46.83	−36.05	−30.03	−24.00	−17.98	−11.96	−5.94	+0.08
7	−45.59	−35.67	−29.65	−23.63	−17.61	−11.59	−5.57	+0.46
8	−44.50	−35.31	−29.29	−23.27	−17.24	−11.22	−5.20	+0.82
9	−43.54	−34.96	−28.94	−22.92	−16.90	−10.88	−4.86	+1.18
10	−42.67	−34.62	−28.60	−22.58	−16.56	−10.54	−4.52	+1.50
11	−41.88	−34.30	−28.28	−22.26	−16.24	−10.22	−4.20	+1.82
12	−41.15	−33.99	−27.97	−21.95	−15.93	−9.91	−3.89	+2.13
13	−40.48	−33.69	−27.67	−21.65	−15.63	−9.61	−3.59	+2.43
14	−39.86	−33.40	−27.38	−21.36	−15.34	−9.32	−3.30	+2.72
15	−39.28	−33.12	−27.10	−21.08	−15.06	−9.04	−3.02	+3.00

The −40dBmo, −50dBmo, and −55dBmo output points significant for the CCITT A-87.6 PCM system specification can be found between steps 13 and 14 on chord 0, steps 4 and 5 on chord 0, and steps 2 and 3 on chord 0, respectively. Outputs corresponding to points below −55dBmo are specified in Table 1 for an accuracy of ± a half step.

THEORY OF OPERATION

Functional Description

The Am6073 is an 8-bit, nonlinear, digital-to-analog converter with high impedance current outputs. The output current value is proportional to the product of the digital inputs and the input reference current. The full scale output current, I_{FS}, is specified by the input binary code 111 1111, and is a linear function of the reference current, i_{REF}. There are two operating modes, encode and decode, which are controlled by the Encode/Decode, ($E/\overline{D}$), input signal. A logic 1 applied to the $E/\overline{D}$ input places the Am6073 in the encode mode and current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output, depending on the state of the Sign Bit (SB) input. A logic 0 at the $E/\overline{D}$ input *places the Am6073* in the decode mode.

The transfer characteristic is a piece-wise linear approximation to the CCITT A-87.6 logarithmic law which can be written as follows:

$$Y = 0.18\ (1 + \ln (A\,|X|\,))\ \mathrm{sgn}\ (X),\quad 1/A \leq |X| \leq 1$$

$$Y = 0.18\ (A\,|X|\,)\ \mathrm{sgn}\ (X),\quad 0 \leq |X| \leq 1/A$$

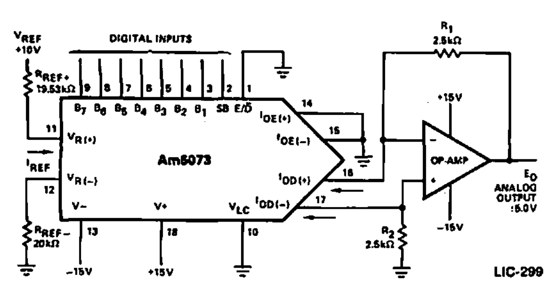
where: X = analog signal level normalized to unity (encoder input or decoder output)
Y = digital signal level normalized to unity (encoder output or decoder input)
A = 87.6

The current flows from the external circuit into one of four possible analog outputs determined by the SB and $E/\overline{D}$ inputs. The output current transfer function can be represented by a total of 16 segments or chords addressable through the SB input and three chord select bits. The two chords closest to the origin of the transfer function, chord 0 and chord 1, are made colinear and contiguous. The beginning of chord 0, specified by the input binary code 000 0000, is offset by $+0.5\mu A$. Each chord can be further divided into 16 steps, all of the same size. The step size changes from one chord to another, with the smallest step of $1.0\mu A$ found in the first two chords near zero output current, and the largest step of $64\mu A$ found in the last chord near full scale output current. This nonlinear feature provides exceptional accuracy for small signal levels. The accuracy for signal amplitudes corresponding to chords 0 and 1 is very close to that of an 11-bit linear, binary D/A converter. The ratio (in dB) between the chord endpoint current, (Step 15), and the current which corresponds to the preceding step, (Step 14), is maintained at about 0.3dB over the entire dynamic range, with the exception of chord 0. The difference between the ratios of full scale current to chord endpoint currents of adjacent chords is similarly maintained at 6dB over the entire dynamic range. Resulting signal-to-quantizing distortions due to non-uniform quantizing levels maintain an acceptably low value over a 40dB range of input speech signals. Note that the 62dB output dynamic range for the Am6073 is very close to the dynamic range of a sign plus 11-bit linear, binary D/A converter.

In order to achieve a smoother transition between adjacent chords, the step size between these chord end points is equal to 1.5 times the step size of the lower chord. Note that this does not apply to chord 0 and chord 1 where adjacent end points differ by only one step, because these two chords are colinear and have the same step sizes. Monotonic operation is guaranteed by the internal device design over the entire output dynamic range by specifying and maintaining the chord end points and step size deviations within the allowable limits.

Operating Modes

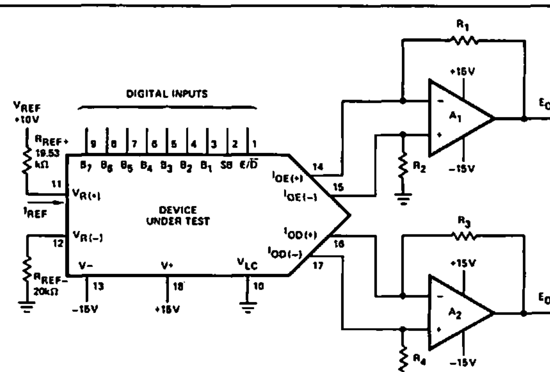
The basic converter function is conversion of digital input data into a corresponding analog current signal, i.e., the basic function is digital-to-analog decoding. The basic decoder connection for a sign plus 7-bit input configuration is shown in Figure 1. The corresponding dynamic range is 62dB, and input-output characteristics conform to the standard decoder transfer function with output current values specified in Table 1. The $E/\overline{D}$ input enables switching between the encode, $I_{OE(+)}$ or $I_{OE(-)}$, and the decode, $I_{OD(+)}$ or $I_{OD(-)}$, outputs. A typical encode/decode test circuit is shown in Figure 2. This circuit is used for output current measurements. When the $E/\overline{D}$ input is high, (a logic 1), the converter will assume the encode operating mode and the output current will flow into one of the I_{OE} outputs (as determined by the SB input). When operating in the encode mode as shown



$I_{REF} = V_{REF}/R_{REF}$
IDEAL VALUES: $I_{REF} = 512\mu A$, $I_{FS} = 2016\mu A$

	$E/\overline{D}$	SB	B_1	B_2	B_3	B_4	B_5	B_6	B_7	E_O
POSITIVE FULL SCALE	0	1	1	1	1	1	1	1	1	5.040V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.004V
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0.0012V
(−) ZERO SCALE	0	0	0	0	0	0	0	0	0	−0.0012V
(−) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	−0.004V
NEGATIVE FULL SCALE	0	0	1	1	1	1	1	1	1	−5.040V

Figure 1. Detailed Decoder Connections.



$R_1 = R_2 = R_3 = R_4 = 2.5k\Omega \pm 0.1\%$ LIC-300

LINE SELECTION TABLE

TEST GROUP	$E/\overline{D}$	SB	OUTPUT MEASUREMENT	
1	1	1	I_{OE} (+)	(E_{O1}/R_1)
2	1	0	I_{OE} (−)	(E_{O1}/R_2)
3	0	1	I_{OD} (+)	(E_{O2}/R_3)
4	0	0	I_{OD} (−)	(E_{O2}/R_4)

Figure 2. Output Current DC Test Circuit.

in Figure 3, an offset current equal to a half step in each chord is required to obtain the correct encoder transfer characteristic. Since the size of this step varies from one chord to another, it cannot easily be added externally. As indicated in the block diagram this required half step of encode current, I_{EN}, is automatically added to the I_{OE} output through the internal chip design. This additional current will, for example, make the ideal full scale current in the encode mode larger than the same current in the decode mode by 32μA. Similarly, the current levels in the first chord near the origin will be offset by 0.5μA, which will bring the ideal encode current value for step 0 on chord 0 to $\pm$1.0μA with respect to the corresponding decode current value of 0.5μA. This additional encode half step of current can be used for extension of the output dynamic range from 62dB to 66dB, when the converter is performing only the decode function. The corresponding decoder connection utilizes the E/$\overline{D}$ input as a ninth digital input and has the outputs $I_{OD(+)}$ and $I_{OE(+)}$ and the outputs $I_{OD(-)}$ and $I_{OE(-)}$ tied together, respectively.

When encoding or compression of an analog signal is required, the Am6072 can be used together with a Successive Approximation Register (SAR), comparator, and additional SSI logic elements to perform the A/D data conversion, as shown in Figure 3. The encoder transfer function, shown on page 1, characterizes this A/D converter system. The first task of this system is to determine the polarity of the incoming analog signal and to generate a corresponding SB input value. When the proper $\overline{\text{START}}$, ($\overline{\text{S}}$), and $\overline{\text{CONVERSION COMPLETE}}$, ($\overline{\text{CC}}$), signal levels are set, the first clock pulse sets the MSB output of the SAR, Am2502, to a logic 0 and sets all other parallel digital outputs to logic 1 levels. At the same time, the flip-flop is triggered, and its output provides the E/$\overline{D}$ input with a logic 0 level. No current flows into the I_{OE} outputs. This disconnects the converter from the comparator inputs, and the incoming analog signal can be compared with the ground applied to the opposite comparator input. The resulting comparator output is fed to the Am2502 serial data input, D, through an exclusive-or gate. At the same time, the second input to the same exclusive-or gate is held at a logic 0 level by the additional successive approximation logic shown in Figure 3. This exclusive-or gate inverts the comparator's outputs whenever a negative signal polarity is detected. This maintains the proper output current coding, i.e., all ones for full scale and all zeros for zero scale.

The second clock pulse changes the E/$\overline{D}$ input back to a logic 1 level because the $\overline{\text{CC}}$ signal changed. It also clocks the D input signal of the Am2502 to its MSB output, and transfers it to the SB input of the Am6073. Depending upon the SB input level, current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output of the Am6073.

Nine clock pulses are required to obtain a digital binary representation of the incoming analog signal at the eight Am2502 digital outputs. The resulting Am6073 analog output signal is compared with the analog input signal after each of the nine successive clock pulses. The analog signal should not be allowed to change its value during the data conversion time. In high speed systems, fast changes of the analog signals at the A/D system input are usually prevented by using sample and hold circuitry.

Additional Considerations and Recommendations

In Figure 1, an optional operational amplifier converts the Am6073 output current to a bipolar voltage output. When the SB input is a logic 1, sink current appears at the amplifier's negative input, and the amplifier acts as a current to voltage converter, yielding a positive voltage output. With the SB value at a logic 0, sink current appears at the amplifier's positive input. The amplifier behaves as a voltage follower, and the true current outputs will swing below ground with essentially no change in output current. The SB input steers current into the appropriate (+) or (−) output of the Am6073. The resulting operational amplifier's output in Figure 1 should ideally be symmetrical with resistors R1 and R2 matched.

In Figure 2, two operational amplifiers measure the currents of each of the four Am6073 analog outputs. Resistor tolerances of 0.1% give 0.1% output measurement error (approximately 2μA at full scale). The input offset currents of the A1 and A2 devices also increase output measurement error and this error is most significant near zero scale. The Am101A and 308 devices, for example, may be used for A1 and A2 since their maximum offset currents, which would add directly to the measurement error, are only 10nA and 1nA respectively. The input offset voltages of the A1 and A2 devices, with output resistor values of 2.5kΩ, also contribute to the output measurement error by a factor of 400nA for

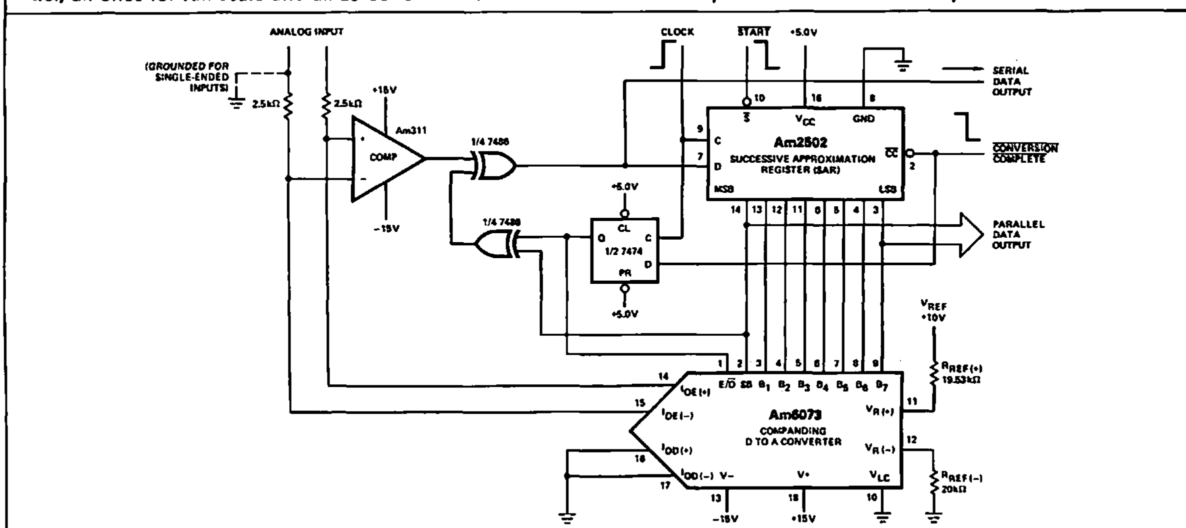


Figure 3. Detailed Encoder Connections.

LIC-301

every mV of offset at the A1 and A2 outputs. Therefore, to minimize error, the offset voltages of A1 and A2 should be nulled.

The recommended operating range for the reference current I_{REF} is from 0.1mA to 1.0mA. The full scale output current, I_{FS}, is a linear function of the reference current, and may be calculated from the equation $I_{FS} = 3.94\ I_{REF}$. This tight relationship between I_{REF} and I_{FS} alleviates the requirement for trimming the I_{REF} current if the R_{REF} resistor values are within ±1% of the calculated value. Lower values of I_{REF} will reduce the negative power supply current, (I−), and will increase the reference amplifier negative common mode input voltage range.

The ideal value for the reference current $I_{REF} = V_{REF}/R_{REF}$ is 512μA. The corresponding ideal full scale decode and encode current values are 2016μA and 2048μA, respectively. A percentage change from the ideal I_{REF} value produced by changes in V_{REF} or R_{REF} values produces the same percentage change in decode and encode output current values. The positive voltage supply, V+, may be used, with certain precautions, for the positive reference voltage V_{REF}. In this case, the reference resistor $R_{REF(+)}$ should be split into two resistors and their junction bypassed to ground with a capacitor of 0.01μF. The total resistor value should provide the reference current $I_{REF} = 512\mu A$. The resistor $R_{REF(-)}$ value should be approximately equal to the $R_{REF(+)}$ value in order to compensate for the errors caused by the reference amplifier's input offset current.

An alternative to the positive reference voltage applications shown in Figures 1, 2 and 3 is the application of a negative voltage to the $V_{R(-)}$ terminal through the resistor $R_{REF(-)}$ with the $R_{REF(+)}$ resistor tied to ground. The advantage of this arrangement is the presence of very high impedance at the $V_{R(-)}$ terminal while the reference current flows from ground through $R_{REF(+)}$ into the $V_{R(+)}$ terminal.

The Am6073 has a wide output voltage compliance suitable for driving a variety of loads. With $I_{REF} = 512\mu A$ and V− = −15V, positive voltage compliance is +18V and negative voltage compliance is −5.0V. For other values of I_{REF} and V−, the negative voltage compliance, $V_{OC(-)}$, may be calculated as follows:

$$V_{OC(-)} = (V-) + 2(I_{REF} \cdot 1.55k\Omega) + 8.4V,$$

where 1.55kΩ and 8.4V are equivalent worst case values for the Am6073.

The following table contains $V_{OC(-)}$ values for some specific V−, I_{REF}, and I_{FS} values.

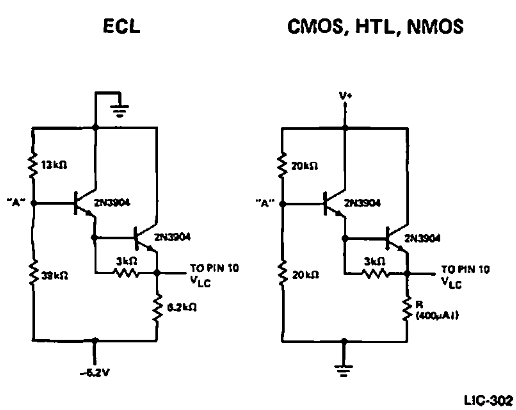
Negative Output Voltage Compliance $V_{OC(-)}$

V−	I_{REF} (I_{FS})		
	256μA (1mA)	512μA (2mA)	1024μA (4mA)
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

The V_{LC} input can accommodate various logic input switching threshold voltages allowing the Am6073 to interface with various logic families. This input should be placed at a potential which is 1.4V below the desired logic input switching threshold. Two external discrete circuits which provide this function for non-TTL driven inputs are shown in Figure 4. For TTL-driven logic inputs, the V_{LC} input should be grounded. If negative voltages are applied at the digital logic inputs, they must have a value which is more positive than the sum of the chosen V− value and +10V.

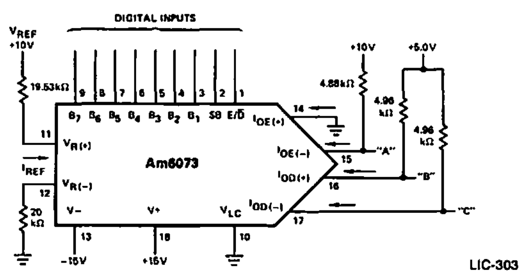
With a V− value chosen between −15V and −11V, the $V_{OC(-)}$, the input reference common mode voltage range, and the logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− value chosen.

With a V+ value chosen between +5V and +15V, the reference amplifier common mode positive voltage range and the V_{LC} input values are reduced by an amount equivalent to the difference between +15V and the V+ value chosen.



(See Notes 2 and 3)

Figure 4. Interfacing Circuits for ECL, CMOS, HTL, and NMOS Logic Inputs.



INPUT CODE (E/D̄, SB, B_1, . . ., B_7)	OUTPUT VOLTAGE (V) "A"	"B"	"C"	DIFF
10 111 1111	0			
10 110 1111	+5.00	N/A	N/A	N/A
10 000 0000	+10.00			
01 111 1111		−5.00	+5.00	−10.00
01 110 1111		+0.00	+5.00	−5.00
01 000 0000	N/A	+5.00	+5.00	0
00 000 0000		+5.00	+5.00	0
00 110 1111		+5.00	+0.00	+5.00
00 111 1111		+5.00	−5.00	+10.00

Figure 5. Resistive Output Connections.

Notes: 2. Set the voltage "A" to the desired logic input switching threshold.
3. Allowable range of logic threshold is typically −5V to +13.5V when operating the companding DAC on ±15V supplies.

ADDITIONAL DECODE OUTPUT CURRENT TABLES

Table 3
Normalized Decoder Output (Sign Bit Excluded)

STEP (S)		CHORD (C) 0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	33	66	132	264	528	1056	2112
1	0001	3	35	70	140	280	560	1120	2240
2	0010	5	37	74	148	296	592	1184	2368
3	0011	7	39	78	156	312	624	1248	2496
4	0100	9	41	82	164	328	656	1312	2624
5	0101	11	43	86	172	344	688	1376	2752
6	0110	13	45	90	180	360	720	1440	2880
7	0111	15	47	94	188	376	752	1504	3008
8	1000	17	49	98	196	392	784	1568	3136
9	1001	19	51	102	204	408	816	1632	3264
10	1010	21	53	106	212	424	848	1696	3392
11	1011	23	55	110	220	440	880	1760	3520
12	1100	25	57	114	228	456	912	1824	3648
13	1101	27	59	118	236	462	944	1888	3776
14	1110	29	61	122	244	488	976	1952	3904
15	1111	31	63	126	252	504	1008	2016	4032
STEP SIZE		2	2	4	8	16	32	64	128

The normalized decode current, ($I_{C,S}$), where C is chord number and S is step number, is calculated using: $I_{CS} = 2^C(S + 16.5)$ for $C \geqslant 1$, and $I_{C,S} = 2S + 1$ for $C = 0$. The ideal decode current, (I_{OD}), in μA is calculated using: $I_{OD} = (I_{C,S}/I_{7,15(norm.)}) \bullet I_{FS}(\mu A)$, where $I_{C,S}$ is the corresponding normalized current. To obtain normalized encode values the corresponding normalized half-step value should be added to all entries in Table 3.

Table 4
Decoder Step Size Summary

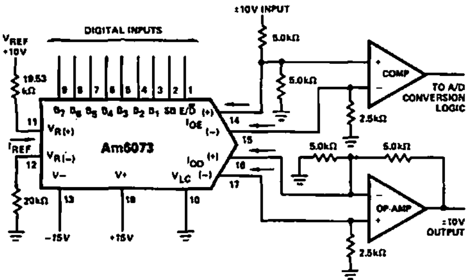
Chord	Step Size Normalized to Full Scale	Step Size in μA with 2016μA F. S.	Step Size as a % of Full Scale	Step Size in dB at Chord Endpoints	Step Size as a % of Reading at Chord Endpoints	Resolution & Accuracy of Equivalent Binary DAC
0	2	1.0	0.05%	0.58	6.45%	Sign + 11 Bits
1	2	1.0	0.05%	0.28	3.17%	Sign + 11 Bits
2	4	2.0	0.1%	0.28	3.17%	Sign + 10 Bits
3	8	4.0	0.2%	0.28	3.17%	Sign + 9 Bits
4	16	8.0	0.4%	0.28	3.17%	Sign + 8 Bits
5	32	16.0	0.8%	0.28	3.17%	Sign + 7 Bits
6	64	32.0	1.6%	0.28	3.17%	Sign + 6 Bits
7	128	64.0	3.2%	0.28	3.17%	Sign + 5 Bits

Table 5
Decoder Chord Size Summary

Chord	Chord Endpoints Normalized to Full Scale	Chord Endpoints in μA with 2016μA F. S.	Chord Endpoints as a % of Full Scale	Chord Endpoints in dB Down from Full Scale
0	31	15.5	0.77%	−42.28
1	63	31.5	1.56%	−36.12
2	126	63.0	3.13%	−30.10
3	252	126.0	6.25%	−24.08
4	504	252.0	12.5%	−18.06
5	1008	504.0	25.0%	−12.04
6	2016	1008.0	50.0%	−6.02
7	4032	2016.0	100%	0

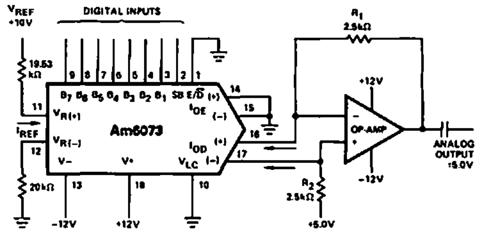
BASIC CIRCUIT CONNECTIONS

±10V RANGE ENCODER/DECODER CONNECTIONS



LIC-304

COMPLIANCE EXTENSION USING AC COUPLED OUTPUT



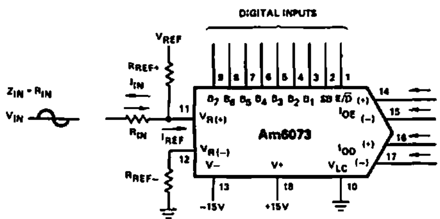
IDEAL VALUES:

$I_{REF} = 512\mu A$

$I_{FS} = 2016\mu A$

LIC-305

LOW INPUT IMPEDANCE CONNECTION



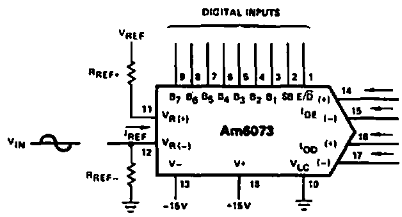
$I_{REF} = V_{IN}/R_{IN} + V_{REF}/R_{REF+}$

$I_{FS} \approx 4(I_{REF})$

$R_{REF-} = [(R_{REF+})(R_{IN})]/(R_{REF+} + R_{IN})$

LIC-306

HIGH INPUT IMPEDANCE CONNECTION

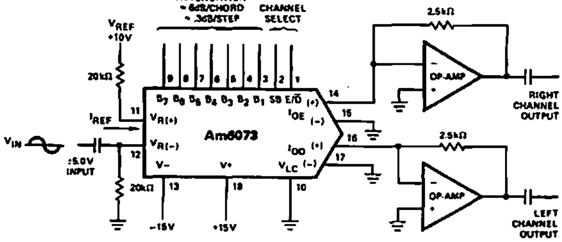


$I_{REF} = (V_{REF} - V_{IN})/R_{REF+}$

$I_{FS} \approx 4(I_{REF})$

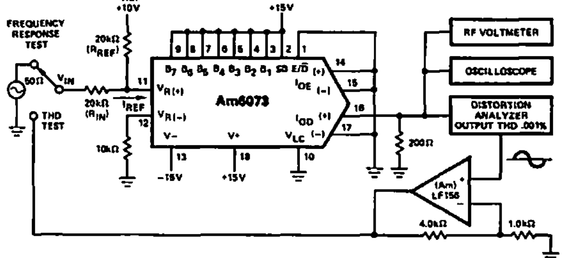
LIC-307

LOGARITHMIC DIGITAL GAIN CONTROL (Notes 4, 5)



LIC-308

REFERENCE AMPLIFIER DYNAMIC TEST CIRCUIT



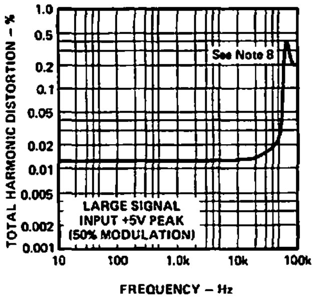
LIC-309

Notes: 4. Low distortion outputs are provided over 62dB range.

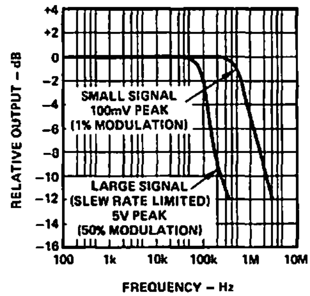
5. Up to 4 channels of output may be selected by E/$\overline{D}$ and SB logic inputs.

TYPICAL PERFORMANCE CURVES

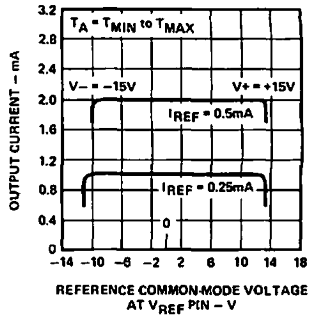
Reference Amplifier Total Harmonic Distortion Versus Frequency (80kHz Filter) (Notes 6, 7, 8)



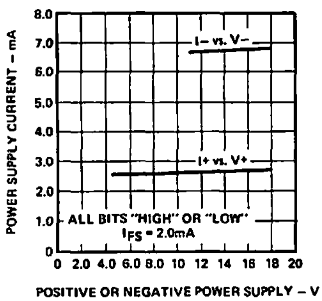
Reference Amplifier Input Frequency Response



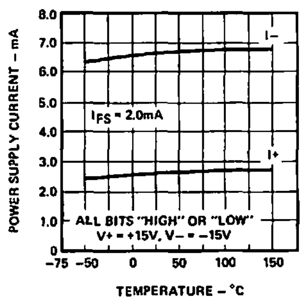
Reference Amplifier Input Common-Mode Range (Note 9)



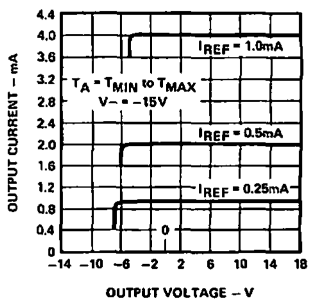
Power Supply Currents Versus Power Supply Voltages



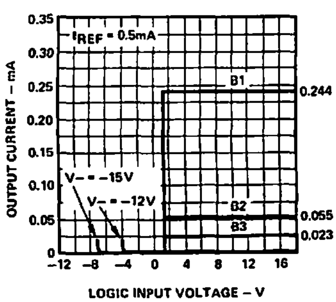
Power Supply Currents Versus Temperature



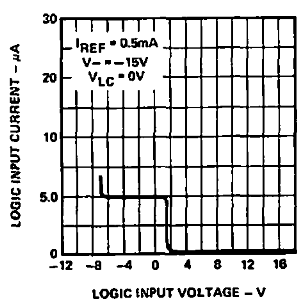
Output Current Versus Output Voltage (Output Voltage Compliance)



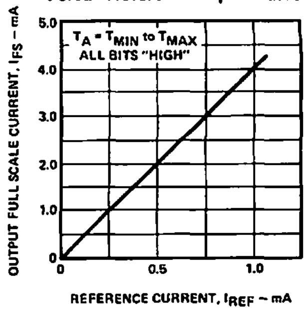
Bit Transfer Characteristics (Note 10)



Logic Input Current Versus Input Voltage and Logic Input Range (Note 11)



Output Full Scale Current Versus Reference Input Current

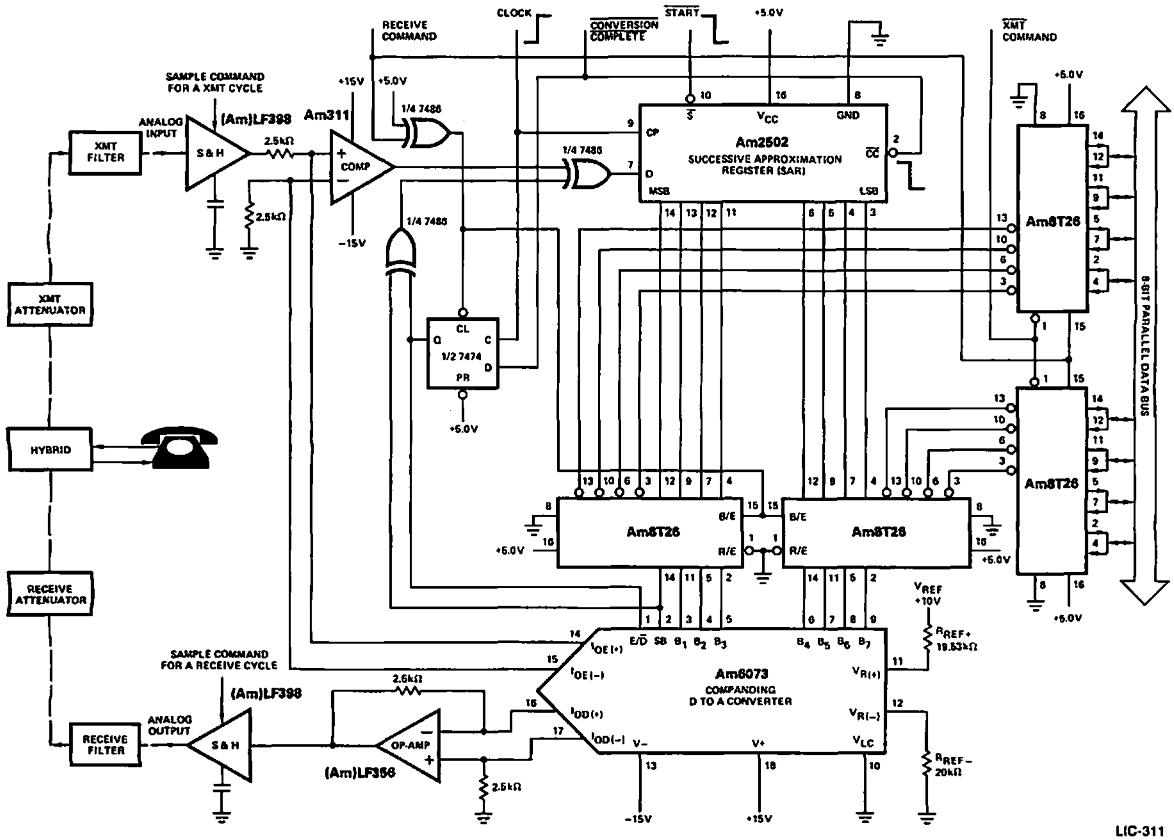


LIC-310

Notes:
6. THD is nearly independent of the logic input code.
7. Similar results are obtained for a high input impedance connection using $V_{R(-)}$ as an input.
8. Increased distortion above 50kHz is due to a slew rate limiting effect which determines the large signal bandwidth. For an input of ±2.5V peak (25% modulation), the bandwidth is 100kHz.
9. Positive common mode range is always (V+) −1.5V.
10. All bits are fully switched with less than a half step error at switching points which are guaranteed to lie between 0.8V and 2.0V over the operating temperature range.
11. The logic input voltage range is independent of the positive power supply and logic inputs may swing above the supply.

TIME SHARED CONVERTER CONNECTIONS

SINGLE CHANNEL PCM CODEC – PARALLEL DATA I/O

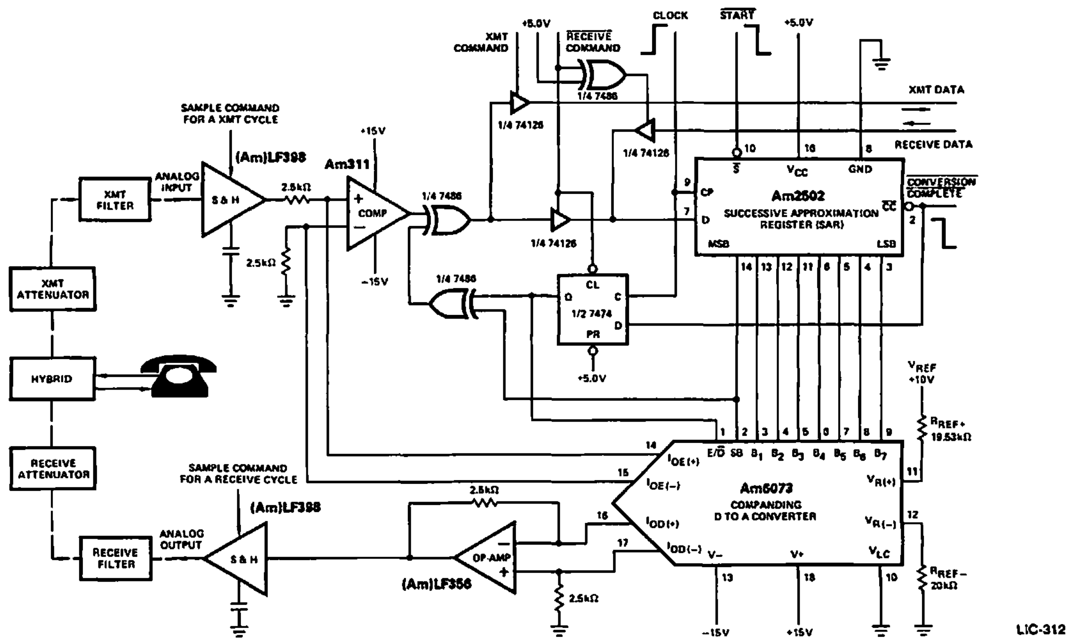


APPLICATION INFORMATION

1. To perform a transmit operation cycle the $\overline{\text{START}}$ pulse must be held low for one clock cycle; the receive operation is performed without the successive approximation register, SAR.
2. $\overline{\text{XMT}}$ and RECEIVE command signals are mutually exclusive.
3. Duration of the RECEIVE command signal must accommodate the Am6073 settling time plus the sampling time required by the sample and hold, (S & H), circuit used at the CODEC's analog output. The receiving data must not change during this time.
4. A $\overline{\text{XMT}}$ command signal must be issued after a high-to-low transition of the $\overline{\text{CONVERSION COMPLETE}}$, $\overline{\text{CC}}$, signal. Its duration depends on the time required by the digital time division switch circuitry to sample the 8-bit parallel transmit data bus.
5. Data conversion for a transmit operation is completed in 9 clock cycles because the SAR must be initialized before every new conversion. Data conversion for a receive operation corresponds to the Am6073 settling time; the receiving and transmit data transfers can be done simultaneously by employing separate transmit and receive data buses and utilizing data storage devices for the receive data.
6. A sample command pulse for a transmit operation can coincide with the $\overline{\text{START}}$ pulse; its duration depends on the sample and hold circuit used at the CODEC's analog input.
7. A sample command pulse for a receive operation must be delayed from a low-to-high transition of the RECEIVE command signal by an amount equal to the Am6073 settling time. Its termination can coincide with a high-to-low transition of the RECEIVE command signal.
8. The code assignment for outgoing or incoming parallel data provides uncomplemented binary values for signal sign and magnitude. The data bus, as a result, yields "high zeros" density for small signal amplitudes.

TIME SHARED CONVERTER CONNECTIONS (Cont.)

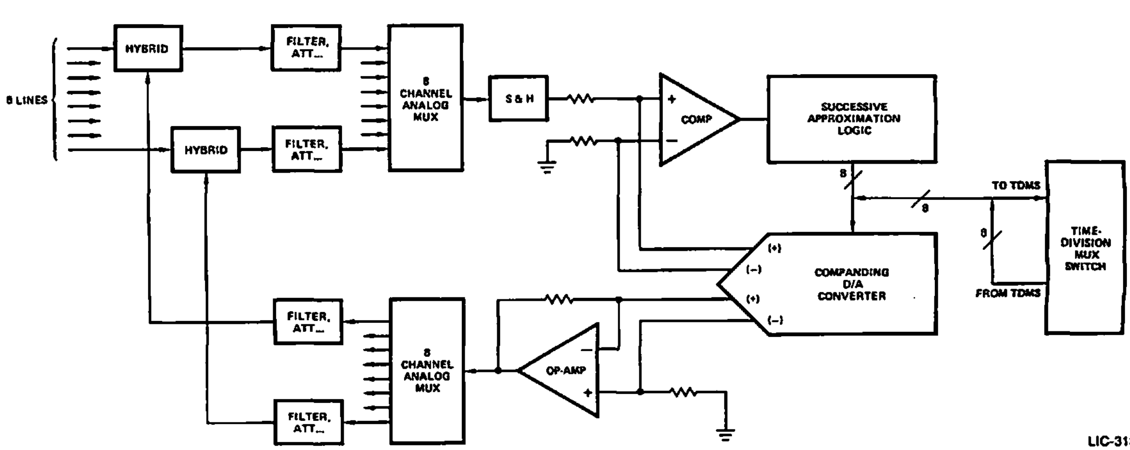
SINGLE CHANNEL PCM CODEC – SERIAL DATA I/O



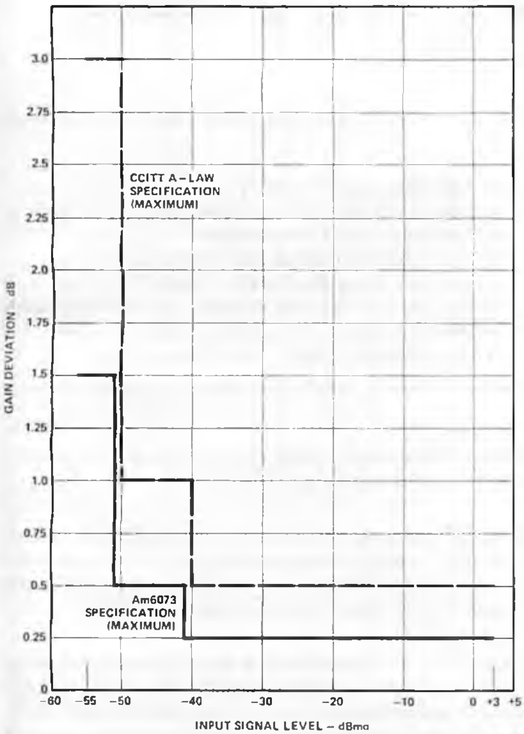
APPLICATION INFORMATION

1. Before beginning either a transmit or a receive operation, the START signal must be held low for one complete clock cycle.
2. XMT and RECEIVE command signals are mutually exclusive. Their durations must accommodate the time required for conversion of an outgoing or an incoming series of 8 digital bits, respectively.
3. Data conversion for either operation, transmit or receive, is completed in 9 clock cycles.
4. During the receive cycle the successive approximation register, SAR, is acting as a serial-in to parallel-out shift register, with data supplied from data storage devices.
5. A sample command pulse for a transmit cycle must be issued before a XMT command signal; its duration depends on the sample and hold, S & H, circuit used.
6. A sample command pulse for a receive cycle must be delayed by a time equal to the Am6073 settling time after a high-to-low transition of the CONVERSION COMPLETE, CC, signal occurs.
7. The code assignment for outgoing or incoming parallel data provides uncomplemented binary values for signal sign and magnitude. The data bus, as a result, yields "high zeros" density for small signal amplitudes.

8 LINE CODEC TDM PCM/PABX SYSTEM – BLOCK DIAGRAM

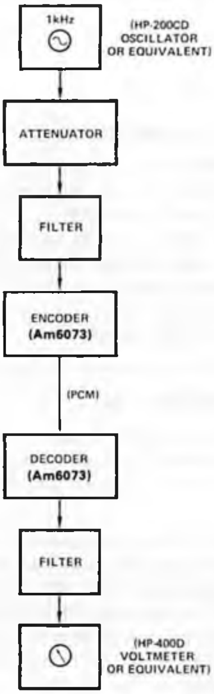


CCITT A–LAW COMPANDOR TRACKING SPECIFICATION



LIC-314

COMPANDOR TRACKING TEST BLOCK DIAGRAM



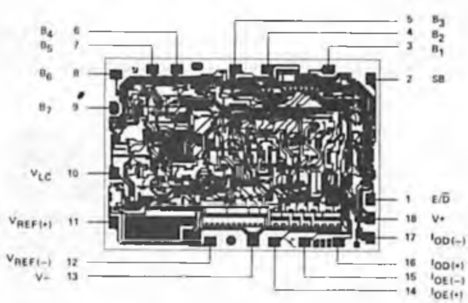
LIC-315

CCITT NOISE AND DISTORTION SPECIFICATION

The Am6073 has a negligible idle channel noise contribution. Signal-to-quantizing-distortion ratio, (S/D), is guaranteed to exceed the minimum values specified for PCM channels at audio frequencies as follows:

Input Level 1020 Hz Sinewave	S/D, C-Message Weighting
0 to –30 dBmo	33 dB
At –40 dBmo	27 dB
At –45 dBmo	22 dB

Metallization and Pad Layout



80 X 114 Mils

Am6080

Microprocessor System Compatible 8-Bit High Speed Multiplying D/A Converter

DISTINCTIVE CHARACTERISTICS

- 8-Bit D/A with 8-Bit input data latch
- Compatible with most popular microprocessors including the Am9080A-4 and the Am2900
- Write, Chip Select and Data Enable logic on chip
- DAC appears as memory location to microprocessor
- MSB inversion under logic control
- Differential current output
- Choice of 6 coding formats
- Fast settling current output −160ns
- Nonlinearity to ±0.1% max over temperature range
- Full scale current pre-matched to ±1 LSB
- High output impedance and voltage compliance
- Low full scale current drift − ±5ppm/°C
- Wide range multiplying capability −2.0MHz bandwidth
- Direct interface to TTL, CMOS, NMOS
- High speed data latch − 80ns min write time

GENERAL DESCRIPTION

The Am6080 is a monolithic 8-bit multiplying Digital-to-Analog converter with an 8-bit data latch, chip select and other control signal lines which allow direct interface with microprocessor buses.

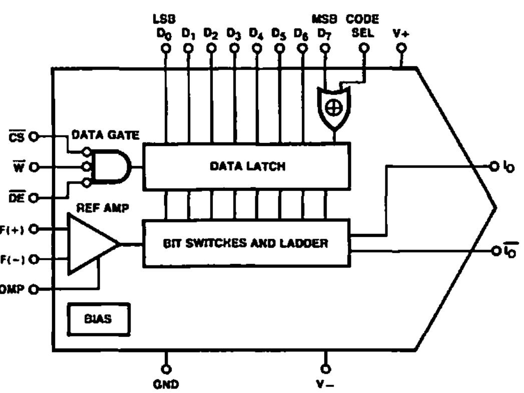
The converter allows a choice of 6 different coding formats. The most significant bit (D_7) can be inverted or non-inverted under the control of the code select input. The code control also provides a zero differential current output for 2's complement coding. A high voltage compliance, complementary current output pair is provided. The data latch is very high speed which makes the Am6080 capable of interfacing with high speed microprocessors.

Monotonic multiplying performance is maintained over a more than 40 to 1 reference current range. Matching within ±1 LSB between reference and full scale current eliminates the need for full scale trimming in most applications.

The Am6080 guarantees full 8-bit monotonicity. Nonlinearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the full power supply voltage and temperature range.

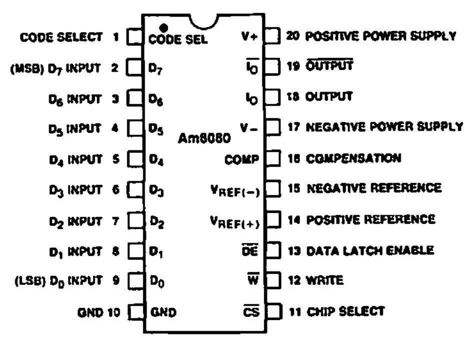
Applications for the Am6080 include microprocessor compatible data acquisition systems and data distribution systems, 8-bit A/D converters, servo-motor and pen drivers, waveform generators, programmable attenuators, analog meter drivers, programmable power supplies, CRT display drivers and high speed modems.

EQUIVALENT CIRCUIT



LIC-061

CONNECTION DIAGRAM
Top View



Pin 1 marked for orientation.

LIC-062

ORDERING INFORMATION

Package Type	Temperature Range	Nonlinearity	Order Number
Hermetic DIP	−55°C to +125°C	.1% .19%	Am6080ADM Am6080DM
Hermetic DIP	0°C to +70°C	.1% .19%	Am6080ADC Am6080DC
Molded DIP	0°C to +70°C	.1% .19%	Am6080APC Am6080PC

MAXIMUM RATINGS

Operating Temperature		Power Supply Voltage	±18V
Am6080ADM, Am6080DM	−55°C to +125°C	Logic Inputs	−5V to +18V
Am6080ADC, Am6080DC Am6080APC, Am6080PC	0°C to +70°C	Analog Current Outputs	−12V to +18V
		Reference Inputs ($V_{14}V_{15}$)	V− to V+
Storage Temperature	−65°C to +150°C	Reference Input Differential Voltage (V_{14} to V_{15})	±18V
Lead Temperature (Soldering, 60 sec)	300°C	Reference Input Current (I_{14})	1.25mA

ELECTRICAL CHARACTERISTICS

These specifications apply for $V_+ = +5V$, $V_- = -15V$, $I_{REF} = 0.5mA$, over the operating temperature range unless otherwise specified. Output characteristics refer to all outputs.

Parameter	Description	Conditions	Am6080A Min.	Am6080A Typ.	Am6080A Max.	Am6080 Min.	Am6080 Typ.	Am6080 Max.	Unit
	Resolution		8	8	8	8	8	8	bits
	Monotonicity		8	8	8	8	8	8	bits
D.N.L.	Differential Nonlinearity		–	–	±0.19	–	–	±0.39	%FS
N.L.	Nonlinearity		–	–	±0.1	–	–	±0.19	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{14} = R_{15} = 20.000k\Omega$ $T_A = 25°C$	1.984	1.992	2.000	1.976	1.992	2.008	mA
TCI_{FS}	Full Scale Tempco		–	±5	±20	–	±10	±40	ppm/°C
			–	.0005	±.002	–	.001	±.004	%FS/°C
V_{OC}	Output Voltage Compliance		−10	–	+18	−10	–	+18	Volts
I_{FSS}	Full Scale Symmetry	$I_{FS1} - \overline{I_{FS1}}$	–	±0.1	±1.0	–	±0.2	±2.0	μA
I_{ZS}	Zero Scale Current		–	0.01	0.4	–	0.01	0.8	μA
I_{RR}	Reference Current Range	V− = −5V	0	0.5	0.55	0	0.5	0.55	mA
		V− = −15V	0	0.5	1.1	0	0.5	1.1	mA
V_{IL}	Logic Input Levels — Logic "0"		–	–	0.8	–	–	0.8	Volts
V_{IH}	Logic Input Levels — Logic "1"		2.0	–	–	2.0	–	–	Volts
I_{IN}	Logic Input Current	V_{IN} = −5V to +18V	–	–	40	–	–	40	μA
V_{IS}	Logic Input Swing	V− = −15V	−5	–	+18	−5	–	+18	Volts
I_{15}	Reference Bias Current		–	−0.5	−2.0	–	−0.5	−2.0	μA
dI/dt	Reference Input Slew Rate	$R_{14(EQ)} = 800\Omega$ CC = 0pF	4.0	8.0	–	4.0	8.0	–	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	V+ = +4.5V to +5.5V, V− = −15V	–	±0.0003	±0.01	–	±0.0005	±0.01	%FS
$PSSI_{FS-}$		V− = −13.5V to − 16.5V, V+ = +5V	–	±0.0005	±0.01	–	±0.0005	±0.01	%FS
V+	Power Supply Range	$I_{REF} = 0.5mA$, $V_{OUT} = 0V$	4.5	–	18	4.5	–	18	Volts
V−			−18	–	−4.5	−18	–	−4.5	Volts
I+	Power Supply Current	V+ = +5V, V− = −5V	–	9.8	14.7	–	9.8	14.7	mA
I−			–	−7.4	−9.9	–	−7.4	−9.9	mA
I+		V+ = +5V, V− = −15V	–	9.8	14.7	–	9.8	14.7	mA
I−			–	−7.4	−9.9	–	−7.4	−9.9	mA
I+		V+ = +15V, V− = −15V		9.8	14.7	–	9.8	14.7	mA
I−			–	−7.4	−9.9	–	−7.4	−9.9	mA
P_O	Power Dissipation	V+ = +5V, V− = −5V	–	86	123	–	86	123	mW
		V+ = +5V, V− = −15V	–	160	222	–	160	222	mW
		V+ = +15V, V− = −15V	–	258	369	–	258	369	mW

Am6080 FUNCTIONAL PIN DESCRIPTION

Symbol	Function
D_0-D_7	D_0-D_7 are the input bits 1-8 to the input data latch. Data is transferred to the data latch when $\overline{CS}$, $\overline{DE}$, and $\overline{W}$ are active and is latched when any of the enable signals go inactive.
$\overline{CS}$	Chip Select – This active low input signal enables the Am6080. Writing into the data latch occurs only when the device is selected.
$\overline{W}$	Write – This active low control signal enables the data latch when the $\overline{CS}$ and $\overline{DE}$ inputs are active.
$\overline{DE}$	Data Latch Enable – This active low input is used to enable the data latch. The $\overline{CS}$, $\overline{DE}$, and $\overline{W}$ must be active in order to write into the data latch.
CODE SEL	Code Select – When CODE SEL = 0, the MSB (D_7) is inverted and 1 LSB balance current is added to the $\overline{I_O}$ output.
$V_{REF(+)}$ $V_{REF(-)}$	Positive and negative reference voltage to the reference bias amplifier. These differential inputs allow the use of positive, negative and bipolar references.
COMP	Compensation – Frequency compensating terminal for the reference amplifier.
I_O, $\overline{I_O}$	These are high impedance complementary current outputs. The sum of these currents is always equal to I_{FS}

FUNCTION TABLES

DATA LATCH CONTROL

$\overline{CS}$	$\overline{W}$	$\overline{DE}$	Data Latch
0	0	0	Transparent
X	X	1	Latched
X	1	X	Latched
1	X	X	Latched

X = Don't Care

CODE SELECT

CODE SEL	Function
0	MSB Inverted (Note 1)
1	MSB Non-inverted

Note 1. LSB balance current is added to the $\overline{I_O}$ output.

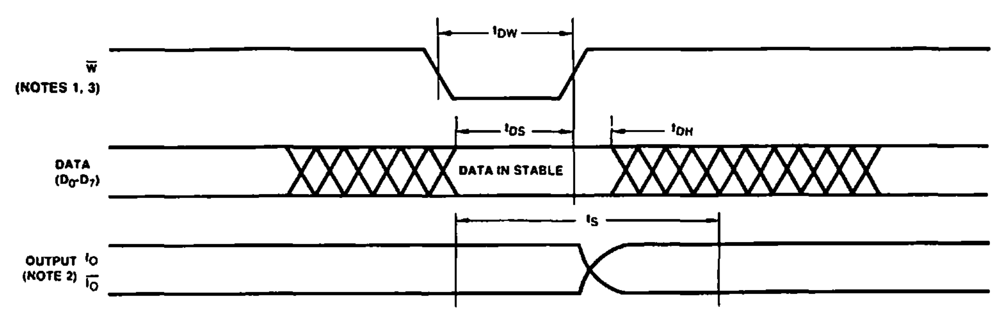
AC CHARACTERISTICS

$V_+ = +5V$, $V_- = -15V$, $I_{REF} = 0.5mA$, $R_L < 500\Omega$, $C_L < 15pF$ over the operating temperature range unless otherwise specified

Parameter	Description		Conditions	Commercial Temp. Grades Min.	Commercial Temp. Grades Typ.	Commercial Temp. Grades Max.	Military Temp. Grades Min.	Military Temp. Grades Typ.	Military Temp. Grades Max.	Unit
t_s	Settling Time, All Bits Switched		$T_A = 25°C$ Settling to ±½LSB		160			160		ns
t_{PLH}	Propagation Delay	Each bit	$T_A = 25°C$ 50% to 50%		80	160		80	160	ns
t_{PHL}		All bits switched			80	160		80	160	
t_{OH}	Data Hold Time		See timing diagram	10	−30		10	−30		ns
t_{OS}	Data Set Up Time		See timing diagram	80	35		100	35		ns
t_{DW}	Data Write Time		See timing diagram	80	35		100	35		ns

Notes: 1. t_{DW} is the overlap of $\overline{W}$ low, $\overline{CS}$ low, and $\overline{DE}$ low. All three signals must be low to enable the latch. Any signal going inactive latches the data.
2. t_S is measured with the latches open from the time the data becomes stable on the inputs to the time when the outputs are settled to within ±1/2 LSB. All bits switched on or off.
3. The internal time delays from $\overline{CS}$, $\overline{W}$ and $\overline{DE}$ inputs to the enabling of the latches are all equal.

TIMING DIAGRAM

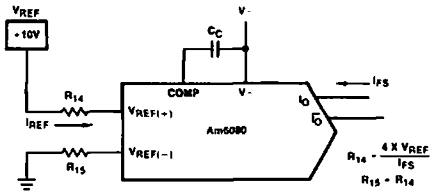


LIC-063

APPLICATION HINTS:

1. **Reference current and reference resistor.**
There is a 1 to 4 scale up between the reference current (I_{REF}) and the full scale output current (I_{FS}). If $V_{REF} = +10V$ and $I_{FS} = 2mA$, the value of the R_{14} is:

$$R_{14} = \frac{4 \times 10 \text{ Volt}}{2mA} = 20K\Omega$$



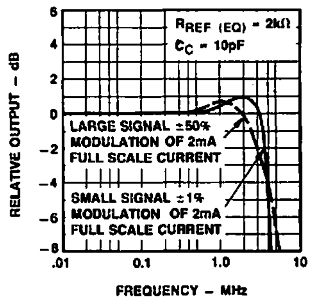
LIC-064

2. **Reference amplifier compensation.**
For AC reference applications, a minimum value compensation capacitor (C_C) is normally used. The value of this capacitor depends on R_{15}. The minimum values to maximize *bandwidth without* oscillation are as follows:

Table 2
Compensation Capacitor
(I_{FS} = 2mA, I_{REF} = 0.5mA)

R_{REF} (kΩ)	C_C (pF)
20	100
10	50
5	25
2	10
1	5
.5	0

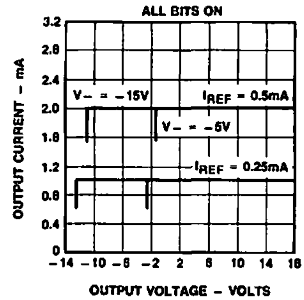
Reference Amplifier Frequency Response



A 0.01μF capacitor is recommended for the fixed reference operation.

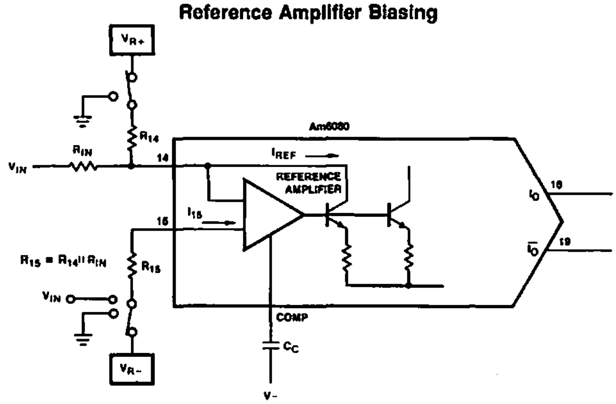
LIC-065

Output Voltage Compliance



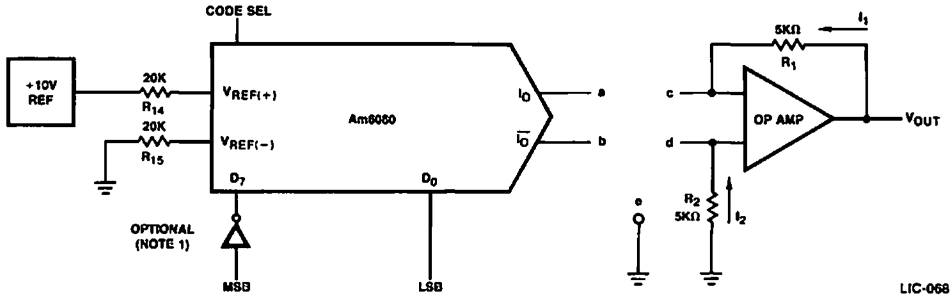
LIC-066

Reference Amplifier Biasing



Reference Configuration	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01μF	V_{R+}/R_{14}
Negative Reference	0V	V_{R-}	N/C	.01μF	$-V_{R-}/R_{14}$
Lo Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1)	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$ (Note 2)
Hi Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1)	$(V_{R+} - V_{IN})/R_{14}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$

Notes: 1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least C = 5pFX $R_{14(eq)}$ in kΩ. For R_{14} < 800Ω no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{14} must be greater than $-V_{IN}$ Max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 14 should be 800Ω or less and an additional resistor may be connected from pin 14 to ground to lower the impedance.



CODE FORMAT		CODE SEL	CONNECTIONS	OUTPUT SCALE	OUT SEL	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	I_1 (mA)	I_2 (mA)	V_{OUT}
UNIPOLAR	Straight binary: one polarity with true input code, true zero output.	1	a-c b-e	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	0	9.960
				Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	0	9.920
				Zero scale	X	0	0	0	0	0	0	0	0	.000	0	.000
	Complementary binary: one polarity with complementary input code, true zero output.	1	a-e b-c	Positive full scale	X	0	0	0	0	0	0	0	0	1.992	0	9.960
				Positive full scale − LSB	X	0	0	0	0	0	0	0	1	1.984	0	9.920
				Zero scale	X	1	1	1	1	1	1	1	1	.000	0	.000
SYMMETRICAL OFFSET	Straight offset binary: offset half scale, symmetrical about zero, no true zero output.	1	a-c b-d	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	.000	9.960
				Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	.008	9.880
				(+) Zero scale	X	1	0	0	0	0	0	0	0	1.000	.992	.040
				(−) Zero scale	X	0	1	1	1	1	1	1	1	.992	1.000	−.040
				Negative full scale − LSB	X	0	0	0	0	0	0	0	1	.008	1.984	−9.880
				Negative full scale	X	0	0	0	0	0	0	0	0	.000	1.992	−9.960
	1's complement: offset half scale, symmetrical about zero, no true zero output MSB complemented.. (need inverter at D_7)	1 (Note 1)	a-c b-d	Positive full scale	X	0	1	1	1	1	1	1	1	1.992	.000	9.960
				Positive full scale − LSB	X	0	1	1	1	1	1	1	0	1.984	.008	9.880
				(+) Zero scale	X	0	0	0	0	0	0	0	0	1.000	.992	.040
				(−) Zero scale	X	1	1	1	1	1	1	1	1	.992	1.000	−.040
				Negative full scale − LSB	X	1	0	0	0	0	0	0	1	.008	1.984	−9.880
				Negative full scale	X	1	0	0	0	0	0	0	0	.000	1.992	−9.960
OFFSET WITH TRUE ZERO	Offset binary: offset half scale, true zero output MSB complemented remainder add to I_O. (need inverter at D_7)	0 (Note 1)	a-c b-d	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	.008	9.920
				Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	.016	9.840
				+ LSB	X	1	0	0	0	0	0	0	1	1.008	.992	.080
				Zero scale	X	1	0	0	0	0	0	0	0	1.000	1.000	.000
				− LSB	X	0	1	1	1	1	1	1	1	1.992	1.008	−.080
				Negative full scale + LSB	X	0	0	0	0	0	0	0	1	.008	1.992	−9.920
				Negative full scale	X	0	0	0	0	0	0	0	0	.000	2.000	−10.000
	2's complement: offset half scale true zero output MSB complemented.	0	a-c b-d	Positive full scale	X	0	1	1	1	1	1	1	1	1.992	.008	9.920
				Positive full scale − LSB	X	0	1	1	1	1	1	1	0	1.984	.016	9.840
				+1 LSB	X	0	0	0	0	0	0	0	1	1.008	.992	.080
				Zero scale	X	0	0	0	0	0	0	0	0	1.000	1.000	.000
				−1 LSB	X	1	1	1	1	1	1	1	1	.992	1.008	−.080
				Negative full scale + LSB	X	1	0	0	0	0	0	0	1	.008	1.992	−9.920
				Negative full scale	X	1	0	0	0	0	0	0	0	.000	2.000	−10.000

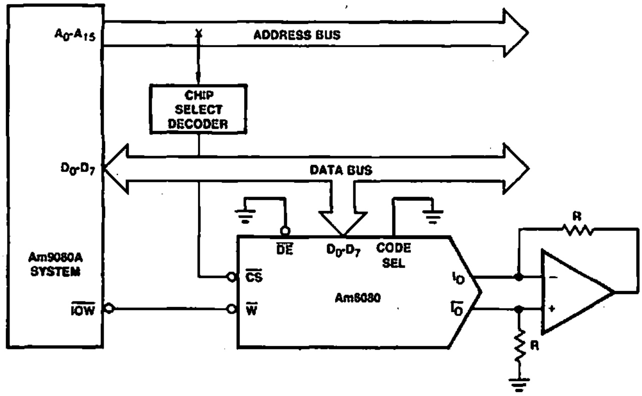
Note 1: An external inverter is necessary since the code select inverts the MSB and adds a 1 LSB balance current to $\overline{I_O}$. Only one of these features is desired for this code.

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

SYSTEM APPLICATIONS

Am9080A DATA SYSTEM

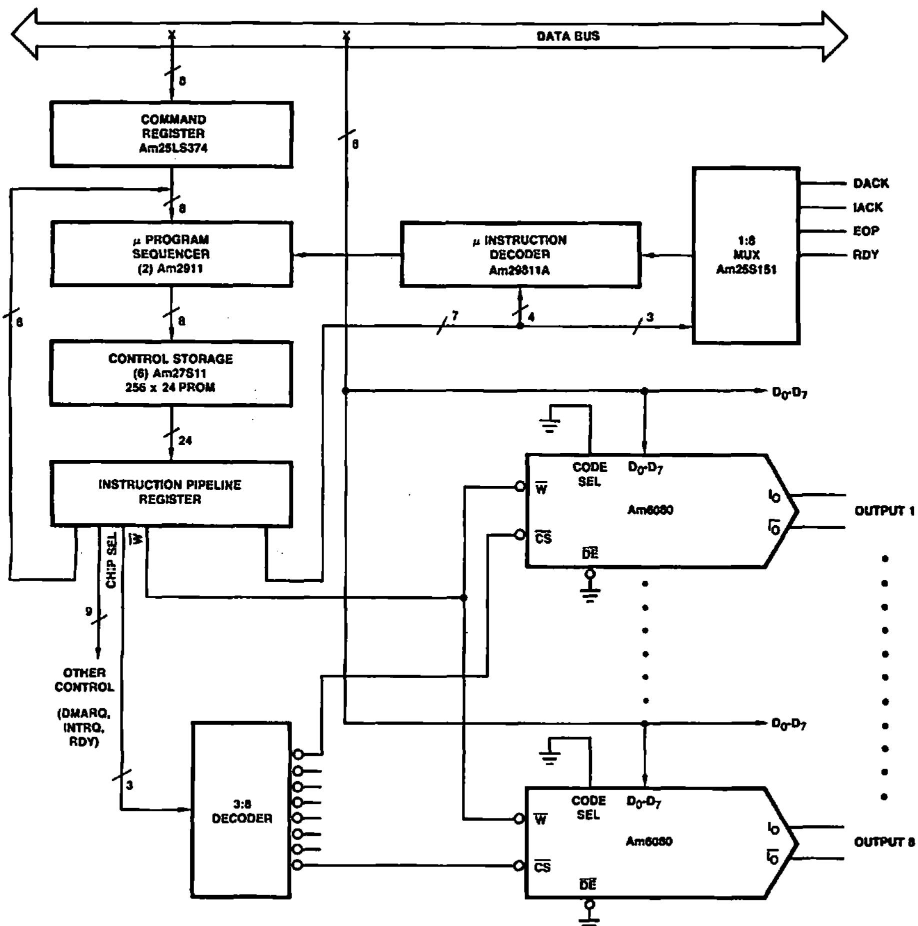


WRITING DATA INTO THE Am6080 (2's Complement)

PORT 1	:EQU OOH OUTPUT PORT ADDRESS
MOV A, M	:GET DATA FROM MEMORY
OUT 0 PORT1	:SEND DATA

LIC-069

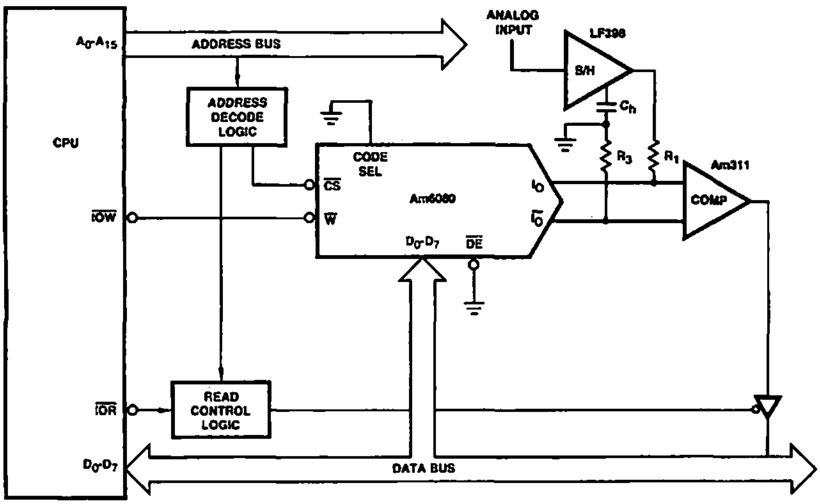
Am2900 DATA SYSTEM: MULTIPLE ANALOG INPUTS



LIC-070

SYSTEM APPLICATIONS (Cont.)

ANALOG/DIGITAL CONVERTER UNDER SOFTWARE CONTROL



LIC-071

Am9080A SOFTWARE FOR A/D CONVERSION USING Am6080.

SEQ		SOURCE STATEMENT	
0	PORT1	EQU 00H	;6080 A/O PORT ADDRESS
1	PORT3	EQU 02H	;COMPARATOR ADDRESS
2		ORG 3E50H	
3	START:	LXI SP,STAKS−16	;INITIAL STAKS POINTER
4	SAMPLE:	CALL ADCON	;CALL A/D CONVERSATION
5		JMP SAMPLE	;NEXT SAMPLE
6	ADCON:	XRA A	:CLEAR ACC
7		MOV D,A	;CLEAR D REG
8		STC	;SET CARRY
9		RAR	;SET BIT 7 TO 1
10		MOV B,A	;STORE TEST BIT AT B REGISTER
11	LOOP:	MOV E,A	;STORE TEST WORD
12		OUT PORT1	;OUTPUT TO A/D
13		IN PORT3	;INPUT FROM COMP
14		CRA A	;SET SIGN FLAG
15		JM NEXT	;IF SMALLER GO TO NEXT BIT
16		MOV D,E	;SAVE RESULT
17	NEXT:	MOV A,B	;GET NEXT TRIAL BIT
18		RAR	;SHIFT RIGHT ONCE
19		RC	;RETURN ON CARRY
20		MOV B,A	;STORE TEST BIT
21		ADD 0	;ACCUMULATE RESULT
22		JMP LOOP	;TRY NEXT BIT
23	STAKS:	DS 16	
24		END START	

APPLICATIONS

Instrumentation and Control

Data Acquisition
Data Distribution
Function Generation
Servo Controls
Programmable Power Supplies
Digital Zero Scale Calibration
Digital Full Scale Calibration
Digitally Controlled Offset Null

Audio

Music Distribution
Digitally Controlled Gain
Potentiometer Replacement
Digital Recording
Speech Digitizing

Signal Processing

CRT Displays
IF Gain Control
8 x 8 Digital Multiplication
Line Driver

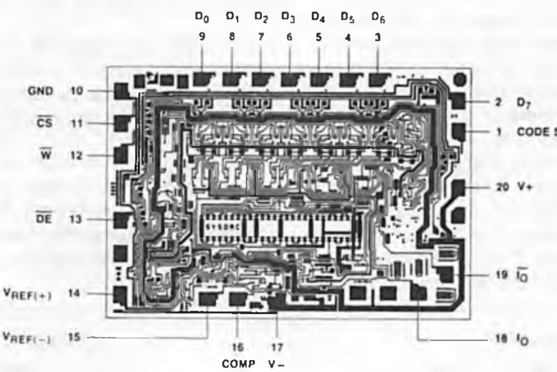
A/D Converters

Ratiometric ADC
Differential Input ADC
Microprocessor Controlled ADC

D/A Converters

Single Quadrant Multiplying DAC
Two Quadrant Multiplying DAC
Four Quadrant Multiplying DAC

Metallization and Pad Layout



DIE SIZE 0.085" X 0.124"

Am6081

Microprocessor System Compatible 8-Bit High Speed Multiplying D/A Converter

DISTINCTIVE CHARACTERISTICS

- 8-Bit D/A with 8-Bit input data latch
- Compatible with most popular microprocessors including the Am9080A-4 and the Am2900
- Write, Chip Select and Data Enable logic on chip
- DAC appears as memory location to microprocessor
- MSB inversion under logic control
- Differential current outputs
- Output current mode multiplexer with logic selection
- 2-Bit status latch for output select and code select
- Choice of 8 coding formats
- Fast settling current output – 200ns
- Nonlinearity to ±0.1% max over temperature range
- Full scale current pre-matched to ±1 LSB
- High output impedance and voltage compliance
- Low full scale current drift – ±5ppm/°C
- Wide range multiplying capability –2.0MHz bandwidth
- Direct interface to TTL, CMOS, NMOS
- Output range selection with on chip multiplexer
- High speed data latch – 80ns min write time

GENERAL DESCRIPTION

The Am6081 is a monolithic 8-bit multiplying Digital-to-Analog converter with an 8-bit data latch, a 2-bit status latch, chip select and other control signal lines which allow direct interface with microprocessor buses.

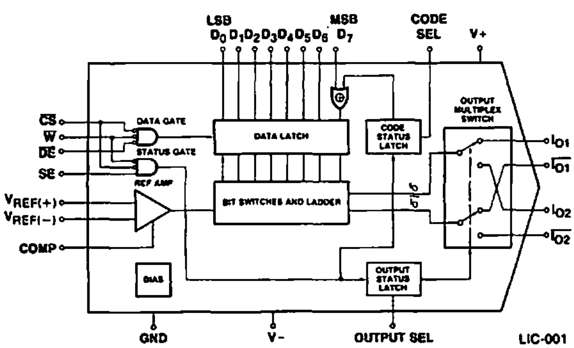
The converter allows a choice of 8 different coding formats. The most significant bit (D_7) can be inverted or non-inverted under the control of the code select input. The code control also provides a zero differential current output for 2's complement coding. A pair of high voltage compliance, dual complementary current output channels is provided and is selected by the output status command. The output multiplexer also allows analog bus connection of several converters, range or output load selection, and time-shared operation between D/A and A/D functions. The data and status latches are high speed which makes the Am6081 capable of interfacing with high speed microprocessors. The DE and SE control signals allow the data and status latches to be updated individually or simultaneously.

Monotonic multiplying performance is maintained over a more than 40 to 1 reference current range. Matching within ±1 LSB between reference and full scale current eliminates the need for full scale trimming in most applications.

The Am6081 guarantees full 8-bit monotonicity. Nonlinearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the full power supply voltage and temperature range.

Applications for the Am6081 include microprocessor compatible data acquisition systems and data distribution systems, 8-bit A/D converters, servo-motor and pen drivers, waveform generators, programmable attenuators, analog meter drivers, programmable power supplies, CRT display drivers and high speed modems.

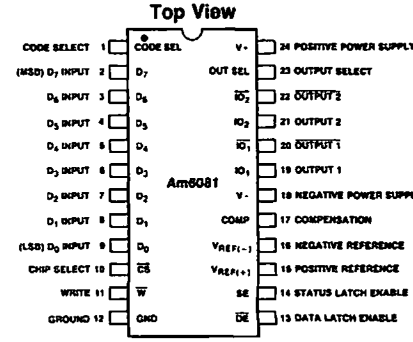
EQUIVALENT CIRCUIT



LIC-001

CONNECTION DIAGRAM

Top View



LIC-002

ORDERING INFORMATION

Package Type	Temperature Range	Nonlinearity	Order Number
Hermetic DIP	−55°C to +125°C	±.1%	Am6081ADM
		±.19%	Am6081DM
Hermetic DIP	0°C to +70°C	±.1%	Am6081ADC
		±.19%	Am6081DC
Molded DIP		±.1%	Am6081APC
		±.19%	Am6081PC

Am6081 FUNCTIONAL PIN DESCRIPTION

Symbol	Function
$\overline{CS}$	Chip Select – This active low input signal enables the Am6081. Writing into the data or status latches occurs only when the device is selected.
$\overline{DE}$	Data Latch Enable – This active low input is used to enable the data latch. The $\overline{CS}$, $\overline{DE}$, and $\overline{W}$ must be active in order to write into the data latch.
SE	Status Latch Enable – This active high input is used to enable the status latches. The $\overline{CS}$, SE, and $\overline{W}$ must be active in order to write into the status latches.
$\overline{W}$	Write – This active low control signal enables the data and status latches when the $\overline{CS}$, $\overline{DE}$, and SE inputs are active.
D_0-D_7	D_0-D_7 are the input bits 1-8 to the input data latch. Data is transferred to the data latch when $\overline{CS}$, $\overline{DE}$, and $\overline{W}$ are active and is latched when any of the enable signals go inactive.
CODE SEL	Code Select – Input to the CODE SEL latch. The latch is transparent when $\overline{CS}$, SE and $\overline{W}$ are active and is latched when any of the above signals go inactive. When CODE SEL latch = 0, the MSB (D_7) is inverted and 1 LSB balance current is added to the $\overline{I_O}$ output.
OUT SEL	Output Select – Input to the OUT SEL latch. The latch is transparent when $\overline{CS}$, SE and $\overline{W}$ are active and is latched when any of the above signals go inactive. When the OUT SEL latch is low, the channel 1 output pair (I_{O1}, $\overline{I_{O1}}$) is selected. When the OUT SEL latch is high, the channel 2 output pair (I_{O2}, $\overline{I_{O2}}$) is selected.
$V_{REF(+)}$ $V_{REF(-)}$	Positive and negative reference voltage to the reference bias amplifier. These differential inputs allow the use of positive, negative and bipolar references.
COMP	Compensation – Frequency compensating terminal for the reference amplifier.
I_{O1}, $\overline{I_{O1}}$ I_{O2}, $\overline{I_{O2}}$	These high impedance current output pairs are selected by the output select latch. I_{O1} and I_{O2} are true outputs and $\overline{I_{O1}}$ and $\overline{I_{O2}}$ are complementary outputs.

FUNCTION TABLES

DATA LATCH CONTROL

$\overline{CS}$	$\overline{W}$	$\overline{DE}$	Data Latch
0	0	0	Transparent
X	X	1	Latched
X	1	X	Latched
1	X	X	Latched

STATUS LATCH CONTROL

$\overline{CS}$	$\overline{W}$	SE	CODE SEL and OUT SEL Latch
0	0	1	Transparent
X	X	0	Latched
X	1	X	Latched
1	X	X	Latched

CODE SELECT AND OUTPUT SELECT

CODE SEL	OUT SEL	Function
0	–	MSB Inverted (Note 1)
1	–	MSB Non-inverted
–	0	Output Channel 1
–	1	Output Channel 2

X = Don't Care

Note 1. 1LSB balance current is added to the $\overline{I_O}$ output.

MAXIMUM RATINGS

Operating Temperature		Power Supply Voltage	±18V
Am6081ADM, Am6081DM	−55°C to +125°C	Logic Inputs	−5V to +18V
Am6081ADC, Am6081DC Am6081APC, Am6081PC	0°C to +70°C	Analog Current Outputs	−12V to +18V
		Reference Inputs (V_{15}, V_{16})	V− to V+
Storage Temperature	−65°C to +150°C	Reference Input Differential Voltage (V_{15} to V_{16})	±18V
Lead Temperature (Soldering, 60 sec)	300°C	Reference Input Current (I_{15})	1.25mA

GUARANTEED FUNCTIONAL SPECIFICATIONS

Resolution	8 bits
Monotonicity	8 bits

ELECTRICAL CHARACTERISTICS

These specifications apply for $V_+ = +5V$, $V_- = -15V$, $I_{REF} = 0.5mA$, over the operating temperature range unless otherwise specified. Output characteristics refer to all outputs.

Parameter	Description	Conditions	Am6081A Min.	Am6081A Typ.	Am6081A Max.	Am6081 Min.	Am6081 Typ.	Am6081 Max.	Unit
	Resolution	Straight coding/Sign Magnitude	8/9	8/9	8/9	8/9	8/9	8/9	bits
	Monotonicity	Straight coding/Sign Magnitude	8/9	8/9	8/9	8/9	8/9	8/9	bits
D.N.L.	Differential Nonlinearity		–	–	±0.19	–	–	±0.39	%FS
N.L.	Nonlinearity		–	–	±0.1	–	–	±0.19	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{15} = R_{16} = 20.000k\Omega$ $T_A = 25°C$	1.984	1.992	2.000	1.976	1.992	2.008	mA
TCI_{FS}	Full Scale Tempco		–	±5	±20	–	±10	±40	ppm/°C
			–	±.0005	±.002		±.001	±.004	%FS/°C
V_{OC}	Output Voltage Compliance		−10	–	+18	−10	–	+18	Volts
I_{FSS}	Full Scale Symmetry	$I_{FS1} - \overline{I_{FS1}}$ or $I_{FS2} - \overline{I_{FS2}}$	–	±0.1	±1.0	–	±0.2	±2.0	μA
I_{OSS}	Output Switch Symmetry	$I_{FS1} - I_{FS2}$ or $\overline{I_{FS1}} - \overline{I_{FS2}}$	–	±0.1	±1.0	–	±0.2	±2.0	μA
I_{ZS}	Zero Scale Current		–	0.01	0.4	–	0.01	0.8	μA
I_{DIS}	Output Disable Current	Output of mpx "Off" Channels	–	0.01	0.05	–	0.01	0.05	μA
I_{RR}	Reference Current Range	V− = −5V	0	0.5	0.55	0	0.5	0.55	mA
		V− = −15V	0	0.5	1.1	0	0.5	1.1	mA
V_{IL}	Logic Input Levels: Logic "0"		–	–	0.8	–	–	0.8	Volts
V_{IH}	Logic Input Levels: Logic "1"		2.0	–	–	2.0	–	–	Volts
I_{IN}	Logic Input Current	$V_{IN} = -5V$ to $+18V$	–	–	40	–	–	40	μA
V_{IS}	Logic Input Swing	V− = −15V	−5	–	+18	−5	–	+18	Volts
I_{16}	Reference Bias Current		–	−0.5	−2.0	–	−0.5	−2.0	μA
dI/dt	Reference Input Slew Rate	$R_{15(EQ)} = 800\Omega$ CC = 0pF	4.0	8.0	–	4.0	8.0	–	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	V+ = +4.5V to +5.5V, V− = −15V	–	±0.0005	±0.01	–	±0.0005	±0.01	%FS
$PSSI_{FS-}$		V− = −13.5V to −16.5V, V+ = +5V	–	±0.0005	±0.01	–	±0.0005	±0.01	%FS
V+	Power Supply Range	$I_{REF} = 0.5mA$, $V_{OUT} = 0V$	4.5	–	18	4.5	–	18	Volts
V−			−18	–	−4.5	−18	–	−4.5	Volts
I+	Power Supply Current	V+ = +5V, V− = −5V	–	9.8	14.7	–	9.8	14.7	mA
I−			–	−7.4	−9.9	–	−7.4	−9.9	mA
I+		V+ = +5V, V− = −15V	–	9.8	14.7	–	9.8	14.7	mA
I−			–	−7.4	−9.9	–	−7.4	−9.9	mA
I+		V+ = +15V, V− = −15V		9.8	14.7	–	9.8	14.7	mA
I−			–	−7.4	−9.9	–	−7.4	−9.9	mA
P_D	Power Dissipation	V+ = +5V, V− = −5V	–	86	123	–	86	123	mW
		V+ = +5V, V− = −15V	–	160	222	–	160	222	mW
		V+ = +15V, V− = −15V	–	258	369	–	258	369	mW

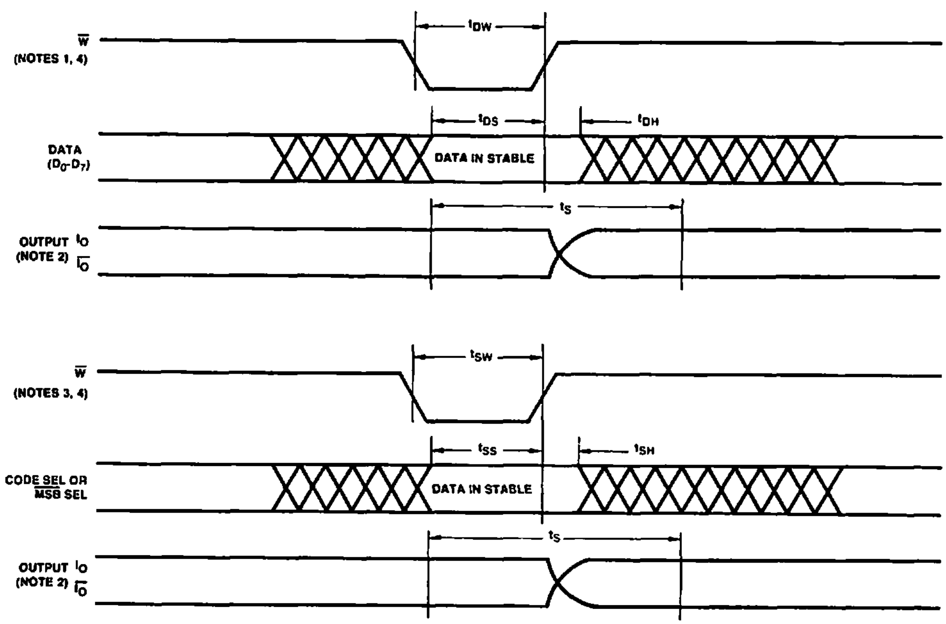
AC CHARACTERISTICS

$V_+ = +5V$, $V_- = -15V$, $I_{REF} = 0.5mA$, $R_L < 500\Omega$, $C_L < 15pF$ over the operating temperature range unless otherwise specified

Parameter	Description		Conditions	Commercial Temp. Grades Min.	Commercial Temp. Grades Typ.	Commercial Temp. Grades Max.	Military Temp. Grades Min.	Military Temp. Grades Typ.	Military Temp. Grades Max.	Unit
t_S	Settling Time, All Bits Switched		$T_A = 25°C$ Settling to ±½LSB		200			200		ns
t_{PLH}	Propagation Delay	Each bit	$T_A = 25°C$ 50% to 50%		90	180		90	180	ns
t_{PHL}		All bits switched			90	180		90	180	
t_{OS}	Output Switch Settling Time		$T_A = 25°C$ to ±1/2LSB of I_{FS}		250			250		ns
t_{OP}	Output Switch Propagation Delay		$T_A = 25°C$, 50% to 50%		150	300		150	300	ns
t_{DH}	Data Hold Time		See timing diagram	10	−30		10	−30		ns
t_{DS}	Data Set Up Time		See timing diagram	80	35		100	35		ns
t_{DW}	Data Write Time		See timing diagram	80	35		100	35		ns
t_{SH}	Status Hold Time		See timing diagram	10	−70		10	−70		ns
t_{SS}	Status Set Up Time		See timing diagram	200	100		250	100		ns
t_{SW}	Status Write Time		See timing diagram	200	100		250	100		ns

Notes:
1. t_{DW} is the overlap of $\overline{W}$ low, $\overline{CS}$ low, and $\overline{DE}$ low. All three signals must be low to enable the latch. Any signal going inactive latches the data.
2. t_S is measured with the latches open from the time the data becomes stable on the inputs to the time when the outputs are settled to within ±1/2 LSB. All bits switched on or off.
3. t_{SW} is the overlap of $\overline{W}$ low, $\overline{CS}$ low and SE high, all three signals must be active to enable the latch and any signal going inactive will latch the data.
4. The internal time delays from $\overline{CS}$, $\overline{W}$, SE and $\overline{DE}$ inputs to the enabling of the latches are all equal.

TIMING DIAGRAM



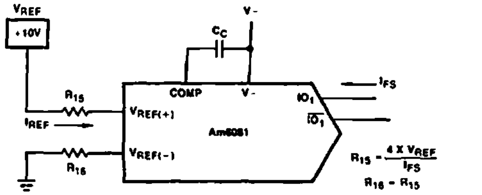
LIC-003

APPLICATION HINTS

1. Reference current and reference resistor

There is a 1 to 4 scale up between the reference current (I_{REF}) and the full scale output current (I_{FS}). If V_{REF} = +10V and I_{FS} = 2mA, the value of the R_{15} is:

$$R_{15} = \frac{4 \times 10 \text{ Volt}}{2\text{mA}} = 20\text{K}\Omega$$



LIC-004

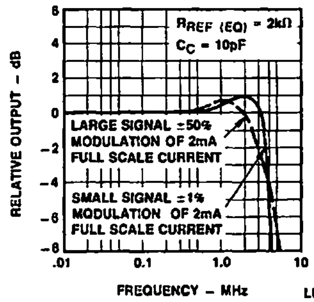
2. Reference amplifier compensation

For AC reference applications, a minimum value compensation capacitor (C_C) is normally used. The value of this capacitor depends on R_{15}. The minimum values to maximize bandwidth without oscillation are as follows:

Table 2
Compensation Capacitor
(I_{FS} = 2mA, I_{REF} = 0.5mA)

R_{REF} (kΩ)	C_C (pF)
20	100
10	50
5	25
2	10
1	5
.5	0

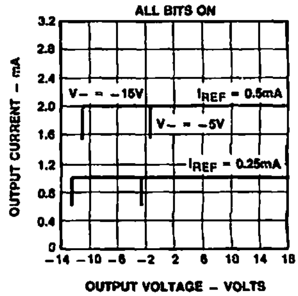
Reference Amplifier Frequency Response



LIC-005

Output Voltage Compliance

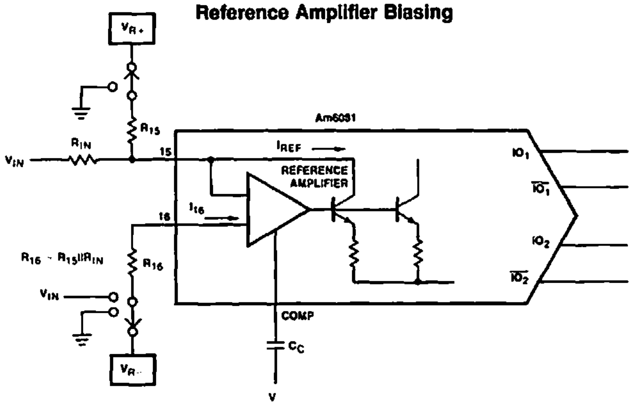
ALL BITS ON



LIC-006

A 0.01μF capacitor is recommended for the fixed reference operation.

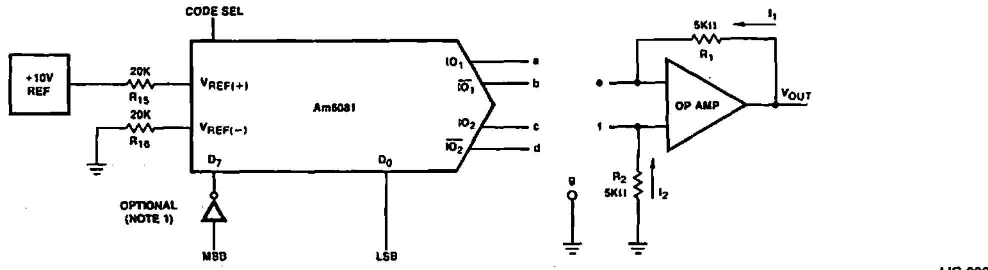
Reference Amplifier Biasing



LIC-007

Reference Configuration	R_{15}	R_{16}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01μF	V_{R+}/R_{15}
Negative Reference	0V	V_{R-}	N/C	.01μF	$-V_{R-}/R_{15}$
Lo Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1)	$(V_{R+}/R_{15}) + (V_{IN}/R_{IN})$ (Note 2)
Hi Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1)	$(V_{R+} - V_{IN})/R_{15}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{15}) + (V_{IN}/R_{IN})$

Notes:
1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least C = 5pF x $R_{15(EQ)}$ (in kΩ). For R_{15} < 800Ω no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{15} must be greater than $-V_{IN}$ Max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 15 should be 800Ω or less and an additional resistor may be connected from pin 15 to ground to lower the impedance.



Note: Connect all unused outputs to ground.

CODE FORMAT		CODE SEL	OUT SEL	CON-NECTIONS	OUTPUT SCALE	OUT SEL	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	I_1 (mA)	I_2 (mA)	V_{OUT}
UNIPOLAR	Straight binary: one polarity with true input code, true zero output.	1	0	a-e b-g	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	0	9.960
					Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	0	9.920
					Zero scale	X	0	0	0	0	0	0	0	0	.000	0	.000
			1	c-e d-g													
	Complementary binary: one polarity with complementary input code, true zero output.	1	0	a-g b-e	Positive full scale	X	0	0	0	0	0	0	0	0	1.992	0	9.960
					Positive full scale − LSB	X	0	0	0	0	0	0	0	1	1.984	0	9.920
					Zero scale	X	1	1	1	1	1	1	1	1	.000	0	.000
			1	c-g d-e													
SIGNED MAGNITUDE	Signed magnitude binary: 8 bits + sign reflected code, overlapping true zero output.	1		a-e c-f	Positive full scale	1	1	1	1	1	1	1	1	1	1.992	.000	9.960
					Positive full scale − LSB	1	1	1	1	1	1	1	1	0	1.984	.000	9.920
					(+) Zero scale	1	0	0	0	0	0	0	0	0	.000	.000	.000
					(−) Zero scale	0	0	0	0	0	0	0	0	0	.000	.000	.000
					Negative full scale − LSB	0	1	1	1	1	1	1	1	0	.000	1.984	−9.920
					Negative full scale	0	1	1	1	1	1	1	1	1	.000	1.992	−9.960
	Complementary signed magnitude: 8 bits + sign complementary reflected code, overlapping true zero output.	1		b-e d-f	Positive full scale	1	0	0	0	0	0	0	0	0	1.992	.000	9.960
					Positive full scale − LSB	1	0	0	0	0	0	0	0	1	1.984	.000	9.920
					(+) Zero scale	1	1	1	1	1	1	1	1	1	.000	.000	.000
					(−) Zero scale	0	1	1	1	1	1	1	1	1	.000	.000	.000
					Negative full scale − LSB	0	0	0	0	0	0	0	0	1	.000	1.984	−9.920
					Negative full scale	0	0	0	0	0	0	0	0	0	.000	1.992	−9.960
SYMMETRICAL OFFSET	Straight offset binary: offset half scale, symmetrical about zero, no true zero output.	1	0	a-e b-f	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	.000	9.960
					Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	.008	9.880
					(+) Zero scale	X	1	0	0	0	0	0	0	0	1.000	.992	.040
			1	c-e d-f	(−) Zero scale	X	0	1	1	1	1	1	1	1	.992	1.000	−.040
					Negative full scale − LSB	X	0	0	0	0	0	0	0	1	.008	1.984	−9.880
					Negative full scale	X	0	0	0	0	0	0	0	0	.000	1.992	−9.960
	1's complement: offset half scale, symmetrical about zero, no true zero output MSB complemented. (need inverter at D_7)	1 (Note 1)	0	a-e b-f	Positive full scale	X	0	1	1	1	1	1	1	1	1.992	.000	9.960
					Positive full scale − LSB	X	0	1	1	1	1	1	1	0	1.984	.008	9.980
					(+) Zero scale	X	0	0	0	0	0	0	0	0	1.000	.992	.040
			1	c-e d-f	(−) Zero scale	X	1	1	1	1	1	1	1	1	.992	1.000	−.040
					Negative full scale − LSB	X	1	0	0	0	0	0	0	1	.008	1.984	−9.880
					Negative full scale	X	1	0	0	0	0	0	0	0	.000	1.992	−9.960
OFFSET WITH TRUE ZERO	Offset binary: offset half scale, true zero output MSB complemented remainder add to I_O. (need inverter at D_7)	0 (Note 1)	0	a-e b-f	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	.008	9.920
					Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	.016	9.840
					+ LSB	X	1	0	0	0	0	0	0	1	1.008	.992	.080
					Zero scale	X	1	0	0	0	0	0	0	0	1.000	1.000	.000
			1	c-e d-f	− LSB	X	0	1	1	1	1	1	1	1	1.992	1.008	−.080
					Negative full scale + LSB	X	0	0	0	0	0	0	0	1	.008	1.992	−9.920
					Negative full scale	X	0	0	0	0	0	0	0	0	.000	2.000	−10.000
	2's complement: offset half scale true zero output MSB complemented.	0	0	a-e b-f	Positive full scale	X	0	1	1	1	1	1	1	1	1.992	.008	9.920
					Positive full scale − LSB	X	0	1	1	1	1	1	1	0	1.984	.016	9.840
					+1 LSB	X	0	0	0	0	0	0	0	1	1.008	.992	.080
					Zero scale	X	0	0	0	0	0	0	0	0	1.000	1.000	.000
			1	c-e d-f	−1 LSB	X	1	1	1	1	1	1	1	1	.992	1.008	−.080
					Negative full scale + LSB	X	1	0	0	0	0	0	0	1	.008	1.992	−9.920
					Negative full scale	X	1	0	0	0	0	0	0	0	.000	2.000	−10.000

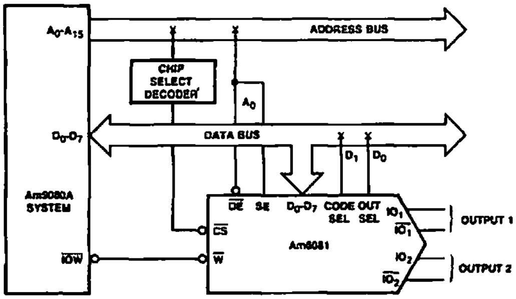
Note 1: An external inverter is necessary since the code select inverts the MSB and adds a 1 LSB balance current to $\overline{I_O}$. Only one of the two features is desired for these codes.

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.
2. The sign on any of the sign-magnitude codes may be changed by reversing the output terminal pair.
3. The polarity of the unipolar codes may be changed by driving the opposite side of the balanced load.

SYSTEM APPLICATIONS

Am9080A DATA SYSTEM: SEPARATE UPDATE OF DATA AND STATUS



SELECT OUTPUT PORT 1

MVI A, 2	:	SET STATUS TO 0 (SELECT OUTPUT 1)
OUT 1	:	SEND STATUS
MOV A, M	:	GET DATA FROM MEMORY
OUT 0	:	SEND DATA

SELECT OUTPUT PORT 2

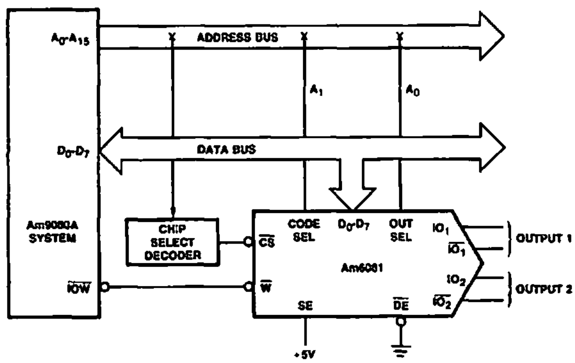
MVI A, 3	:	SET STATUS TO 1 (SELECT OUTPUT 2)
OUT 1	:	SEND STATUS
MOV A,M	:	GET DATA FROM MEMORY
OUT 0	:	SEND DATA

SELECT OUTPUT PORT 2 AND 2's COMPLEMENT CODE

MVI A, 1	:	SET STATUS TO 3 (OUTPUT 2, MSB COMP)
OUT 1	:	SEND STATUS
MOV A, M	:	GET DATA FROM MEMORY
OUT 0	:	SEND DATA

LIC-009

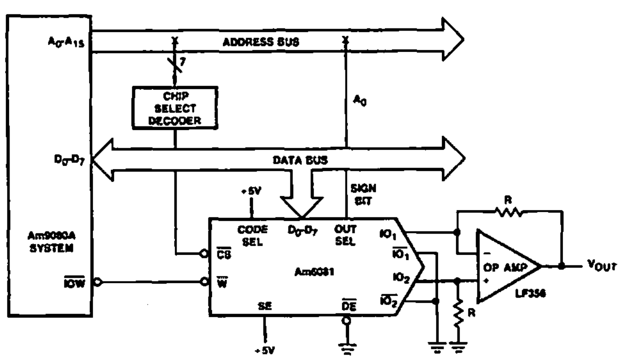
Am9080A DATA SYSTEM: SIMULTANEOUS UPDATE OF DATA AND STATUS



MOV A, M	:	GET DATA IN ACCUMULATOR
OUT 0	:	OUTPUT DATA TO PORT 1, 2'S COMPLEMENT
OUT 1	:	OUTPUT DATA TO PORT 2, 2'S COMPLEMENT
OUT 2	:	OUTPUT DATA TO PORT 1, STRAIGHT BINARY
OUT 3	:	OUTPUT DATA TO PORT 2, STRAIGHT BINARY

LIC-010

Am9080A DATA SYSTEM: 8-BIT PLUS SIGN CONVERSION

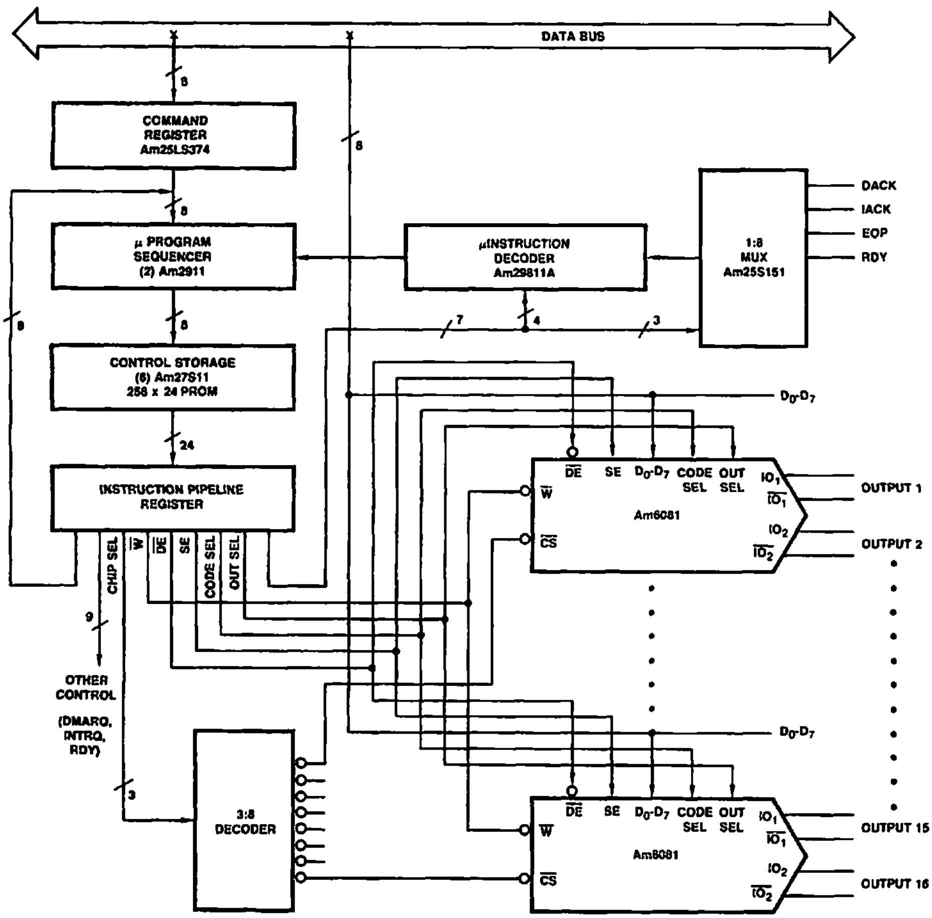


MOV A, M	:	LOAD MAGNITUDE (8-BITS)
OUT 0	:	SEND POSITIVE OUTPUT
OUT 1	:	SEND NEGATIVE OUTPUT

LIC-011

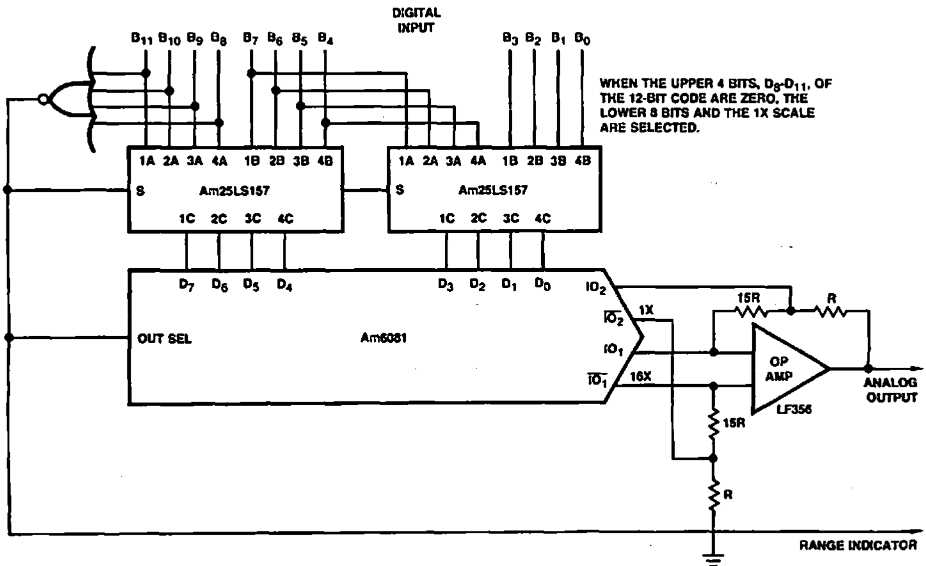
SYSTEM APPLICATIONS (Cont.)

Am2900 DATA SYSTEM: MULTIPLE ANALOG OUTPUTS



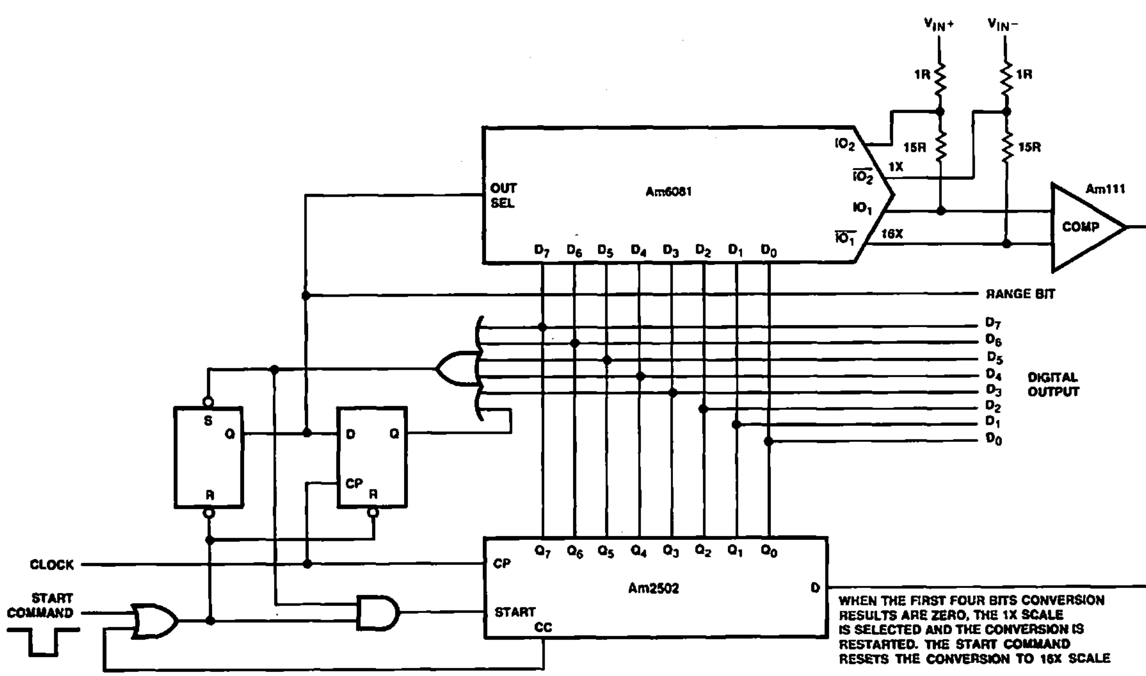
SYSTEM APPLICATIONS (Cont.)

D/A CONVERSION WITH 12-BIT DYNAMIC RANGE



LIC-013

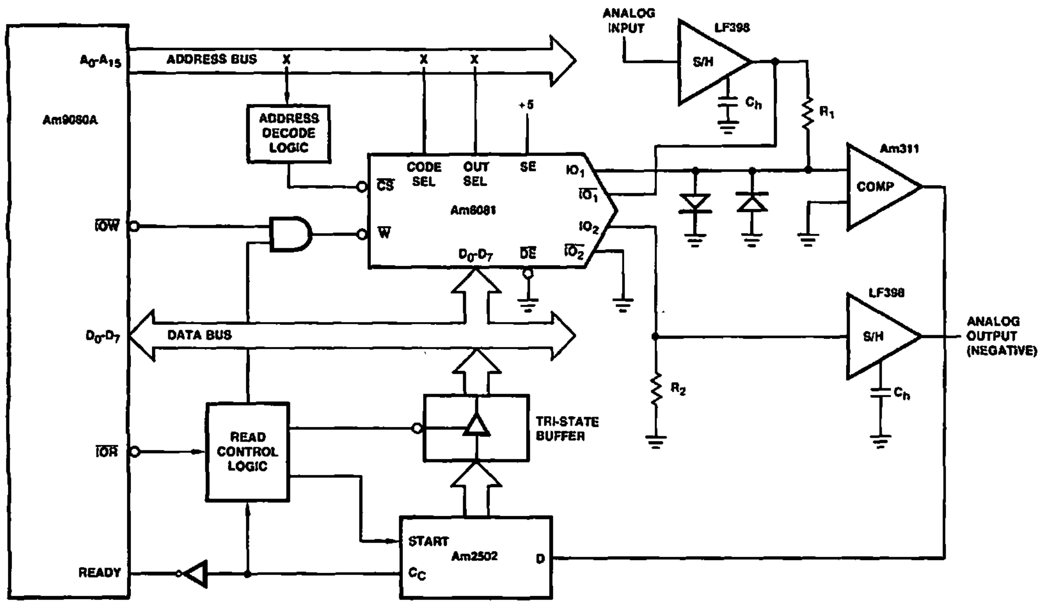
A/D CONVERSION WITH AUTO RANGING AND DIFFERENTIAL INPUT



LIC-014

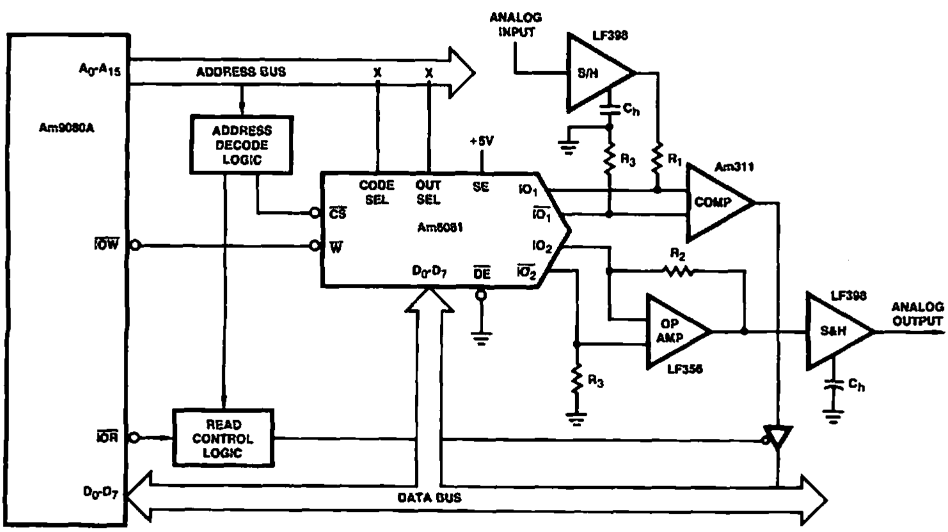
SYSTEM APPLICATIONS (Cont.)

ANALOG/DIGITAL TRANSCEIVER WITH HARDWARE CONTROLLED SUCCESSIVE APPROXIMATION A/D CONVERSION



LIC-015

ANALOG/DIGITAL TRANSCEIVER WITH SOFTWARE CONTROLLED A/D CONVERSION



LIC-016

Am9080A SOFTWARE FOR A/D AND D/A CONVERSION USING Am6081

SEQ		SOURCE STATEMENT	
0	PORT1	EQU 00H	
1	PORT3	EQU 02H	
2	PORT2	EQU 01H	
3		ORG 3E50H	
4	START:	LXI SP,STAKS-16	;INITIAL STAKS POINTER
5	SAMPLE:	CALL ADCON	;CALL A/D CONVERSATION
6		CMA	
7		CALL DACON	;CALL D/A CONVERSION
8		JMP SAMPLE	;NEXT SAMPLE
9	ADCON:	XRA A	:CLEAR ACC
10		MOV D,A	;CLEAR D REG
11		STC	;SET CARRY
12		RAR	;SET BIT 7 TO 1
13		MOV B,A	;STORE TEST BIT AT B REGISTER
14	LOOP:	MOV E,A	;STORE TEST WORD
15		CMA	
16		OUT PORT1	;OUTPUT TO A/D
17		IN PORT3	;INPUT FROM COMP
18		CMA	
19		CRA A	;SET SIGN FLAG
20		JM NEXT	;IF SMALLER GO TO NEXT BIT
21		MOV D,E	;SAVE RESULT
22	NEXT:	MOV A,B	;GET NEXT TRIAL BIT
23		RAR	;SHIFT RIGHT ONCE
24		RC	;RETURN ON CARRY
25		MOV B,A	;STORE TEST BIT
26		ADD D	;ACCUMULATE RESULT
27		JMP LOOP	;TRY NEXT BIT
28	DACON:	OUT PORT 2	;OUTPUT TO D/A
29		MVI C,05H	;LOAD C REG WITH TIME
30		DCR C	;TIME DELAY
31		RZ	;RETURN
32	FILT:	RET	
33	STAKS:	DS 16	
34		END START	

ADVANCED MICRO DEVICES DATA CONVERSION PRODUCTS

Digital to Analog Converters

- AmDAC-08 – 8-Bit High Speed Multiplying D/A Converter
- Am1508/1408 – 8-Bit Multiplying D/A Converter
- Am6070 – 8-Bit Companding D/A Converter for Control Systems (μ-law)
- Am6071 – 8-Bit Companding D/A Converter for Control Systems (A-law)
- Am6072 – 8-Bit Companding D/A Converter for Telecommunications (μ-law)
- Am6073 – 8-Bit Companding D/A Converter for Telecommunicatons (A-law)
- Am6080 – 8-Bit High Speed Multiplying D/A Converter System/Microprocessor Compatible
- Am6081 – 8-Bit High Speed Multiplying D/A Converter System/Microprocessor Compatible
- •Am6689 – 8-Bit, Ultra High Speed D/A Converter (ECL)
- •Am6012 – 12-Bit High Speed Multiplying D/A Converter

Analog to Digital Converters

- •Am6688 – 4-Bit Quantizer (Ultra High Speed A/D Converter)

Successive Approximation Registers

- Am2502 – 8-Bit Successive Approximation Registers
- Am2503 – 8-Bit Successive Approximation Registers
- Am2504 – 12-Bit Successive Approximation Registers

Sample and Hold Amplifiers

- LF198/398 –Monolithic Sample and Hold Amplifier
- •Am6098 –Precision Sample and Hold Amplifier

Comparators

- LM111/311 – Precision Voltage Comparator
- LM119/319 – Dual Comparator
- Am686 – High Speed Voltage Comparator

High Speed Operational Amplifiers

- Am118/318 – High Speed Operational Amplifier
- LF155/156/157 – JFET Input Operational Amplifiers
- LF355/356/357 – JFET Input Operational Amplifiers

• To be announced.

APPLICATIONS

Instrumentation and Control

Data Acquisition
Data Distribution
Data Transceiver
Function Generation
Servo Controls
Programmable Power Supplies
Digital Zero Scale Calibration
Digital Full Scale Calibration
Digitally Controlled Offset Null

Audio

Music Distribution
Digitally Controlled Gain
Potentiometer Replacement
Digital Recording
Speech Digitizing

Signal Processing

CRT Displays
Floating Point Analog Processors
IF Gain Control
Four Quadrant Multiplexer
8 x 8 Digital Multiplication
Line Driver

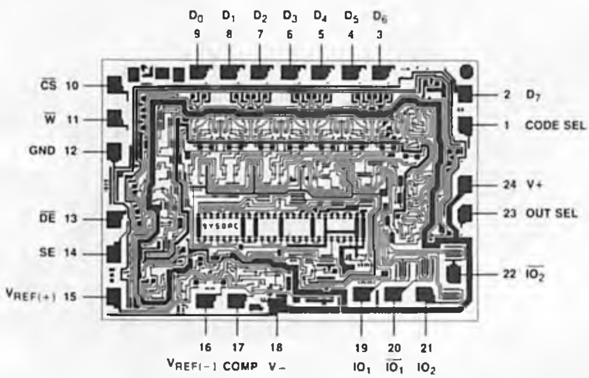
A/D Converters

Ratiometric ADC
Differential Input ADC
Multiple Input Range ADC
Two Channel ADC
Microprocessor Controlled ADC

D/A Converters

Single Quadrant Multiplying DAC
Two Quadrant Multiplying DAC
Four Quadrant Multiplying DAC
Two Channel DAC
Multiple Output Range DAC

Metallization and Pad Layout



DIE SIZE 0.085" X 0.124"

DATA CONVERSION WITH COMPANDING DAC DEVICES

By Dragan Milojkovic

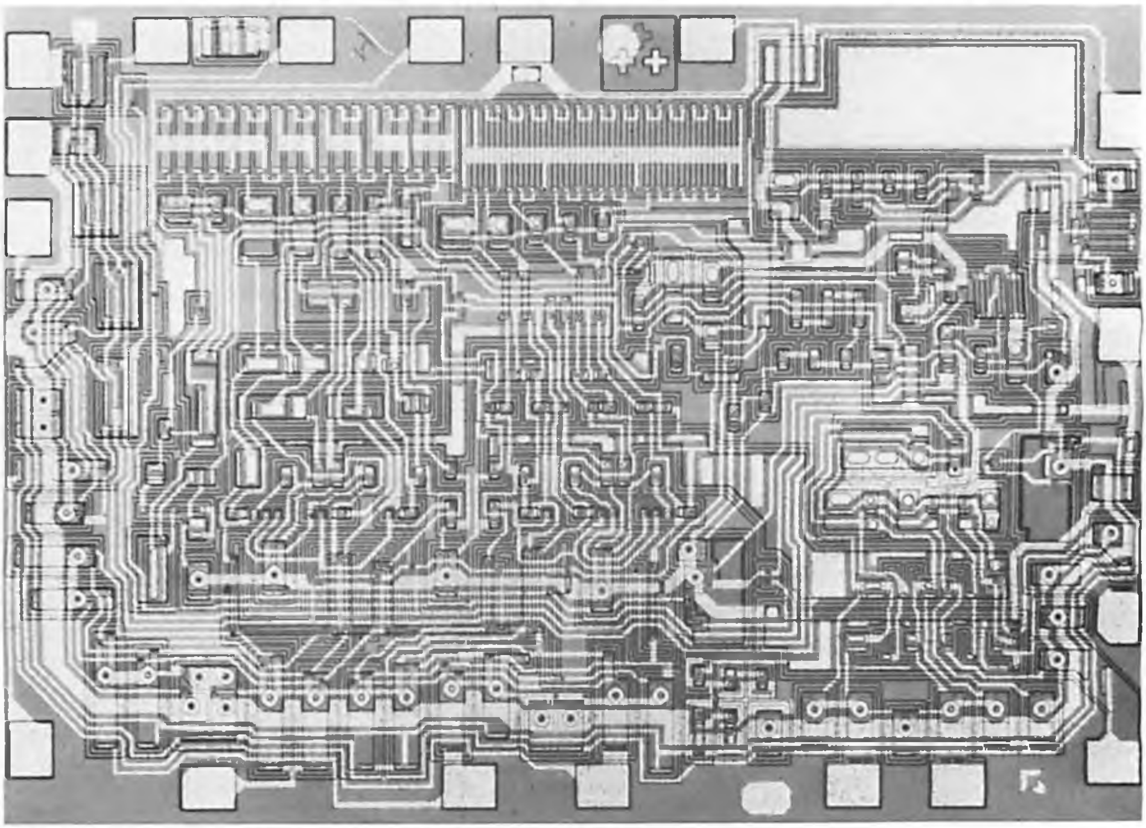


TABLE OF CONTENTS

INTRODUCTION

Modern electronic systems are replacing many of the analog signal processing and transmission functions with digital data processing. The use of digital electronics can lead to improvements in system cost, performance, accuracy and reliability. Digital systems can transmit many signals on the same line in a multiplexed mode and do not suffer from the same kinds of noise and crosstalk problems that are inherent in analog systems. The digital processing of analog information requires conversion of the analog signal into digital form and the reverse conversion of the digital result back into an analog signal. Analog to digital converters, (ADC), and digital to analog converters, (DAC), perform these functions. The DAC is the key circuit element in both of these processes since it is used in a feedback loop to generate the ADC function. Monolithic technology has advanced dramatically in the last few years making low cost 8-bit DACs a reality today; in the near future, 10 and 12-bit monolithic DACs will also become available. This trend in DAC technology will help accelerate the trend toward more digital processing and transmission of analog information.

Many analog signals vary in amplitude from very small values to very large values. The dynamic range of a converter is a measure of its ability to handle a wide range of input amplitudes and is defined as the ratio of the largest resolvable signal (V_{IN} max.) to the smallest signal (V_{IN} min.) that can be handled. This ratio is often expressed in decibels using the conversion formula 20 log (V_{IN}max/V_{IN}min). Linear DACs resolve a ratio of 2^n:1, (n equals the number of bits), or n • 6dB. An 8-bit linear DAC, for example, resolves a ratio of 256:1 or 48dB.

The accuracy of a converter is a prime concern in most applications. Accuracy is generally specified with respect to the full scale output (as a percent of full scale) or to the smallest step size (i.e., ±1/2LSB refers to ±1/2 of the smallest step size). Linear converters tend to be more accurate as the number of steps increases because the step size decreases. Many systems require high accuracy as a percent of the input signal level rather than as a percent of full scale. The accuracy as a percent of input signal level (reading) decreases as the signal level decreases because the amount of error is constant. An 8-bit linear DAC with an accuracy of .2% of full scale (±1/2 LSB) has an accuracy of .2% of reading for input signals near full scale, but an accuracy of only 20% of reading for an input near 1% of full scale.

For many types of applications, the accuracy and dynamic range of an 8-bit linear DAC are sufficient. However, there are many classes of problems that require a wider dynamic range to handle signal ratios of several thousand to one. Voice processing, speed control and music synthesis fall into this category. A 12-bit linear DAC provides a wider dynamic range, 72dB, and higher accuracy than an 8-bit linear DAC. However, these devices are very expensive, and, furthermore, it turns out that while most applications require the dynamic range of the 12-bit linear DAC they do not require its accuracy. A nonlinear DAC can provide such performance with fewer digital bits. It does so by using a nonlinear transfer characteristic to compress an analog signal into a digital word, and a complementary transfer characteristic to expand the digital values into analog signals with a wide dynamic range.

An 8-bit nonlinear DAC can achieve a 72dB dynamic range with accuracy expressed as a percent of reading that ranges from 1.6% to 3.2% over the entire dynamic range of the device. The overall nonlinear analog to digital and digital to analog conversion procedure is called the companding process. This note will discuss the Am6070 family of Companding DACs and their applications.

Companding Principles

Companding transfer functions were originally developed to satisfy the requirements of telephone voice communication systems. Studies of speech signals have shown that the distribution of amplitudes covers a range of several thousand to one and that the lower amplitude signals occur more often than the large amplitude signals. More attention should, therefore, be paid to the low level signals. It is important to maintain a better signal to distortion ratio (the ratio of signal level to conversion error) for low level signals at the expense of a poorer ratio for the less probable high level signals. In order to accomplish this goal, a logarithmic type of transfer characteristic is used with more steps at low levels and fewer steps at high levels.

A true logarithmic function has a discontinuity at zero and thus cannot be used directly for signal compression. A modified transfer characteristic with the form "log (1+x)" can be used to smooth the characteristic near zero. Two popular schemes have been developed – the μ-law by the Bell system for use in U.S. telephone systems and the A-law by the CCITT for use in European systems. They can be described by the following mathematical equations:

$$\mu\text{-Law: } Y = 0.18 \ln(1+\mu|X|)\ \mathrm{sgn}(X)$$

$$\text{A-Law: } Y = 0.18(1 + \ln(A|X|))\ \mathrm{sgn}(X), \quad 1/A \le |X| \le 1$$

$$Y = 0.18(A|X|)\ \mathrm{sgn}(X), \quad 0 \le |X| \le 1/A$$

where: X = analog signal level normalized to unity (encoder input or decoder output)
Y = digital signal level normalized to unity (encoder output or decoder input)
μ = 255 and A = 87.6

Both functions require that the size of the analog output change increase for each increasing digital code. In order to implement such a function, an overly complex analog circuit would be needed. This requirement is met, instead, by a piecewise linear approximation. In this approximation, an 8-bit digital word generates 256 analog outputs with a transfer characteristic which is symmetrical about the origin. Figure 1 shows the μ-law and A-law transfer characteristics and the linear 8-bit DAC transfer characteristic. The positive 128 steps are divided into 8 segments or chords of 16 steps each, from step 0 to step 15. The step size is constant within a chord and doubles for each increasing chord. If the step size in the first chord, chord 0, is assigned a value of 1, the next chord, chord 1, has a step size of 2, chord 2 has a step size of 4, etc. The last chord has a step size of 128 units and ends roughly at the value 4000. The 128 steps represent a 7-bit digital word with a dynamic range of 72dB, 20 log (4000:1), which is equivalent to the dynamic range of a 12-bit linear DAC.

The above description describes the μ-law curve. The A-law differs from the μ-law only in the first two chords. The step size in the A-law DAC does not change between the first and second chords, but doubles in all succeeding chords. The A-law DAC has a 1/2 step offset at zero so that the positive and negative zero codes do not generate the same point. The A-law DAC has a dynamic range of 62dB which is equivalent to an 11-bit linear DAC.

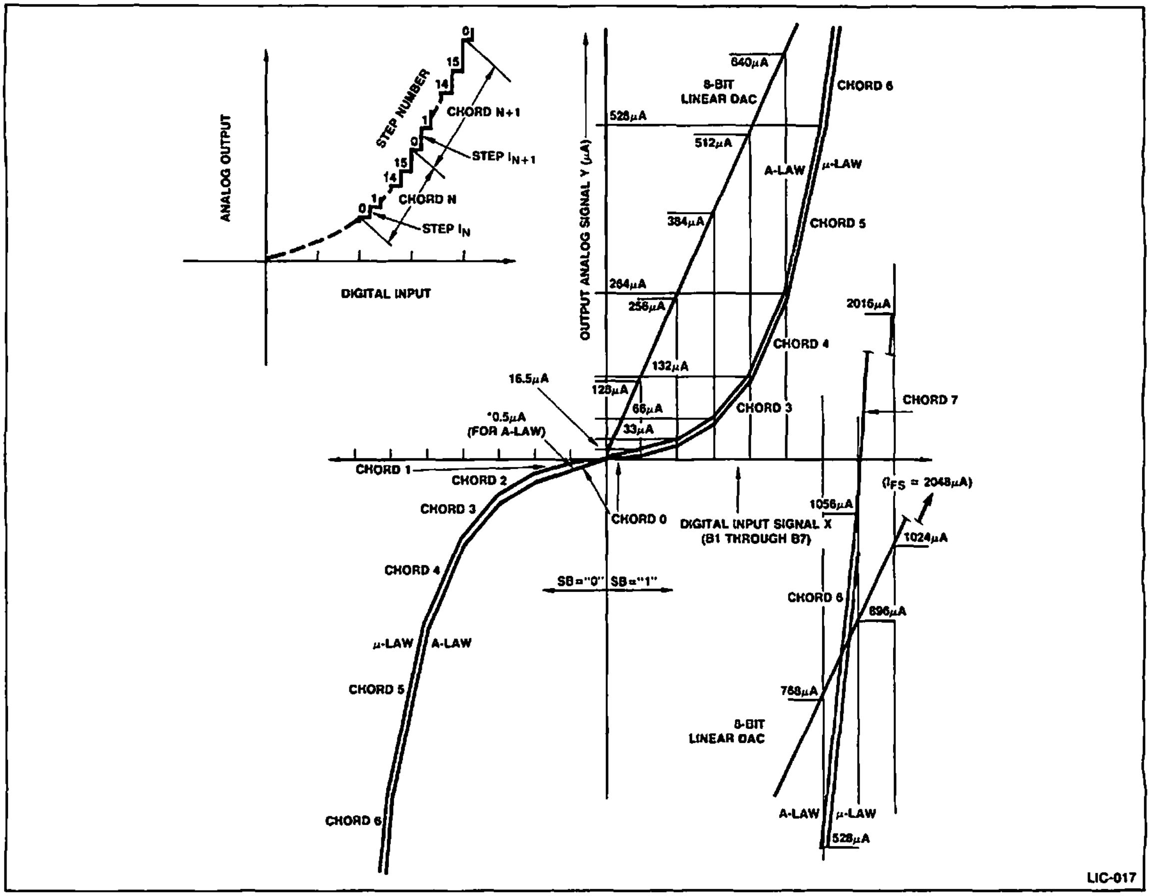


Fig. 1. Transfer Functions for μ-Law and A-Law Decoders.

Analog to Digital Conversion Using DACs

A digital input word to a DAC corresponds to an exact and unique analog output level. The total number of discrete output levels, m, depends on the number of DAC binary inputs, ($m=2^n$, n = number of input bits), and each output level is specified to be within a certain error band of its ideal value. An analog input to an ADC, on the other hand, may have an infinite number of signal levels which must be represented with only a finite number of digital output combinations. The output code, ideally, identifies the digital word that most closely represents the analog input. The classical way to generate a fast ADC function is to use a DAC in a feedback loop together with special ADC logic, employing a comparator and a successive approximation register (SAR). The feedback loop compares the DAC output with the analog input and decides whether the digital code is greater than or less than the input to the DAC. The input to the DAC is then increased or decreased accordingly, and another comparison is made. This technique causes each bit to be changed one at a time, and, by comparing the DAC's output with the analog input, the value of that bit is determined. Modification of one bit at a time, starting with the most significant bit and ending with the least significant bit, leads to an output which with each successive bit becomes a closer approximation of the input level. A total of n comparisons are needed for an n-bit converter.

The overall transfer characteristic of the entire ADC system is shown in Figure 2a. The ADC logic approximates the input analog signal by rounding off to the closest lower digital value. The maximum uncertainty in the digital representation of the analog input will be a full bit. In order to reduce this uncertainty, the ADC transfer curve can be modified to round to the nearest digital code, instead of the lowest, by adding a half step offset to the characteristic as shown in Figure 2b. The ADC now changes its outputs for analog inputs halfway between digital code points and gives a reading with ±1/2 step uncertainty. The half step offset necessary for better ADC accuracy is easily provided by increasing the DAC's analog output level by a half step whenever the DAC is used in an ADC scheme. This additional half step is easy to generate with linear DACs because of their constant step size throughout the entire dynamic range. For a Companding DAC this addition is much more difficult since the step size varies with signal value. In order to alleviate this problem, the Companding DAC has a built in capability to produce an appropriate half step offset signal at its output by a logic command. When this command input ($\overline{E}/D$ pin) is at logic 0, the Companding DAC is in the decode mode and the output will not contain the half step offset current. When the command input is at logic 1, the DAC is in the encode mode, i.e., within an ADC scheme, and the output current is increased by the correct half step for any input mode.

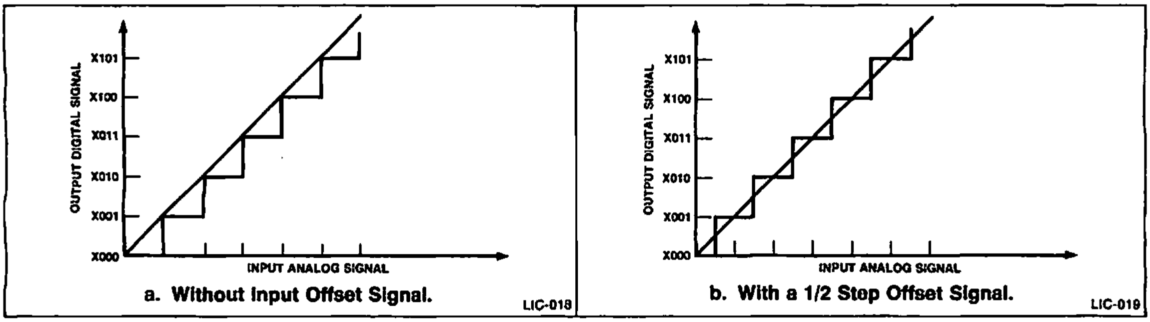


Fig. 2. Transfer Characteristic of an A to D Conversion System.

Companding DACs in Industrial Systems

Companding DACs differ from linear DACs in output dynamic range, transfer function, and the size of intermediate output steps. Comparable 8-bit linear DACs, such as the popular AmDAC-08, have a linear transfer characteristic with 256 linear steps, where each step is 8μA in size. The AmDAC-08 has a dynamic range of only 48dB while the 8-bit Companding DAC, (Am6070), has an output dynamic range of 72dB, which is also achievable with a 12-bit linear DAC. The output current increments of the Companding DAC, corresponding to small output signals, are significantly smaller than 8μA, which is the step size for the AmDAC-08. The step sizes in the first four chords of the Companding DAC transfer function are 0.5μA, 1.0μA, 2.0μA, and 4.0μA, respectively, with a total of 64 steps and a current value at the end of the fourth chord of approximately 100μA. By comparison, the AmDAC-08 uses only 12 uniform steps to resolve a 100μA output current level.

Given the assumption that most industrial systems employ an 8-bit digital data bus, the 8-bit DAC is a logical choice for interfacing with these systems. Companding DACs can be used in the same general applications as the AmDAC-08, particularly for reconstruction of analog signals with dynamic ranges that exceed 48dB. One example is the measurement of gas or liquid pressure, in an industrial environment, by pressure transducers with a pressure range of 0 to 3000PSI. Another example is digital recording of sound signals which usually exhibit a very large dynamic range.

The Companding DAC's logarithmic-like nonlinear transfer function suggests the application of this device for simulation of nonlinear waveforms which can be generated by converting a sequence of bytes, from an 8-bit processor, into an analog signal with an exponential shape. This type of signal can be used in nonlinear control systems such as motor velocity controllers. Additionally, the high resolution and accuracy of the Companding DAC transfer function, for small output signal levels, provide a very smooth and precise analog control signal to devices whose outputs are voltage or current dependent.

In general, the Companding DAC should be used in any system where a large dynamic range is needed. Such systems include servo motor controls, electromechanical positioning, voice and music synthesis and recording, secure communications, log sweep generators, digital control of gain and attenuation, and microprocessor controlled signal generation.

Companding DACs in PCM Transmission Systems

The companding laws were developed to satisfy the requirements of the telephone system for the digital transmission of voice signals. Voice signals exhibit a dynamic range of several thousand to one. To transmit this information with 8-bit words and retain reasonable accuracy at low levels, a companding transfer characteristic must be used to compress the analog signal prior to transmission and to restore the original signal after reception. The transmission of an analog signal in a digital format involves sampling, quantizing (A to D conversion), and compressing the analog signal as shown in Figure 3. The receiver must perform the complementary functions of expansion, digital to analog conversion and filtering to restore the analog signal waveform. The entire procedure is known as pulse code modulation, (PCM), and is the prevalent technique for digital transmission in communication systems. Currently, the Bell μ-law is the standard in the United States and the CCITT A-law is the standard in Europe.

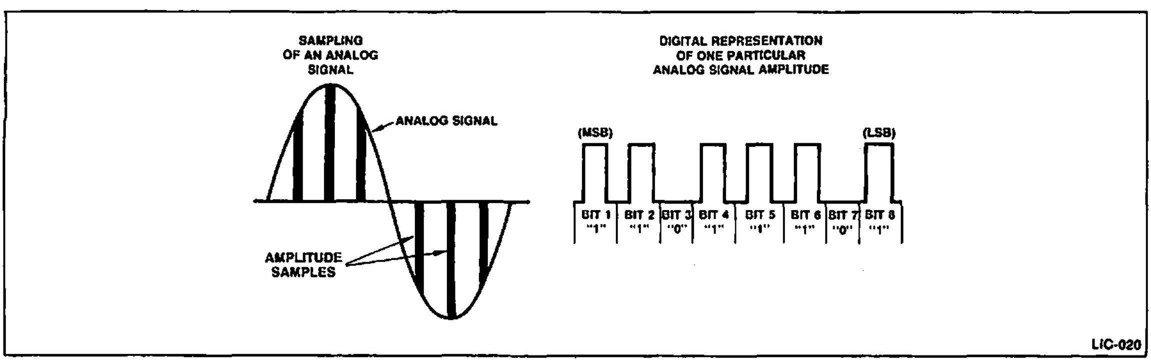


Fig. 3. Pulse Code Modulation Example.

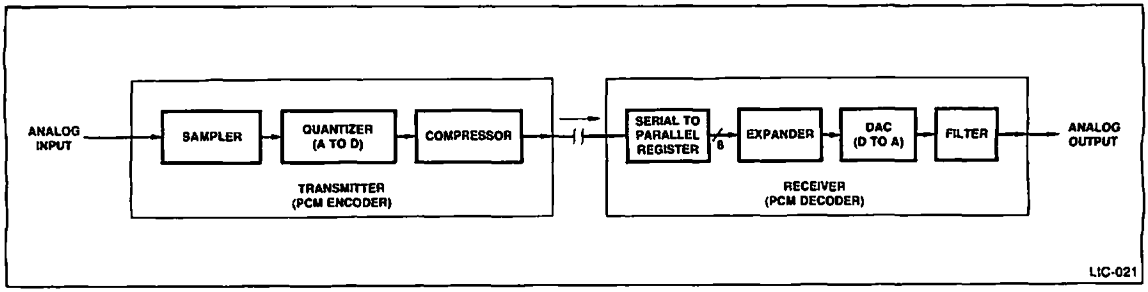


Fig. 4 One-Way PCM Transmission System Block Diagram.

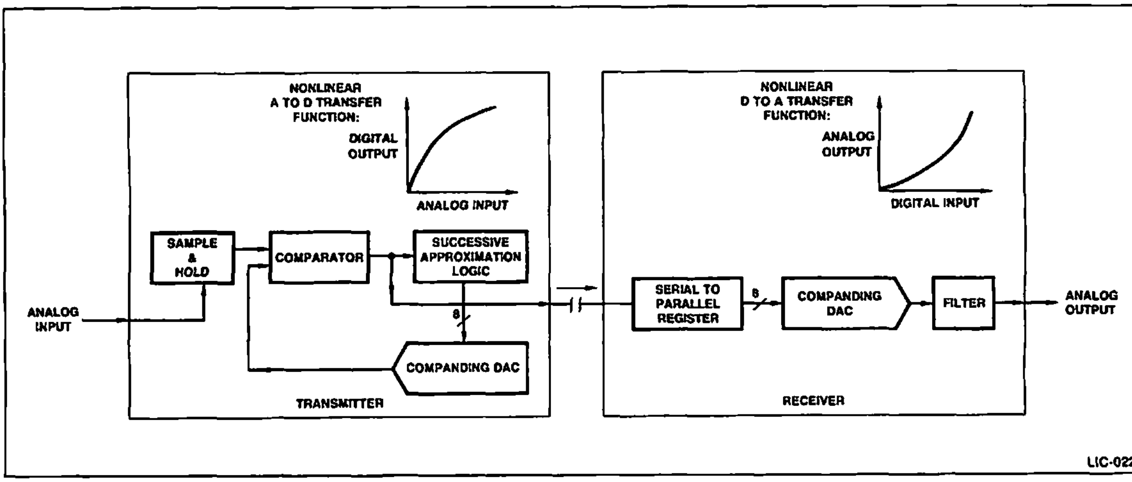


Fig. 5. One-Way PCM Transmission System Implemented with Companding DAC.

A simplified block diagram of a PCM transmission system is shown in Figure 4. The analog signal must be sampled at a rate that is at least twice as fast as the maximum bandwidth of the system, (3.4KHz), in order to achieve satisfactory signal reproduction at the receiver site. (This requirement is based on the Nyquist sampling theorem.) The telephone system uses a sampling rate of 8kHz which allows 125μs between samples. During this time the entire signal sampling, quantizing, encoding, and multiplexing must be completed.

The companding DAC is a complete PCM decoder (receiver) that performs both the decoding and D/A conversion. The DAC has additional encoding capabilities which make it very attractive for use in CODECs (a CODEC is both an Encoder and Decoder). The transfer characteristics of this device closely follow the characteristics defined by the μ-law, (Am6072), or A-law, (Am6073). A typical connection of a Companding DAC in a PCM transmission system is shown in Figure 5. In the transmitter side, the Companding DAC operates in a feedback loop using a SAR to perform the data encoding function. The corresponding logarithmic transfer curve for the entire feedback loop portion of the transmitter is also shown in Figure 5. The value of the sampled signal is estimated by a series of 9 iterations until its appropriate quantized digital representation appears at the 8-bit parallel data output of the SAR. This 8-bit digital code will be transmitted to the digital inputs of another Companding DAC for the decoding operation. The input/output transfer function for the Companding DAC is also shown in Figure 5.

The Companding DAC can be used in PCM decoders, encoders or complete CODECs. It is a high speed device that is capable of handling more than one channel in a multiplexed system. In multi-channel systems Companding DACs can be configured in a variety of ways depending on the number of channels, the method of transmission, (serial or parallel data), and synchronization of the system. A single Companding DAC can be used, for example, to decode all 24 channels in a standard Bell D3 data bank.

COMPANDING DAC CIRCUIT DESCRIPTION

General Circuit Description

The basic function of the 8-bit, Companding DAC is to convert a digital input value into an analog output current. The output current is a function of the digital data inputs and the input reference current. The full scale current, I_{FS}, is generated by the 7-bit data input binary code 111 1111, and is a linear function of the reference current, I_{REF}. There are two operating modes, Encode and Decode, which are controlled by the Encode/Decode, ($E/\overline{D}$), digital control signal. The output dynamic ranges achieved with the sign-plus-7-bit Companding DACs are 62dB (A-law) and 72dB (μ-law) which correspond to the output dynamic ranges of sign-plus-11-bit and sign-plus-12-bit linear binary DACs. Digital data and control inputs provide for easy digital control of converter operations in computer based data conversion systems.

The internal device design assures the accuracy and monotonicity of the Companding DAC over the entire dynamic and temperature ranges by maintaining the chord end points and step size deviations within allowable limits. Parametric deviations and requirements can be expressed in terms of corresponding step fractions which are applied throughout the entire output dynamic range. In industrial environments it is customary to specify allowable deviations from ideal parametric values within ± half a step. However, the μ-law and A-law based PCM communication systems specify the output current deviations in terms of dB, with respect to I_{FS}. Furthermore, these communication requirements in dB cannot be translated to some reasonable "step fraction" deviation which will be common for the entire output dynamic range. Consequently, Companding DACs applied in communication systems must be tested against specific output current values which are calculated separately for each step of the transfer characteristic. This difference between communication and industrial Companding DAC devices is recognized by Advanced Micro Devices which offers μ-law and A-law devices for both the industrial market, Am6070 and Am6071, and the telecommunication market, Am6072 and Am6073.

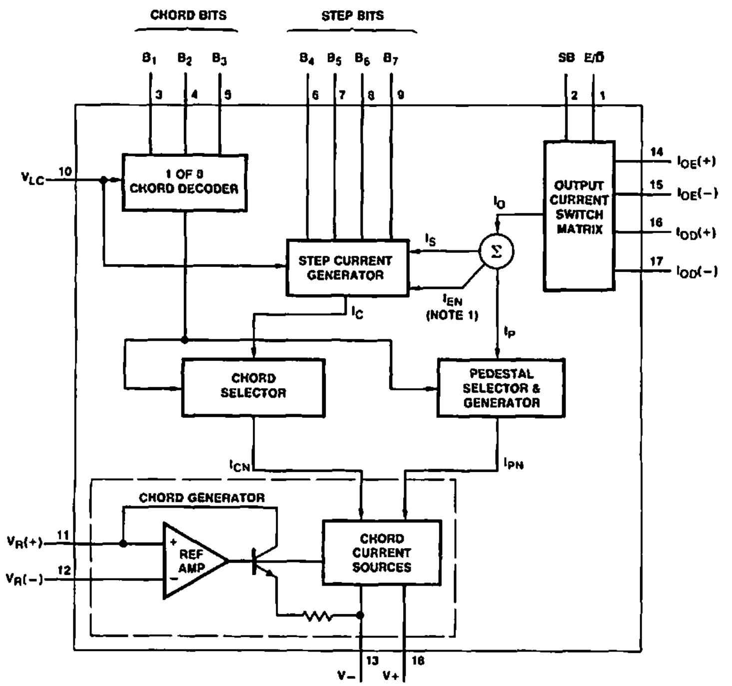
These Companding DACs are manufactured in an 18-pin package. There are seven digital data inputs, (B1 through B7), two control digital input signals, (SB, E/$\overline{D}$), and four analog current outputs, ($I_{OD(+)}$, $I_{OD(-)}$, $I_{OE(+)}$, $I_{OE(-)}$). The maximum output current value or full scale current, I_{FS}, is determined by the value of the reference current, I_{REF}, supplied to the Companding DAC via two analog reference inputs, ($V_{R(+)}$ and $V_{R(-)}$). There are three power supply connections (V−, V+ and Ground).

Detailed Circuit Description

The block diagram of the Companding DAC is shown in Figure 6. The circuit consists of the following five major blocks:

- The chord generator produces the total current for each chord or segment of the curve.
- The pedestal generator generates the pedestal or starting point for each chord.
- The step generator generates the proper step current for each chord.
- The chord decoding logic decodes the chord inputs and controls the inputs to the pedestal and step generator circuits.
- The output switching matrix sums the step and pedestal currents and routes them to the proper output node.

To understand the circuitry of the Companding DAC it is important to understand how the companding curve is generated. The companding curve is a piecewise linear approximation of an exponential characteristic. It consists of 16 linear segments centered around the origin. The curve is symmetrical around the origin so we need only examine the positive portion of the curve. Each segment or chord consists of sixteen steps, step 0 through step 15, and the size of each step doubles as the chord number increases. In order to smooth out the characteristic as the chords change, the step current value for the first step of each higher chord, step 0, is set to be 1 1/2 times larger than the step current values in the lower chord. The succeeding fifteen steps, step 1 to step 15, are 2 times larger than steps of the previous chord. Figure 7 shows a detailed synthesis of the companding function. The first



Note 1: I_{EN} contributes to I_O only in the encode mode specified by E/$\overline{D}$ = "1".

LIC-023

Fig. 6. Companding DAC Functional Block Diagram.

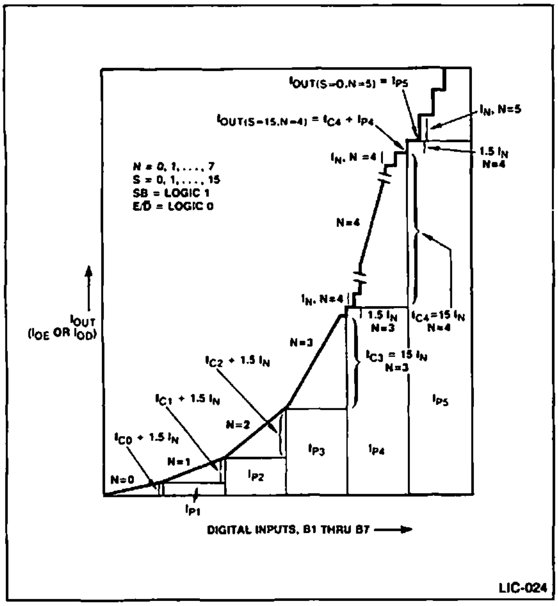


Fig. 7. Construction of μ-Law Transfer Function.

chord, C0, is generated from a current source, I_{C0}. The second chord, C1, starts at current I_{P1}, (known as the pedestal current), and is generated from a current source, I_{C1}, which is twice the value of I_{C0}. The next chord current source, I_{C2}, starts at a pedestal current I_{P2} and has a total value equal to four times I_{C0}. This process continues with each chord N having a total chord current equal to $2^N I_{C0}$ and starting at a pedestal current which equals the summation of all currents in the lower chords:

$$I_{PN} = \sum_{M=0}^{N-1} (I_{CM} + 1.5 \cdot I_M) = 16.5 \sum_{M=0}^{N-1} I_M, \ (I_{P0} = 0),$$

where I_M is the step current value in chord M.

The generation of the pedestal current by summing the lower chords ensures monotonic behavior in the transition between chords. The selection of the proper step within the given chord is accomplished by routing the chord current, I_{CN}, through a step generator which chooses the proper fraction of the chord current necessary to generate the selected number of steps. The resulting net output current I_{OUT}, can be expressed in terms of step currents, I_N, corresponding to the chord N:

$$I_{OUT} = I_{PN} + S \cdot I_N = (16.5 \sum_{M=0}^{N-1} I_M) + S \cdot I_N, \ (I_{P0} = 0),$$

where S = step number = 0, 1, . . . , 15 and N = chord number = 0, 1, . . . , 7.

The circuit has 9 digital inputs, an 8-bit word and a control bit. The 8-bit digital input word is broken into three parts. The first bit is the sign bit and specifies whether the output lies in the positive or negative portion of the curve. The next three bits define which of the 8 chords is to be selected. This three bit field has a value designated as N which is between 0 and 7. The last four bits specify one of the sixteen steps and has a value equal to S. The control bit is the E/$\overline{D}$ signal which controls the output switching.

The chord generator is the key element in the DAC. It must generate eight binary weighted chord currents and is similar to an 8-bit linear DAC. The detailed schematic, shown in Figure 8, shows a master/slave ladder arrangement biased from a reference amplifier and transistor. The reference amplifier forces the base voltage of the reference transistor, (Q_0), to the value required to sink the reference current. This voltage will bias the master ladder so that Q1 runs at $2 \cdot I_{REF}$, Q2 at I_{REF}, Q3 at $.5 \cdot I_{REF}$, and Q4A and Q4B at $.25 \cdot I_{REF}$ each. The slave array uses a binary weighted resistor array to generate the lower four chord currents by dividing the current from Q4B. An 8-bit linear DAC does not require the resistor array in the slave ladder but the Companding DAC does, in order to ensure 12-bit linearity in Chord 0. The LSB current in an AmDAC-08 is 8μA ±4μA while the Chord 0 current source in an Am6070 has a value of 8μA ±.5μA.

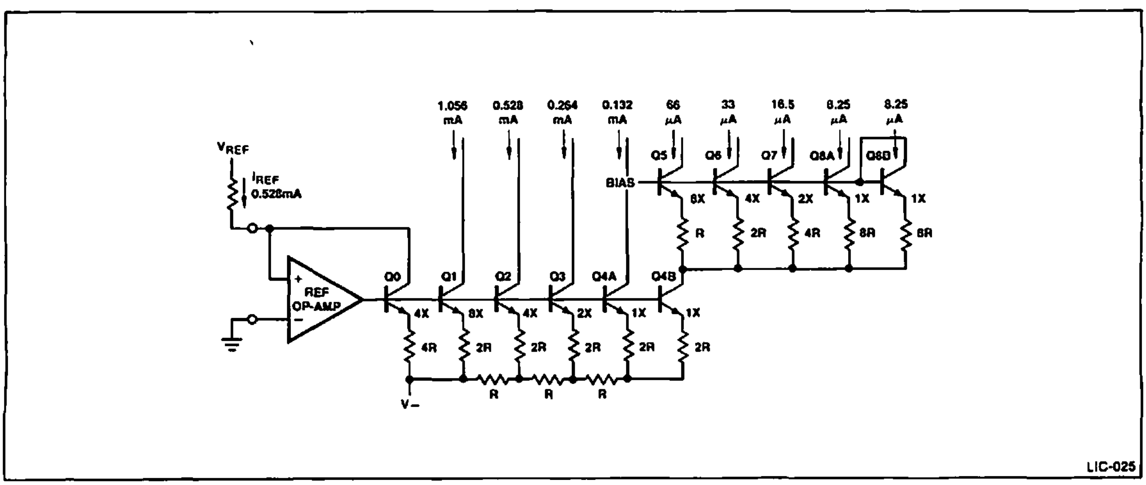


Fig. 8. Chord Current Generator Diagram (Indicated current values correspond to the μ-law DAC).

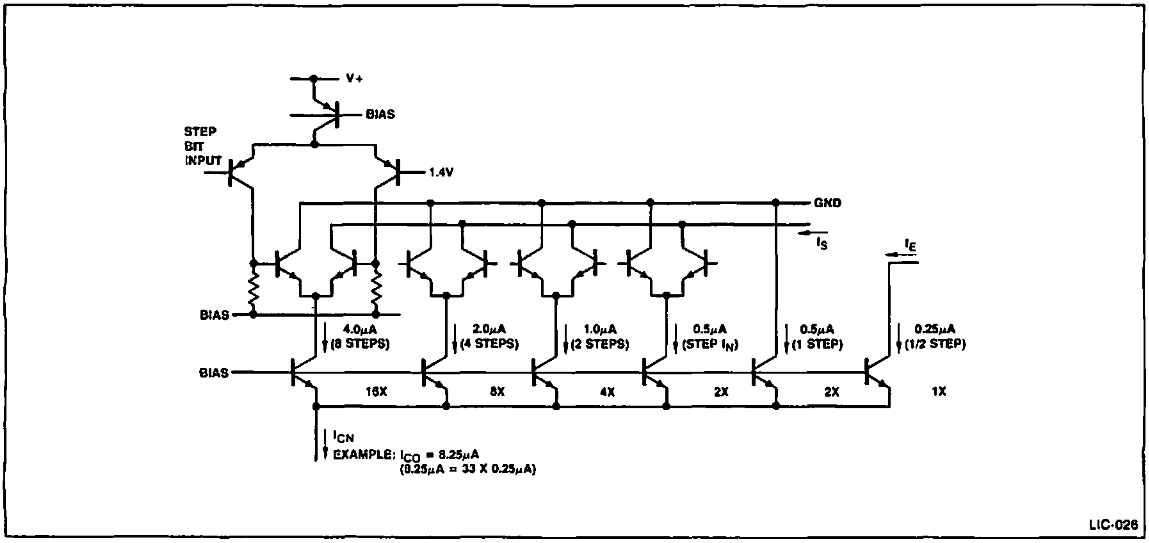


Fig. 9. μ-Law Step Current Generator.

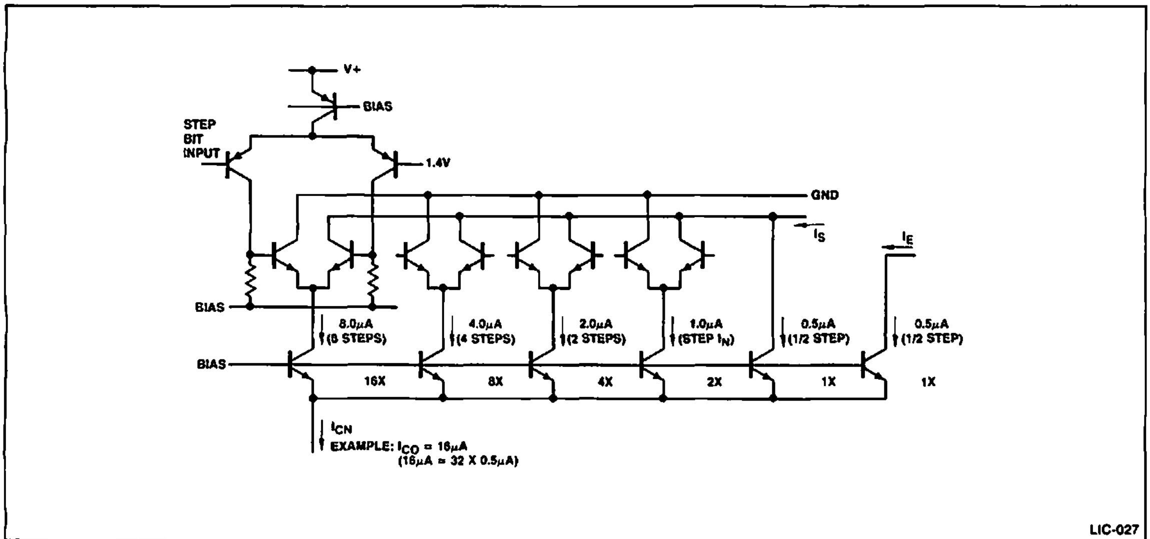


Fig. 10. A-Law Step Current Generator.

The chord select inputs, B1, B2, B3, control a one of eight decoder that selects one of the chords, routes that chord current source to the step generator and switches all the lower order chord current sources to the pedestal generator.

The step generator for the μ-law characteristic is shown in detail in Figure 9. This circuit divides the total chord current source, I_{CN}, into 33 equal parts, and the step current value, I_N, is equal to 2/33 of the chord current source. The 33 parts accommodate the required 1.5 step transition between chords, so that the total internal chord current source is equal to 16.5 steps. The step generator is similar to a four bit DAC but has six current source outputs to generate 8, 4, 2, 1, 1 and 1/2 step currents. This current division can be done using emitter area scaling with enough accuracy to meet the monotonicity and linearity specifications without the use of emitter resistors. The four step bit inputs can choose from 0 to 15 steps to be switched into the output summing network. The 1/2 step current is used as the encode offset current in the encode mode and will track the value of the chord current. When the transition to the next chord is made, the full chord current is switched to the pedestal generator causing a change in the output of 1.5 steps, i.e., from 15 steps to 16.5 steps. The step selector uses a fully differential current switch to ensure high speed performance. This switch does not require capacitive charging and discharging of low current nodes and has a nearly constant 40ns propagation delay over the dynamic range of the varying chord currents, from the first step current on chord 0 of .5μA to the last step current on chord 7 of .5mA.

The output summing network sums the outputs of the pedestal generator, step generator, and encode current, and routes the current to the output selected by the combination of SB and $E/\overline{D}$. If the $E/\overline{D}$ input is high, the encode current, I_{EN}, is summed with the step and pedestal currents and is routed to $I_{OE(+)}$, if SB is 1, or to $I_{OE(-)}$, if SB is 0. If $E/\overline{D}$ is low, only the step and pedestal currents are summed and sent to the output; the output current is routed to $I_{OD(+)}$ or $I_{OD(-)}$ depending on the state of SB. Only one output will be active and the other outputs will be in a high impedance, off, state.

Generation of the μ-Law and A-Law Characteristics

The μ-law and A-law devices have similar characteristics which differ in the chords near zero. In the μ-law device, the step size doubles when chord 0 ends and chord 1 begins and the first step of chord zero is equal to zero, and the points for positive and negative zero are the same. In the A-law curve, the step size does not change between chord 0 and chord 1. The first two chords are colinear and the step size does not start doubling until chord 2. Additionally, the A-law curve has a 1/2 step offset at the zero point so that positive and negative zero are not equal. These differences in the two companding laws are relatively minor and the two laws can be generated from the same integrated circuit with only minor modifications.

The μ-law curve is generated using the earlier described step generator. If step size in the first chord is set to be .5μA, the internal chord 0 current source must be 8.25μA (16.5 x .5μA). Each succeeding internal chord current source doubles in value so that the last two chord current sources are 528μA and 1056μA. The reference current is equal to 1/2 the largest current source, so the required reference current is 528μA. The full scale output current can be calculated by summing all the internal current sources and subtracting 1.5 steps from the most significant chord, because the full scale current output requires only 15 steps out of the available 16.5 steps to be switched into the output. This gives a full scale current of 2007.75μA. The output current for any point on the companding curve can be calculated in terms of the internal chord 0 source, 8.25μA, and its step value, .5μA, using the following formula:

$$I_{N,S} = ((2^N - 1) \cdot 8.25\mu A) + (S \cdot 2^N \cdot 5\mu A)$$

where **N** represents the chord number and S the step number. The first term represents the pedestal current value; the second term the value of the steps in the selected chord.

The A-law curve is generated by using the step generator shown in Figure 10. The internal chord current source is divided into 32 equal parts with current source values of 8, 4, 2, 1, 1/2 and 1/2 steps. The zero offset is generated by summing a 1/2 step current with the output of the step generator independent of input code. The range of output values of the step generator is from 1/2 step to 15.5 steps, and the internal chord current source has a value equal to 16 steps. The 1.5 step transition is accomplished by switching the total internal chord current source to the pedestal generator, i.e., adds 1/2 step, (the encode current I_{EN}), and summing the 1/2 step offset current from the next higher chord, which is the same as one step on the lower chord.

The A-law Companding DAC doubles the size of the chord 0 current source I_{C0} from the μ-law I_{C0} value by connecting the collector of Q8B to Q8A instead of its base as indicated in Figure 8, so that it is equal to the chord 1 current source. The reference current is adjusted to set the first chord step size to 1μA and the internal chord 0 current source value to 16μA. The last two chords will have internal current source values of 512μA and 1024μA each. The reference current required to bias the chord generator is 512μA. The full scale output current can be calculated by summing all the internal chord current sources and subtracting 1/2 step from the last chord, because only 15.5 steps of the 16 steps in the last chord are switched to the output. The full scale current is nominally 2016μA. The current at any point on the A-law companding curve can be calculated by using the following formula:

$$I_{N,S} = (2S+1) \cdot .5\mu A, \text{ for } N=0, \text{ and}$$
$$= (2^{N-1} \cdot 16.5\mu A) + (2^{N-1} \cdot S \cdot 1\mu A), \text{ for } \mathbf{N} \geqslant 1.$$

Output Current Tables

All output current values on the A-law transfer characteristic curve are higher than corresponding μ-law current values, because of the larger step sizes in chord 0 for the A-law characteristic. The different step sizes in chord 0 were originally suggested by the International Telegraph and Telephone

TABLE 1
NORMALIZED A-LAW DECODER OUTPUT
(SIGN BIT EXCLUDED)

STEP (S)	CHORD (C)							
	0	1	2	3	4	5	6	7
0	1	33	66	132	264	528	1056	2112
1	3	35	70	140	280	560	1120	2240
2	5	37	74	148	296	592	1184	2368
3	7	39	78	156	312	624	1248	2496
4	9	41	82	164	328	656	1312	2624
5	11	43	86	172	344	688	1376	2752
6	13	45	90	180	360	720	1440	2880
7	15	47	94	188	376	752	1504	3008
8	17	49	98	196	392	784	1568	3136
9	19	51	102	204	408	816	1632	3264
10	21	53	106	212	424	848	1696	3392
11	23	55	110	220	440	880	1760	3520
12	25	57	114	228	456	912	1824	3648
13	27	59	118	236	462	944	1888	3776
14	29	61	122	244	488	976	1952	3904
15	31	63	126	252	504	1008	2016	4032
STEP SIZE	2	2	4	8	16	32	64	128

TABLE 2
NORMALIZED μ-LAW DECODER OUTPUT
(SIGN BIT EXCLUDED)

STEP (S)	CHORD (C)							
	0	1	2	3	4	5	6	7
0	0	33	99	231	495	1023	2079	4191
1	2	37	107	247	527	1087	2207	4447
2	4	41	115	263	559	1151	2335	4703
3	6	45	123	279	591	1215	2463	4959
4	8	49	131	295	623	1279	2591	5215
5	10	53	139	311	655	1343	2719	5471
6	12	57	147	327	687	1407	2847	5727
7	14	61	155	343	719	1471	2975	5983
8	16	65	163	359	751	1535	3103	6239
9	18	69	171	375	783	1599	3231	6495
10	20	73	179	391	815	1663	3359	6751
11	22	77	187	407	847	1727	3487	7007
12	24	81	195	423	879	1791	3615	7263
13	26	85	203	439	911	1855	3743	7519
14	28	89	211	455	943	1919	3871	7775
15	30	93	219	471	975	1983	3999	8031
STEP SIZE	2	4	8	16	32	64	128	256

TABLE 3
IDEAL A-LAW DECODER OUTPUT VALUES EXPRESSED IN dB DOWN FROM OVERLOAD LEVEL (+3dBmo)

STEP	CHORD							
	0	1	2	3	4	5	6	7
0	−69.11	−38.74	−35.72	−26.70	−20.68	−14.66	−8.64	−2.62
1	−59.57	−38.23	−32.21	−28.19	−20.17	−14.15	−8.13	−2.11
2	−55.13	−37.75	−31.73	−25.71	−19.68	−13.66	−7.64	−1.62
3	−52.21	−37.29	−31.27	−25.25	−19.23	−13.21	−7.19	−1.17
4	−50.03	−36.85	−30.83	−24.81	−18.79	−12.77	−6.75	−0.73
5	−48.28	−36.44	−30.42	−24.40	−18.38	−12.36	−6.34	−0.32
6	−46.83	−36.05	−30.03	−24.00	−17.98	−11.96	−5.94	+0.08
7	−45.59	−35.67	−29.65	−23.63	−17.61	−11.59	−5.57	+0.46
8	−44.50	−35.31	−29.29	−23.27	−17.24	−11.22	−5.20	+0.82
9	−43.54	−34.96	−28.94	−22.92	−16.90	−10.88	−4.86	+1.16
10	−42.67	−34.62	−28.60	−22.58	−16.56	−10.54	−4.52	+1.50
11	−41.88	−34.30	−28.28	−22.26	−16.24	−10.22	−4.20	+1.82
12	−41.15	−33.99	−27.97	−21.95	−15.93	−9.91	−3.89	+2.13
13	−40.48	−33.69	−27.67	−21.65	−15.63	−9.61	−3.59	+2.43
14	−39.86	−33.40	−27.38	−21.36	−15.34	−9.32	−3.30	+2.72
15	−39.28	−33.12	−27.10	−21.08	−15.06	−9.04	−3.02	+3.00

TABLE 4
IDEAL μ-LAW DECODER OUTPUT VALUES EXPRESSED IN dB DOWN FROM OVERLOAD LEVEL (+3dBmo)

STEP	CHORD							
	0	1	2	3	4	5	6	7
0	−	−44.73	−35.18	−27.82	−21.20	−14.90	−8.74	−2.65
1	−69.07	−43.73	−34.51	−27.24	−20.66	−14.37	−8.22	−2.13
2	−63.05	−42.84	−33.88	−26.70	−20.15	−13.87	−7.73	−1.65
3	−59.53	−42.03	−33.30	−26.18	−19.66	−13.40	−7.27	−1.19
4	−57.03	−41.29	−32.75	−25.70	−19.21	−12.96	−6.83	−0.75
5	−55.10	−40.61	−32.24	−25.24	−18.77	−12.53	−6.41	−0.33
6	−53.51	−39.98	−31.75	−24.80	−18.36	−12.13	−6.01	+0.06
7	−52.17	−39.39	−31.29	−24.39	−17.96	−11.74	−5.63	+0.44
8	−51.01	−38.84	−30.85	−23.99	−17.58	−11.37	−5.26	+0.81
9	−49.99	−38.32	−30.44	−23.61	−17.22	−11.02	−4.91	+1.16
10	−49.07	−37.83	−30.04	−23.25	−16.87	−10.68	−4.57	+1.49
11	−48.25	−37.37	−29.66	−22.90	−16.54	−10.35	−4.25	+1.82
12	−47.49	−36.93	−29.29	−22.57	−16.22	−10.03	−3.93	+2.13
13	−46.80	−36.51	−28.95	−22.25	−15.91	−9.73	−3.63	+2.43
14	−46.15	−36.11	−28.61	−21.94	−15.61	−9.43	−3.34	+2.72
16	−45.55	−35.73	−28.29	−21.63	−15.32	−9.15	−3.06	+3.00

Consultive Committee (CCITT), in its recommendation for the encoding laws in Pulse Code Modulation communication systems for voice frequency signals of commercial quality.

This recommendation contains several different tables with information for A-law and μ-law encoding requirements. The most important pair of tables contain all 128 distinctive decoder output current values expressed in normalized units. The normalized current output values for A-law and μ-law Companding DACs are presented in Tables 1 and 2, respectively. Step 0 of chord 0 in the A-law table is equal to the value of one normalized unit, whereas the corresponding normalized zero current value in the μ-law table is zero. The actual size of this normalized unit is NOT REQUIRED TO BE THE SAME for A-law and for μ-law, and entries in Tables 1 and 2 should not be used for any comparison of the two encoding laws. Each table, independently, provides the information for a particular encoding law about required relationships between the output current magnitudes. In addition, the input data coding for Table 2, which contains entries for the μ-law normalized output values, is the one's complement of the input data codes suggested by the original CCITT and Bell D3 specification. However, data input coding shown in Tables 1 and 2 is accepted as standard input data coding in order to have consistent data coding for μ-law and A-law Companding DACs. The maximum normalized current values in Tables 1 and 2 are 4032 and 8031, respectively, and these values can be easily derived by summing all of the 128 normalized steps.

Additional conditions beyond the two maximum normalized values are related to the ratios, in μA, between the amplitudes corresponding to full scale current values, and the amplitudes of output currents which are chosen as the reference outputs for A-law and for μ-law decoding devices. These reference outputs are generated as sinusoidal waveforms of 1kHz by applying a periodic sequence of eight 8-bit data words at the Companding DAC's inputs at an 8kHz rate. These sequences are specified separately for both encoding laws. The signal level at the peaks of these reference sinusoidal waveforms is chosen as the reference 0dB level. This level is implied to be the same for both encoding laws. The dB levels, calculated by using the peaks of the 1kHz sinusoidal waveforms with amplitudes which correspond to the theoretical maximum output current values, are specified to be +3.14dB and +3.17dB above the common reference level for the A-law and μ-law decoding devices, respectively. The small difference in the specified theoretical maximum output current levels implies a very small difference between actual full scale current values for A-law and μ-law decoders. In practice, the actual level for the full scale output current values for both laws is set to be +3.00dB above the reference 0dB level. The ideal decoder output values expressed in dB down from the full scale current output for A-law and μ-law are presented in Tables 3 and 4. The reference 0dB level can be found in these tables between steps 5 and 6 on chord 7. Comparison of the numbers corresponding to step 1 in chord 0 shows a difference between the two encoding laws with respect to the output dynamic ranges. The output dynamic range is 62.57dB for A-law, (+3.00dB to −59.57dB), and 72.07dB for μ-law, (+3.00dB to −69.07dB).

In order to make the electrical designs of A-law and μ-law Companding DACs as similar as possible, the normalized unit value of current in Table 1, A-law table, is chosen to be 0.5μA and the normalized unit current quantity in Table 2, μ-law table, is chosen to be 0.25μA. These different "unit" values will cause the steps in chord 0 for A-law Companding DACs to be twice as large as the corresponding μ-law device step sizes. Consequently, the ideal full scale absolute current values corresponding to 4032 and 8031 normalized units are 2016μA for A-law and 2007.75μA for μ-law DACs. Tables 5 and 6 contain all 128 absolute decoder output current values in μA. These tables can be further expressed in terms of percent of full scale current output, which may be important for some "percentage" oriented applications. Tabulated summaries of step and chord endpoint sizes which can be extracted from Tables 1 through 6 are presented in Tables 7 and 8. The last column in these tables points out that the best resolution and accurac. e /e achieved in chord 0 of the Companding DAC's transfer function.

The output current values presented in Tables 5 and 6 are ideal output currents with ideal reference currents of 528μA and 512μA, respectively. The output current deviations for the communication application of Companding DACs are specified by the compandor tracking system requirements which are illustrated for both decoders in Figures 11 and 12. In both figures a dotted line represents a total gain deviation, in dB, for

TABLE 5
IDEAL A-LAW DECODER OUTPUT CURRENT IN MICROAMPS (SIGN BIT EXCLUDED)

STEP	CHORD							
	0	1	2	3	4	5	6	7
0	.500	16.500	33.000	66.000	132.00	264.00	528.00	1056.00
1	1.500	17.500	35.000	70.000	140.00	280.00	560.00	1120.00
2	2.500	18.500	37.000	74.000	148.00	296.00	592.00	1184.00
3	3.500	19.500	39.000	78.000	156.00	312.00	624.00	1248.00
4	4.500	20.500	41.000	82.000	164.00	328.00	656.00	1312.00
5	5.500	21.500	43.000	86.000	172.00	344.00	688.00	1376.00
6	6.500	22.500	45.000	90.000	180.00	360.00	720.00	1440.00
7	7.500	23.500	47.000	94.000	188.00	376.00	752.00	1504.00
8	8.500	24.500	49.000	98.000	196.00	392.00	784.00	1568.00
9	9.500	25.500	51.000	102.000	204.00	408.00	816.00	1632.00
10	10.500	26.500	53.000	106.000	212.00	424.00	848.00	1696.00
11	11.500	27.500	55.000	110.000	220.00	440.00	880.00	1760.00
12	12.500	28.500	57.000	114.000	228.00	456.00	912.00	1824.00
13	13.500	29.500	59.000	118.000	236.00	472.00	944.00	1888.00
14	14.500	30.500	61.000	122.000	244.00	488.00	976.00	1952.00
15	15.500	31.500	63.000	126.000	252.00	504.00	1008.00	2016.00
STEP SIZE	1	1	2	4	8	16	32	64

TABLE 6
IDEAL μ-LAW DECODER OUTPUT CURRENT IN MICROAMPS (SIGN BIT EXCLUDED)

STEP	CHORD							
	0	1	2	3	4	5	6	7
0	.000	8.250	24.750	57.750	123.75	255.75	519.75	1047.75
1	.500	9.250	26.750	61.750	131.75	271.75	551.75	1111.75
2	1.000	10.250	28.750	65.750	139.75	287.75	583.75	1175.75
3	1.500	11.250	30.750	69.750	147.75	303.75	615.75	1239.75
4	2.000	12.250	32.750	73.750	155.75	319.75	647.75	1303.75
5	2.500	13.250	34.750	77.750	163.75	335.75	679.75	1367.75
6	3.000	14.250	36.750	81.750	171.75	351.75	711.75	1431.75
7	3.500	15.250	38.750	85.750	179.75	367.75	743.75	1495.75
8	4.000	16.250	40.750	89.750	187.75	383.75	775.75	1559.75
9	4.500	17.250	42.750	93.750	195.75	399.75	807.75	1623.75
10	5.000	18.250	44.750	97.750	203.75	415.75	839.75	1687.75
11	5.500	19.250	46.750	101.750	211.75	431.75	871.75	1751.75
12	6.000	20.250	48.750	105.750	219.75	447.75	903.75	1815.75
13	6.500	21.250	50.750	109.750	227.75	463.75	935.75	1879.75
14	7.000	22.250	52.750	113.750	235.75	479.75	967.75	1943.75
15	7.500	23.250	54.750	117.750	243.75	495.75	999.75	2007.75
STEP SIZE	.5	1	2	4	8	16	32	64

TABLE 7
A-LAW DECODER STEP SIZE AND CHORD SIZE SUMMARY

Chord	Step Size Normalized to Full Scale	Chord Endpoints Normalized to Full Scale	Step Size in μA with 2016μA F. S.	Chord Endpoints in μA with 2016μA F. S.	Step Size as a % of Full Scale	Chord Endpoints as a % of Full Scale	Chord Endpoints in dB Down from Full Scale	Resolution & Accuracy of Equivalent Binary DAC
0	2	31	1.0	15.5	0.05%	0.77%	−42.28	Sign + 11 Bits
1	2	63	1.0	31.5	0.05%	1.56%	−36.12	Sign + 11 Bits
2	4	126	2.0	63.0	0.1%	3.13%	−30.10	Sign + 10 Bits
3	8	252	4.0	126.0	0.2%	6.25%	−24.08	Sign + 9 Bits
4	16	504	8.0	252.0	0.4%	12.5%	−18.06	Sign + 8 Bits
5	32	1008	16.0	504.0	0.8%	25.0%	−12.04	Sign + 7 Bits
6	64	2016	32.0	1008.0	1.6%	50.0%	−6.02	Sign + 6 Bits
7	128	4032	64.0	2016.0	3.2%	100%	0	Sign + 5 Bits

TABLE 8
μ-LAW DECODER STEP SIZE AND CHORD SIZE SUMMARY

Chord	Step Size Normalized to Full Scale	Chord Endpoints Normalized to Full Scale	Step Size in μA with 2007.75μA FS	Chord Endpoints in μA with 2007.75μA FS	Step Size as a % of Full Scale	Chord Endpoints as a % of Full Scale	Chord Endpoints in dB Down from Full Scale	Resolution & Accuracy of Equivalent Binary DAC
0	2	30	0.5	7.5	0.025%	0.37%	−48.55	Sign + 12 Bits
1	4	93	1.0	23.25	0.05%	1.16%	−38.73	Sign + 11 Bits
2	8	219	2.0	54.75	0.1%	2.73%	−31.29	Sign + 10 Bits
3	16	471	4.0	117.75	0.2%	5.86%	−24.63	Sign + 9 Bits
4	32	975	8.0	243.75	0.4%	12.1%	−18.32	Sign + 8 Bits
5	64	1983	16.0	495.75	0.8%	24.7%	−12.15	Sign + 7 Bits
6	128	3999	32.0	999.75	1.6%	49.8%	−6.06	Sign + 6 Bits
7	256	8031	64.0	2007.75	3.2%	100%	0	Sign + 5 Bits

various signal levels which can be distributed over the encoder and decoder portions of a "one way" communication system. It is understood that encoder and decoder system portions are implemented with corresponding Companding DACs. For the Bell D3 system μ-law tracking specification, the −37dBmo and −50dBmo output current levels can be found between steps 11 and 12 on chord 1, and steps 8 and 9 on chord 0, respectively. For the CCITT A-law compandor tracking specification, the −40dBmo, −50dBmo, and −55dBmo output current levels can be found in the corresponding A-law tables between steps 13 and 14 on chord 0, steps 4 and 5 on chord 0, and steps 2 and 3 on chord 0, respectively. Conversion of the requirements imposed by Figures 11 and 12 to absolute current values produces corresponding absolute decode output current tables with minimum, ideal and maximum values specified for each step.

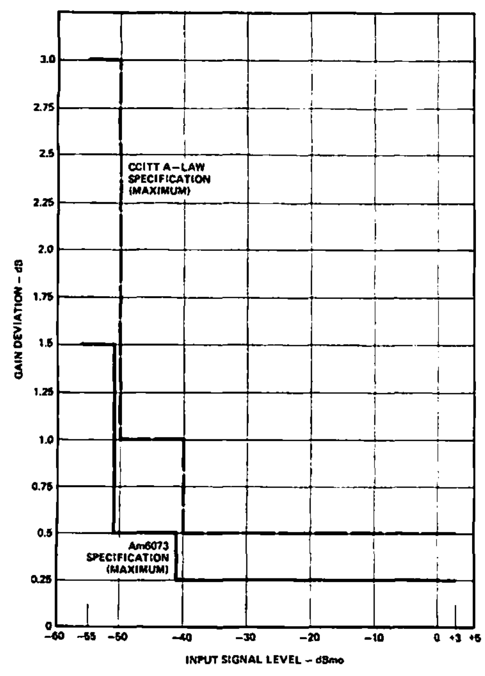


Fig. 11. CCITT A-Law Compandor Tracking Specification.

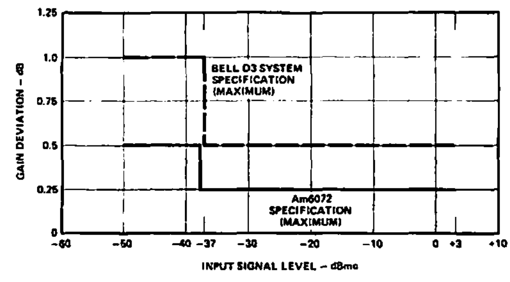


Fig. 12. Bell D3 System Compandor Tracking Specification.

TABLE 9
ABSOLUTE DECODER OUTPUT CURRENT LIMITS IN μA
CONFORMING TO BELL D3 COMPANDOR TRACKING SPECIFICATIONS

STEP NO.	CHORD NO. 0	1	2	3	4	5	6	7
	−.250	7.789	24.048	56.112	120.24	248.49	505.00	1018.02
0	.000	8.250	24.750	57.750	123.75	255.75	519.75	1047.75
	.250	8.739	25.473	59.436	127.36	263.22	534.93	1078.34
	.250	8.733	25.991	59.998	128.01	264.04	536.10	1080.21
1	.500	9.250	26.750	61.750	131.75	271.75	551.75	1111.75
	.750	9.798	27.531	63.553	135.60	279.69	567.86	1144.21
	.750	9.677	27.934	63.885	135.79	279.59	567.19	1142.39
2	1.000	10.250	28.750	65.750	139.75	287.75	583.75	1175.75
	1.250	10.857	29.590	67.670	143.83	296.15	600.80	1210.08
	1.250	10.621	29.878	67.771	143.56	295.13	598.28	1204.58
3	1.500	11.250	30.750	69.750	147.75	303.75	615.75	1239.75
	1.750	11.917	31.648	71.787	152.06	312.62	633.73	1275.95
	1.750	11.565	31.821	71.658	151.33	310.68	629.37	1266.76
4	2.000	12.250	32.750	73.750	155.75	319.75	647.75	1303.75
	2.250	12.976	33.706	75.904	160.30	329.09	666.66	1341.82
	2.250	12.509	33.764	75.544	159.10	326.22	660.46	1328.94
5	2.500	13.250	34.750	77.750	163.75	335.75	679.75	1367.75
	2.750	14.035	35.765	80.020	168.53	345.55	699.60	1407.69
	2.750	13.453	35.707	79.431	166.88	341.77	691.56	1391.13
6	3.000	14.250	36.750	81.750	171.75	351.75	711.75	1431.75
	3.250	15.094	37.823	84.137	176.77	362.02	732.53	1473.56
	3.250	14.397	37.651	83.317	174.65	357.32	722.65	1453.31
7	3.500	15.250	38.750	85.750	179.75	367.75	743.75	1495.75
	3.750	16.154	39.882	88.254	185.00	378.49	765.47	1539.43
	3.750	15.341	39.594	87.204	182.42	372.86	753.74	1515.50
8	4.000	16.250	40.750	89.750	187.75	383.75	775.75	1559.75
	4.250	17.213	41.940	92.371	193.23	394.96	798.40	1605.30
	4.248	16.285	41.537	91.090	190.20	388.41	784.83	1577.68
9	4.500	17.250	42.750	93.750	195.75	399.75	807.75	1623.75
	4.767	18.272	43.998	96.488	201.47	411.42	831.34	1671.16
	4.720	17.229	43.480	94.977	197.97	403.95	815.92	1639.87
10	5.000	18.250	44.750	97.750	203.75	415.75	839.75	1687.75
	5.296	19.331	46.057	100.604	209.70	427.89	864.27	1737.03
	5.192	18.173	45.424	98.863	205.74	419.50	847.02	1702.05
11	5.500	19.250	46.750	101.750	211.75	431.75	871.75	1751.75
	5.826	19.812	48.115	104.721	217.93	444.36	897.21	1802.90
	5.664	19.675	47.367	102.750	213.52	435.05	878.11	1764.23
12	6.000	20.250	48.750	105.750	219.75	447.75	903.75	1815.75
	6.356	20.841	50.174	108.838	226.17	460.82	930.14	1868.77
	6.136	20.647	49.310	106.636	221.29	450.59	909.20	1826.42
13	6.500	21.250	50.750	109.750	227.75	463.75	935.75	1879.75
	6.885	21.871	52.232	112.955	234.40	477.29	963.07	1934.64
	6.608	21.619	51.253	110.523	229.06	466.14	940.29	1888.60
14	7.000	22.250	52.750	113.750	235.75	479.75	967.75	1943.75
	7.415	22.900	54.290	117.072	242.63	493.76	996.01	2000.51
	7.080	22.590	53.197	114.409	236.83	481.68	971.39	1950.79
15	7.500	23.250	54.750	117.750	243.75	495.75	999.75	2007.75
	7.944	23.929	56.349	121.188	250.87	510.23	1028.94	2066.38
STEP SIZE	.5	1	2	4	8	16	32	64

The decoder output current values which comply with the Bell D3 compandor tracking requirements are presented in Table 9. A similar table can be generated for the CCITT A-law compandor tracking specification. The corresponding encode output values can be derived from the decode output values by adding a half a step to all entries in a given decode table. The specified limit values include the combined effects of chord end point deviations, step nonlinearity, encode output errors, full scale current deviation from ideal, full scale symmetry error, zero scale current error, full scale drift, and output impedance change over the specified voltage compliance and temperature ranges. The adjacent step current levels in Table 9 for any particular Companding DAC will not overlap, as might be implied from the presented minimum and maximum values, because the device is guaranteed to be monotonic.

If the decode output limits for the μ-law Companding DAC are specified to be $\pm 1/2$ step from the ideal values, Table 9 can be replaced by a similar table. The most important difference between the two tables would be found in the limit values corresponding to the lower step current values in chords 1 through 7. The approximate representations of $\pm 1/2$ step, ± 1 step limits and the corresponding Bell D3 compandor tracking limits in Table 9 are illustrated in Figure 13.

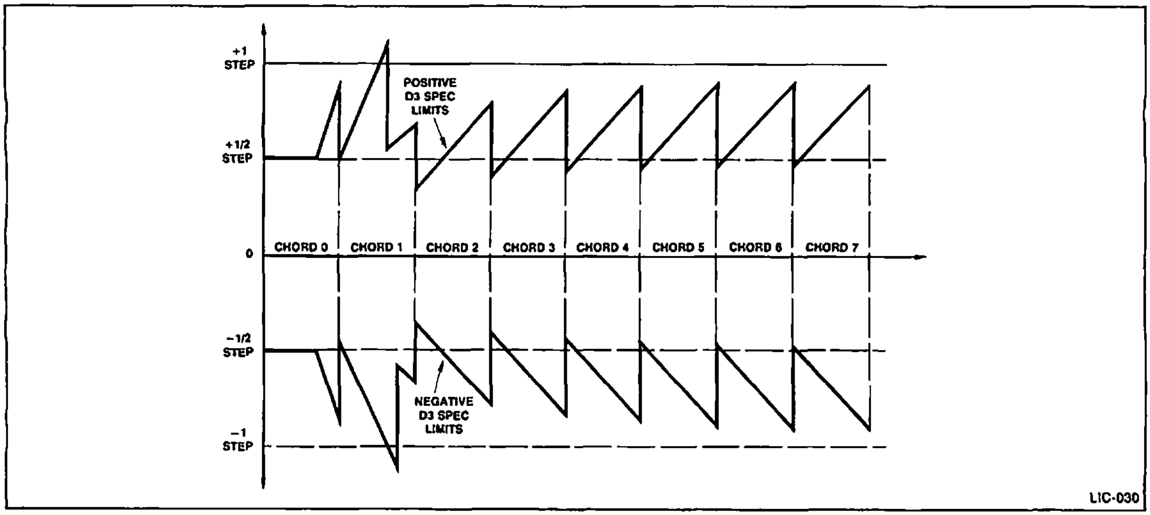


Fig. 13. Output Current Limit Diagrams for D3, ±1/2 Step, and ±1 Step Tolerance Specifications.

Parametric Analysis and Recommendations

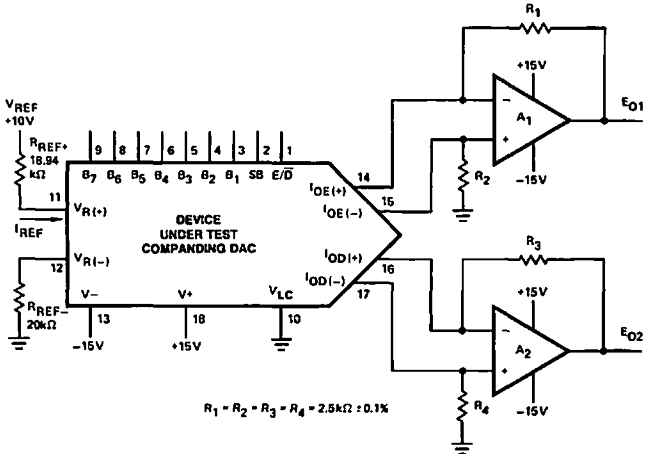
A detailed specification for a digital-to-analog converter should include information about important DAC parameters such as resolution, monotonicity, dynamic range, settling time, nonlinearity, full scale and zero scale current errors, gain error, output voltage compliance, input, output and reference signal levels, operating temperature range, power supply range and power dissipation.

The resolution of a DAC is determined by the maximum number of digital input combinations which can be used to generate analog output signals. The resolution for Companding DACs with sign-plus-7 bit digital data input signals is ±128 steps. A converter is monotonic if its analog output always increases with an increase in the digital value of the input data code. Monotonicity for the Am6070/71/72/73 devices, is guaranteed over the full operating temperature range and for both groups of 128 steps. Two parameters which are used to describe nonlinear errors in a DAC's transfer function are the DAC's nonlinearity and the differential nonlinearity error. The nonlinearity of a Companding DAC is defined as the maximum deviation of the actual output values from an ideal piece-wise linear characteristic calculated from measurements of the actual full scale and zero scale current values. These two current measurements can be used to compute the corresponding theoretical chord endpoint values, and nonlinearity is measured as the difference between this calculated transfer characteristic and the actual current values at the output of the DAC. The differential nonlinearity of the device is a measure of how much any single step current value varies with respect to its theoretical value, (calculated from the actual full scale output current). Differential nonlinearity of ±1/2 step will ensure monotonic behavior. These errors and all other transfer function related errors are specified for the Am6070 Companding DAC Family by the limit current values in the corresponding Absolute Decoder Output Current Level Table.

The DAC's current outputs have a very high impedance, and the output current will not change its value significantly with changes in the applied voltage at the DAC's outputs. The output voltage compliance range is defined as the maximum range of voltages, at the DAC's output, that can be sustained while meeting the output current specifications. The absolute maximum output voltage swing, (I_{REF} = 528μA), is specified between V− plus 10V and V− plus 36V, where V− is the Companding DAC's negative power supply. The maximum range for the reference inputs $V_{R(-)}$ and $V_{R(+)}$ is specified to be between the V− and V+ power supply values. The maximum power supply range, V+ to V−, is specified at 36V, and maximum power dissipation for temperatures less than 100°C is rated at 500mW.

The settling time for a DAC is defined as the elapsed time, after an input code transition, required for the DAC's output to reach a final value within specified limits. These limits are generally ±1/2 of the corresponding step current value. The settling time is usually specified for the input code transition from zero scale to full scale value, and for the Companding DAC Am6070 family the typical value is 300ns. However, this is not the worst case transition. Because of the different step sizes, the output current settling error band changes as the chord current changes, becoming smaller for lower chords. Settling times in chord 7 are measured when the output settles within ±32μA of its final value, while settling times in chord 0 are measured when the output settles to within ±.25μA of it's final value. The worst case transition is, therefore, the transition from full scale current down to zero scale current value, and requires a settling time of 4μs for μ-law DACs and 2.5μs for A-law DACs.

The currents of each of the four Companding DAC's analog outputs can be measured using the circuit shown in Figure 14. This circuit contains 4 resistors, R1, R2, R3, R4, and two operational amplifiers, A1 and A2. Resistor tolerances of 0.1% give 0.1% output measurement error (approximately 2μA at full scale). The input offset current of the operational amplifier also increases the output measurement error. This error is most significant near zero scale. The Am101A and Am308 devices, for example, may be used for A1 and A2, since their maximum offset currents which would add directly to the measurement error, are only 10nA and 1nA, respectively. The input offset voltage of the amplifiers, with output resistor values of 2.5kΩ, also contributes to the output measurement error by a factor of 400nA for every mV of offset voltage. Therefore, to minimize this error, the offset voltages of A1 and A2 should be nulled.



LINE SELECTION TABLE

TEST GROUP	$E/\overline{D}$	SB	OUTPUT MEASUREMENT	
1	1	1	$I_{OE}(+)$	(E_{01}/R_1)
2	1	0	$I_{OE}(-)$	(E_{01}/R_2)
3	0	1	$I_{OD}(+)$	(E_{02}/R_3)
4	0	0	$I_{OD}(-)$	(E_{02}/R_4)

Fig. 14. Companding DAC Output Current DC Test Circuit.

The recommended operating range for the reference current I_{REF} is 0.1mA to 1.0mA. The full scale output current, I_{FS}, is a linear function of the reference current, and may be approximated using the equation $I_{FS} = 3.9 \cdot I_{REF}$. This tight relationship alleviates the requirement for trimming the I_{REF} current if the R_{REF} resistors' values are within ±1% of the calculated value. Lower values of I_{REF} will reduce the negative power supply current, and will increase the reference amplifier negative common mode input voltage range. However, the device accuracy specifications are not guaranteed at reference currents below 0.5mA.

The ideal value for the reference current, (V_{REF}/R_{REF}), is 528μA for μ-law and 512μA for A-law Companding DACs. The corresponding ideal full scale decode current values are 2007.75μA and 2016μA, respectively. A percentage change from the ideal I_{REF} value produced by changes in the V_{REF} or R_{REF} values produces the same percentage change in the decode and encode output current values. The positive voltage supply, V+, may be used, with certain precautions, for the positive reference voltage. In this case, the reference resistor $R_{REF(+)}$ should be split into two resistors and their junction bypassed to ground with a capacitor of about 0.01μF. The total resistor value should provide the required reference current. The $R_{REF(-)}$ resistor value should approximately equal the $R_{REF(+)}$ value in order to compensate for errors caused by the reference amplifier's input bias current.

An alternative to the positive reference voltage biasing is the application of a negative voltage to the $V_{R(-)}$ terminal through the resistor $R_{REF(-)}$ with the $R_{REF(+)}$ resistor tied to ground. The advantage of this arrangement is the presence of very high impedance at the $V_{R(-)}$ terminal while the reference current flows from ground through $R_{REF(+)}$ into the $V_{R(+)}$ terminal.

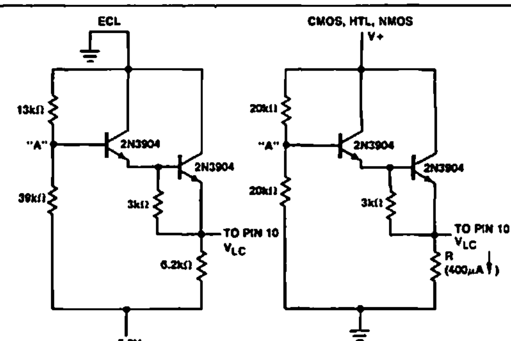
The Companding DAC can be used as a multiplying DAC by varying the reference current. It is important that the reference current have a DC component that guarantees an uninterrupted flow of current INTO the $V_{R(+)}$ terminal. The input reference amplifier has sufficient bandwidth and slew rate, (0.12mA/μs minimum), to handle small signal inputs up to 5% of reference current at frequencies up to 500KHz, and large signal inputs of up to 50% of reference current at frequencies up to 80kHz.

The Companding DAC has a wide output voltage compliance suitable for driving a variety of loads. Using the ideal recommended value for I_{REF} and $V- = -15V$, the positive voltage compliance limit is +18V and the negative voltage compliance limit is −5.0V. For other values of I_{REF} and V−, the negative voltage compliance limit, $V_{OC(-)}$, may be calculated as follows:

$$V_{OC(-)} = (V-) + 2\,(I_{REF} \cdot 1.55k\Omega) + 8.4V,$$

where 1.55kΩ and 8.4V are equivalent worst case values for the Companding DAC.

The V_{LC} input controls the input logic threshold voltage, allowing the device to interface with various logic families. This input should be placed at a potential which is 1.4V below the desired logic input switching threshold. Two external discrete circuits which provide this function for non-TTL driven inputs are shown in Figure 15. For TTL-level logic inputs, the V_{LC} input should be grounded. If negative voltages are applied at the digital logic inputs, they must have a value which is more positive than −5V.



Notes: 1. Set the voltage "A" to the desired logic input switching threshold.
2. Allowable range of logic threshold is typically −5V to +13.5V when operating the companding DAC on ± 15V supplies.

LIC-032

Fig. 15. Interfacing Circuits for ECL, CMOS, HTL and NMOS Logic Inputs.

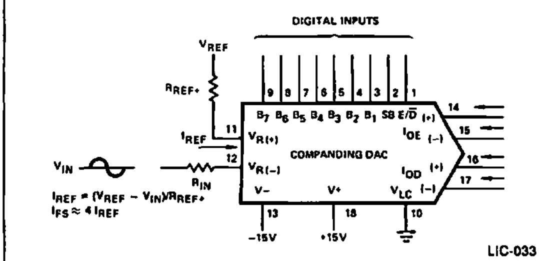
With the V− voltage between −15V and −11V, the $V_{OC(-)}$ value, the input reference common mode voltage range, and the logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− value chosen. With V+ between +5V and +15V, the reference amplifier common mode positive voltage range and the V_{LC} input values are reduced by an amount equivalent to the difference between +15V and the V+ value chosen.

TYPICAL CIRCUIT APPLICATIONS

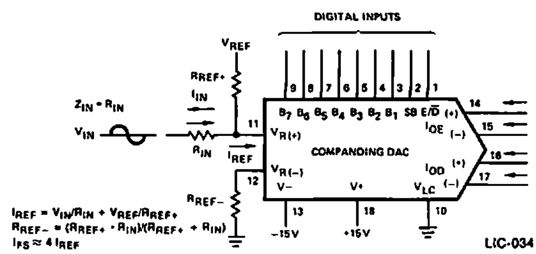
Basic Circuit Connections

The Companding DAC belongs to the class of multiplying D to A converters with true current outputs. The input reference current can be generated by a unipolar constant reference voltage source or by a bipolar AC reference voltage. The applied bipolar reference source usually modulates the reference current, I_{REF}, supplied from the constant reference voltage as shown in Figure 16. Figure 16a shows a high input impedance configuration where the bipolar input signal V_{IN} modulates the voltage level at the $V_{R(+)}$ input by forcing the voltage across R_{REF} to be $V_{REF} - V_{IN}$, which in turn modifies I_{REF}. Figure 16b shows low input impedance connections, where I_{REF} equals the sum of the DC reference current from V_{REF} and the AC input current from V_{IN}. For both low impedance and high impedance connections, the minimum reference current value at the reference input, $V_{R(+)}$ should be at least 0.1mA and the maximum value should not exceed 1.0mA.

The wide output voltage compliance range, (−5V to +18V *with* I_{REF} = 528μA and V− = −15V), allows a variety of loads to be driven. Two typical connections are shown in Figure 17. Voltage output relationships for single ended and differential resistive output connections are described in the output voltage table of Figure 17a. The reference current in this resistive load example is set to be 528μA (μ-law Companding DAC). The resulting negative voltage generated by the currents at the outputs A, B, and C, does not exceed the minimum value of −5V, which corresponds to the lower limit of the output voltage compliance range. In the example with balanced load connections, the sum of the common mode voltage, V_{CM}, and the differential voltage across the load should also be within the −5V and +18V output voltage compliance limit.

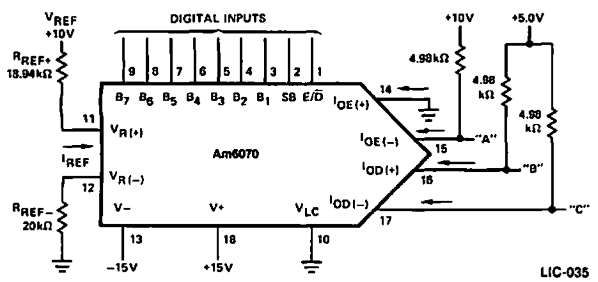


a. High Input Impedance Connection.



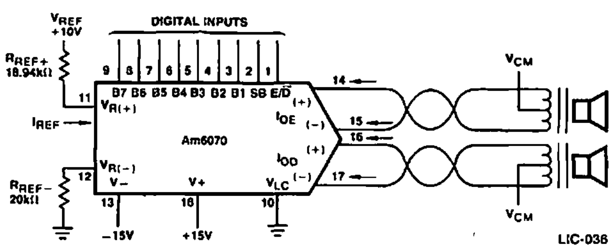
b. Low Input Impedance Connection.

Fig. 16. Companding DAC's Multiplying Connections.



INPUT CODE (E/D̄, SB, B_1, . . ., B_7)	OUTPUT VOLTAGE (V) "A"	"B"	"C"	DIFF
10 111 1111	0			
10 110 1111	+5.02	N/A	N/A	N/A
10 000 0000	+10.00			
01 111 1111		−5.00	+5.00	−10.00
01 110 1111		+0.02	+5.00	−4.98
01 000 0000	N/A	+5.00	+5.00	0
00 000 0000		+5.00	+5.00	0
00 110 1111		+5.00	+0.02	+4.98
00 111 1111		+5.00	−5.00	+10.00

a. Resistive Output Connections.

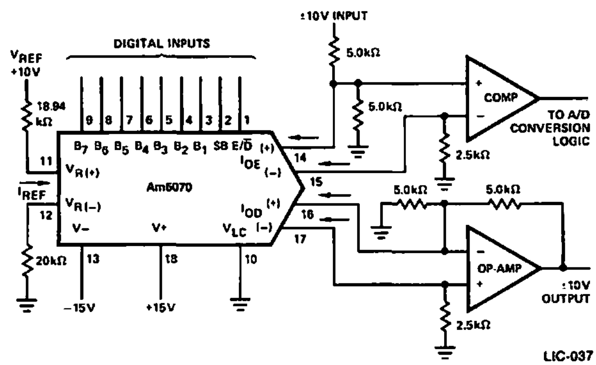


b. Balanced Load Connections.

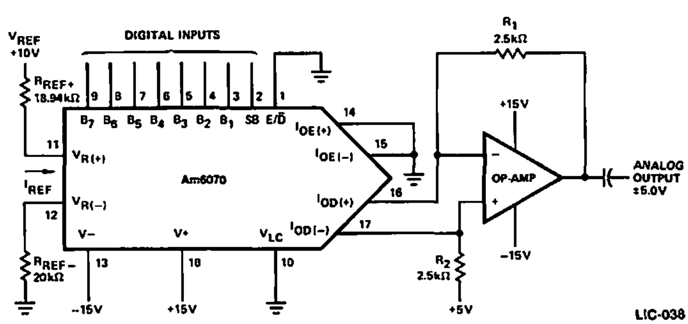
Fig. 17. Companding DAC's Output Connections.

Operational amplifiers and/or comparators can be driven by Companding DACs. The circuits shown in Figure 18 demonstrate various voltage ranges which can be achieved at the outputs of operational amplifiers. The circuit in Figure 18a provides 0V at the op-amp output whenever the E/$\overline{D}$ input is set to logic 1. When the circuit is in the decode mode, E/$\overline{D}$ = 0 the output voltage polarity is determined by the sign bit input level. With the sign bit set low, the $I_{OD(-)}$ output is active and the corresponding full scale output current, $I_{FS} \approx$ 2mA, will generate a maximum negative voltage of −5V at the op-amp's positive input. The chosen resistor values and their connections provide the op-amp with a gain of 2 and a maximum negative output voltage of −10V. With the sign bit set high the $I_{OD(+)}$ output is active and the op-amp's negative input will be held at virtual ground. With a full scale current of 2mA flowing into the $I_{OD(+)}$ pin, the op-amp will act as a transconductance amplifier supplying 2mA to the $I_{OD(+)}$ pin via the 5kΩ feedback resistor. This current will generate a maximum of +10V at the output, which will make the total output voltage swing between −10V and +10V. The circuit in Figure 18b similarly provides a voltage swing between −5V and +5V across the output capacitor. The output dynamic range expander circuit connections, shown in Figure 19, extend the μ-law Companding DAC's dynamic range from 72dB to 78dB. The A-law Companding DAC's dynamic range can be similarly increased from 62dB to 66dB. In this circuit, the outputs $I_{OD(+)}$ and $I_{OE(+)}$ are tied together, and $I_{OD(-)}$ and $I_{OE(-)}$ are tied together; the E/$\overline{D}$ input is used as a fifth step which represents the least significant digital data input, and provides the desired interleaving between the encode and decode current levels. Each chord now contains 32 uniform steps, with the smallest step size value 0.25μA and the largest value 32μA. The resulting full scale current is equal to the corresponding full scale encode current value, and the ratio between the full scale current value and the smallest current step value, I_{FS}/0.25, exceeds 8000 for the μ-law Companding DAC. The smallest and the largest current step sizes will generate 0.625mV and 80mV changes, respectively, at the op-amp output.

Digital inputs SB and E/$\overline{D}$ can be used together with data inputs B1 through B7 to provide an output multiplexing capability when connected as shown in Figure 20. The logarithmic digital attenuator circuit combines the companding DAC's multiplying capabilities with the multiplexing function which is accomplished by using the SB and E/$\overline{D}$ inputs as channel select inputs. The analog signal, V_{IN}, applied at the $V_{R(-)}$ reference input can be attenuated by approximately 0.3dB per step and 6dB per chord, throughout most of the output dynamic range. The SB and E/$\overline{D}$ inputs provide signal switching combinations which will multiplex the attenuated analog signal into four different analog channels.



a. ±10V Range Encode/Decode Connections.



b. Compliance Extension Using AC Coupled Output.

Fig. 18. Some Output Voltage Expansion Schemes.

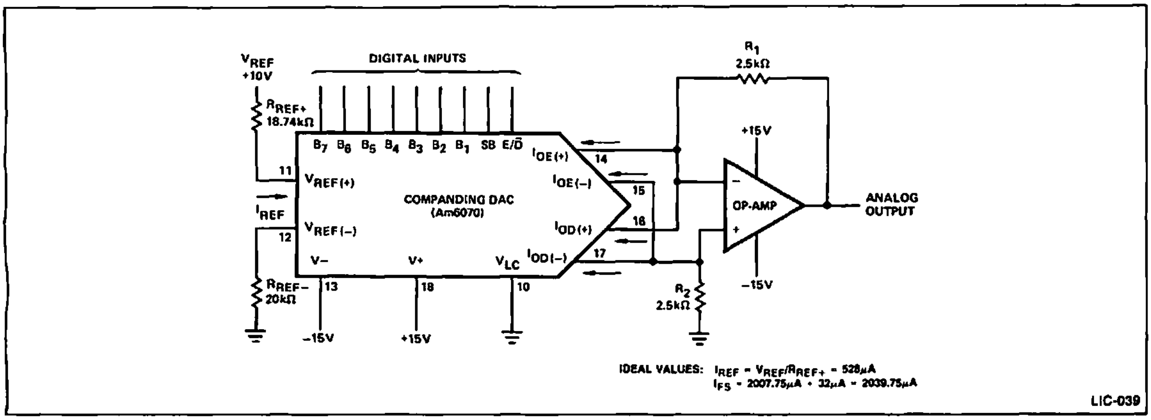


Fig. 19. Output Dynamic Range Expander.

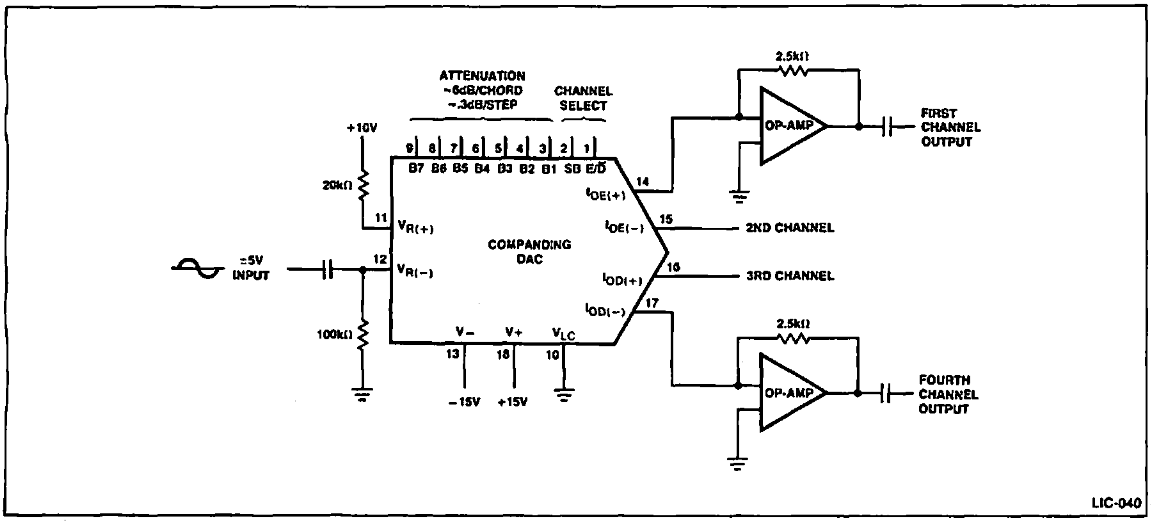


Fig. 20. Logarithmic Digital Attenuator.

For applications where the output dynamic range is to be smaller than 78dB, the circuit connection shown in Figure 21 can be used. With given V_{REF} and V_{IN} values, there are three resistor values, R_{REF}, R1, and R2, which need to be determined. The starting assumption is that a maximum gain of unity from V_{IN} to V_{OUT}, (0dB), is achieved with all digital inputs set to logic 1. The digital inputs all set to logic 0 will determine the minimum gain of the circuit and consequently the desired output dynamic range. Considering the currents flowing through resistors R1, R2, and R_{REF}, and the DAC's output with digital inputs at all 1's, the following relationships can be established:

$$I_{R1} = V'_{OUT}/R1 = I_{OUT} + I_{R2};\ I_{OUT} \approx 3.8\ I_{REF};\ I_{R2} = V_{IN}/R2;$$
$$I_{REF} = (V_{REF} - V_{IN})/R_{REF} \qquad (1)$$

The relationship between output voltages V'_{OUT} and V_{OUT} and input voltages, V_{REF} and V_{IN}, can be expressed as follows:

$$V'_{OUT} = 3.8\,(R1/R_{REF})\,V_{REF} - \left[3.8(R1/R_{REF}) + R1/R2\right] \cdot V_{IN} \qquad (2)$$

$$V_{OUT} = -\left[3.8\ (R1/R_{REF}) + R1/R2\right] \cdot V_{IN}$$

In order to have unity gain, $V_{OUT}/V_{IN} = 1$, the coefficient for V_{IN} in the equations (2) must also be 1:

$$-\left[3.8\ (R1/R_{REF}) + R1/R2\right] = 1 \qquad (3)$$

Two additional conditions for calculating R_{REF}, R1 and R2 values are the minimum gain value G_{min}, and the requirements for the minimum and maximum I_{REF} values, 0.1mA and 1mA, respectively:

$$G_{min,dB} = 20 \log\left[V_{OUT}/V_{IN}\right] = -20 \log (R2/R1), \qquad (4)$$

and $0.1\text{mA} \leq (V_{REF} - V_{IN})/R_{REF} \leq 1\text{mA}$ (5)

The op-amp output in Figure 21 has a DC component that will be attenuated as well as the AC input signal. The output coupling capacitor is used to remove the DC level. However, during switching, the change in DC level will cause a step transient or "click" at the output.

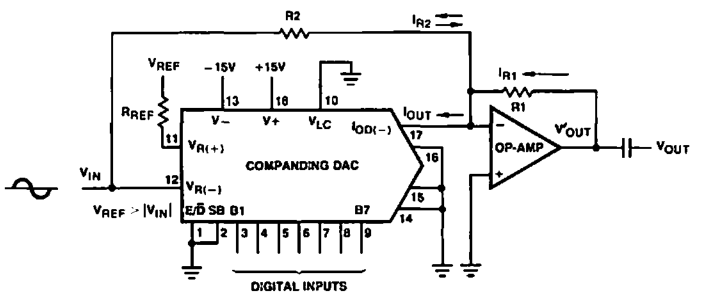


Fig. 21. AC Coupled Digital Attenuator, Adjustable Range.

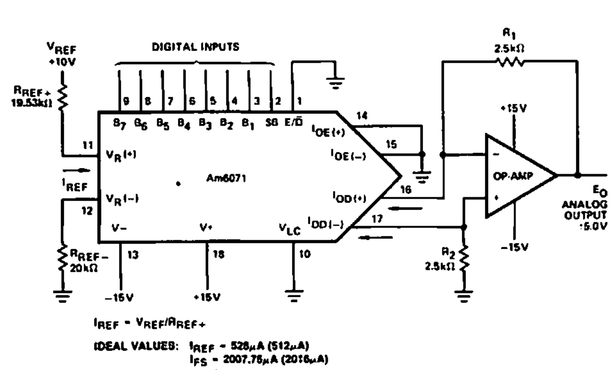
Operating Modes

The Companding DAC has two basic operating modes, decode and encode, which are controlled by the Encode/Decode, E/D̄, input signal. A logic 0 applied to the E/D̄ input places the Companding DAC in the decode mode, and current will flow into the $I_{OD(+)}$ or $I_{OD(-)}$ output, depending on the state of the sign bit, SB, input. A logic 1 at the E/D̄ input places the Companding DAC in the encode mode, which differs from the decode mode by a half step offset current in each chord, and current flows into one of the I_{OE} outputs.

The basic decoder connection for the Companding DAC is shown in Figure 22. The E/D̄ input is grounded, which keeps the Companding DAC in the decode mode. The eight digital data inputs generate an output decode current which is converted by an operational amplifier to a bipolar voltage, E_O. Several discrete E_O values are tabulated in Figure 22 for both μ-law and A-law versions of Companding DACs. The values indicated in parenthesis correspond to the A-law Companding DAC.

The Companding DAC can be used together with a Successive Approximation Register, SAR, a comparator, and additional SSI logic elements to perform the encoding or compression of an analog signal. The circuit, Figure 23, represents an Analog-to-Digital data conversion system. The first task of this system is to determine the polarity of the incoming analog signal and to generate a corresponding SB input. When the proper $\overline{\text{START}}$, $\overline{\text{S}}$, and $\overline{\text{CONVERSION COMPLETE}}$, $\overline{\text{CC}}$, signal levels are set, the first clock pulse sets the MSB output of the SAR, Am2502, to a logic 0 and sets all other parallel digital outputs to logic 1 levels. At the same time, the flip-flop is triggered, and its output provides the E/D̄ input with a logic 0 level. No current flows into the I_{OE} outputs. This disconnects the converter from the comparator inputs, and the incoming analog signal can be compared with ground which is applied to the opposite comparator input. The resulting comparator output is fed to the Am2502 serial data input, D, through an exclusive-or gate. At the same time, the other input to the exclusive-or gate is held at a logic 0 level by the logic shown in Figure 23. This exclusive-or gate inverts the comparator's outputs whenever a negative signal polarity is detected. This maintains the proper output current coding, i.e., all ones for full scale and all zeros for zero scale.

The second clock pulse changes the E/D̄ input back to a logic 1 level because the $\overline{\text{CC}}$ signal changes. It also clocks the D input signal of the Am2502 to its MSB output, and transfers it to the SB input of the Companding DAC. Depending upon the SB input level, the Companding DAC's output current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output.



	E/D̄	SB	B_1	B_2	B_3	B_4	B_5	B_6	B_7	E_O
POSITIVE FULL SCALE	0	1	1	1	1	1	1	1	1	5.040V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.004V
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0.0012V
(−) ZERO SCALE	0	0	0	0	0	0	0	0	0	−0.0012V
(−) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	−0.004V
NEGATIVE FULL SCALE	0	0	1	1	1	1	1	1	1	−6.040V

LIC-042

Fig. 22. Detailed Companding DAC Decoder Connection.

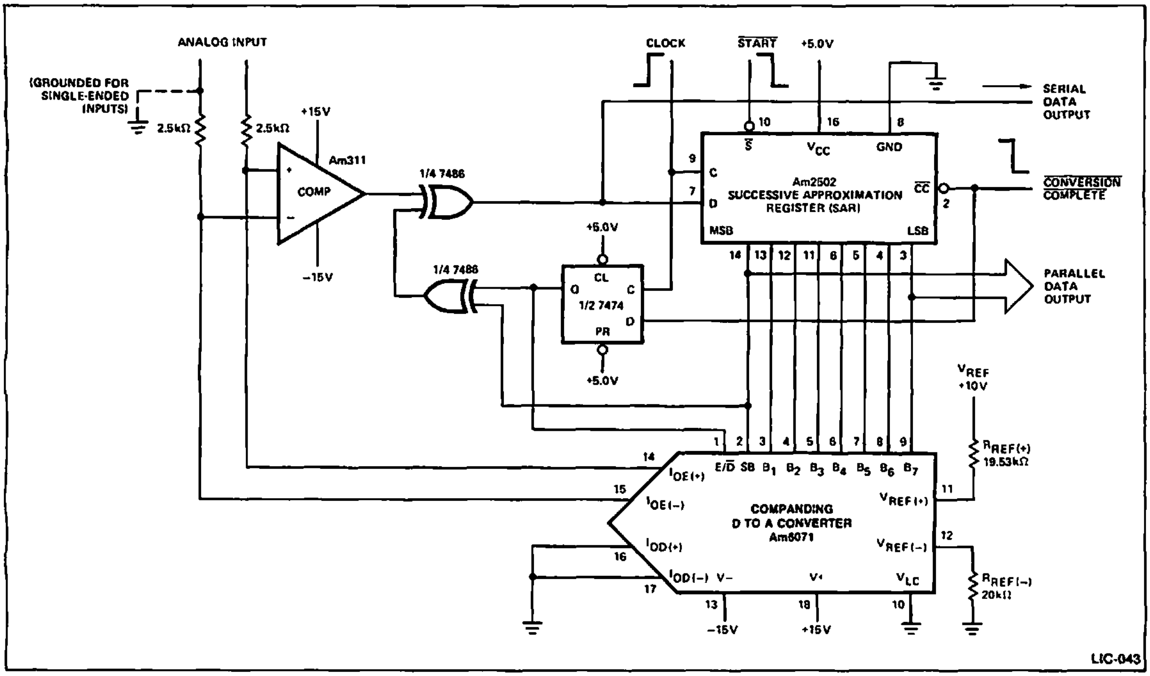


Fig. 23. Detailed Companding DAC Encode Connection.

Nine clock pulses are required to obtain a digital, non-complemented, binary representation of the incoming analog signal at the eight Am2502 digital outputs. The resulting analog output signal is compared with the analog input signal after each of the nine successive clock pulses. The analog input signal should not be allowed to change its value during the data conversion time. In high speed systems, fast changes of the input analog signals are usually prevented by using sample and hold circuitry.

When the Companding DAC is used in a feedback loop with a SAR, the data input transitions in the successive approximation search technique exhibit a maximum change of two adjacent bits, and the starting pattern is 0111 1111. The next successive pattern after the first iteration, will be either 00111111 or 10111111. The worst case settling times are experienced during step bit changes in chord 0, where the output current must settle to $\pm 0.25\mu A$. The worst case settling time is about 600ns for code changes in the upper end of chord zero and 1800ns for code changes near zero. The system clock must take into account the settling time of the DAC, the switching speed of the comparator and the time delays in the SAR. In general, the DAC is the slowest component, (comparator Am311's delay is about 200ns and SAR delays are about 46ns), and will determine the clock rate. For optimum accuracy the clock rate should accommodate the 1800ns settling time near zero scale current. However, faster clock rates (1100ns-1800ns) can be used with some degradation in accuracy for signals near zero.

Microprocessor Based Data Acquisition Systems Applications

High output resolution with guaranteed monotonicity over its entire dynamic range and digitally controllable inputs makes the Companding DAC very attractive for application in data acquisition and control systems. The encoding capability, in particular, provides an acquisition system with considerable flexibility, limited only by the rate of change of the acquired analog input signals.

A typical data acquisition system using the Companding DAC is shown in Figure 24. The A to D data conversion procedure is controlled by the 9080A Microprocessor set, (Am9080A 8-bit Microprocessor, Am8224 Clock Generator and Driver, and Am8238 System Controller and Bus Driver). The START one-shot circuit, Am26S02 will be activated by the START A/D command, ($\overline{CS} = 0$, $\overline{IOW} = 0$), which will initiate the A to D procedure by setting the $\overline{S}$ input of the SAR circuit, Am2502, to a logic 0. The width of the one-shot pulse must be greater than the period of the DATA CLOCK signal to initialize the SAR logic. The duration of DATA CLOCK period must accommodate the worst settling time of the DAC and comparator Am311, to ensure valid data at the SAR input. The one-shot circuit may be eliminated, provided that the expected worst case settling time does not exceed $1\mu s$ and the SYSTEM CLOCK, $\phi 1$, does not exceed 2MHz. The first data clock after $\overline{S}$ goes low sets the $\overline{CC}$ output high, which in turn switches the input sample and hold circuit, (LF198), into the hold mode and puts the microprocessor into a wait state. After eight subsequent DATA CLOCK periods, ($8 \times 2\mu s$), the conversion complete signal, $\overline{CC}$, changes from logic 1 to logic 0, which puts the S & H circuit into the sample mode and allows the microprocessor to resume its functions by removing the logic 0 from the RDYIN input of the Am8224 chip. With a logic 1 at the SAR's $\overline{S}$ input, the DATA CLOCK cannot change the SAR's digital data outputs after completion of conversion. Thus, these outputs will be stable and available for subsequent interrogation. The microcomputer will issue a READ A/D command, ($\overline{CS} = 0$, $\overline{IOR} = 0$), which enables the three-state data buffer, Am25LS241, and transfers the data outputs of the SAR to the system data bus and into the micro-

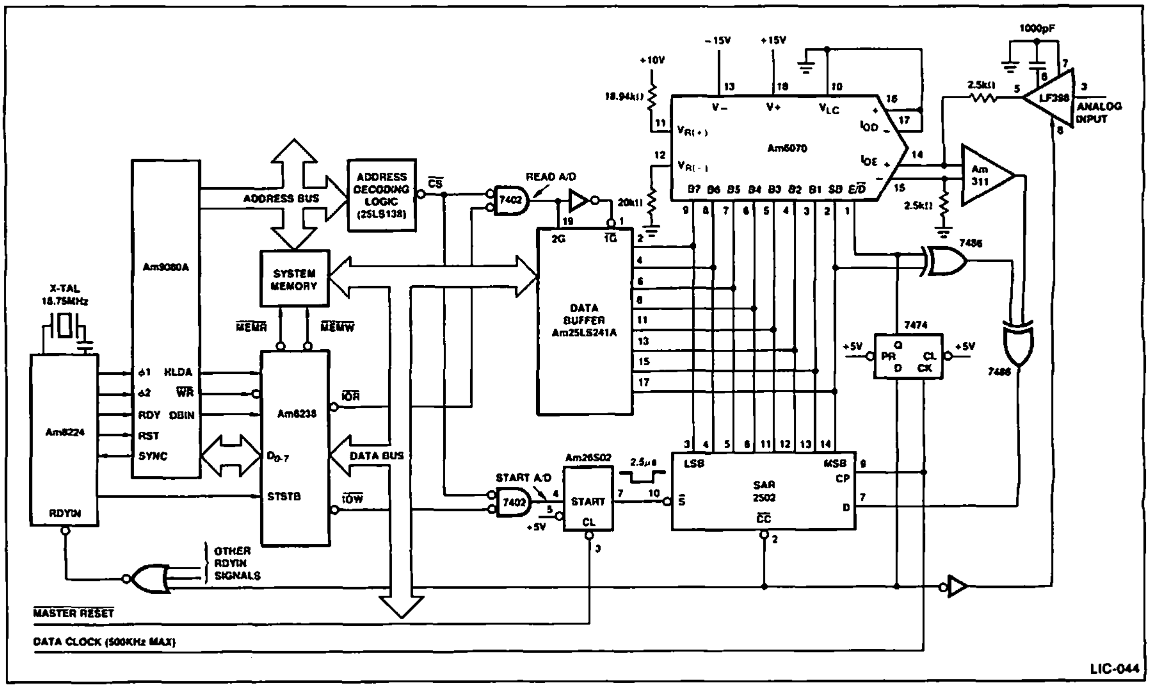


Fig. 24. Microprocessor Controlled Data Acquisition System.

processor's accumulator. A subsequent memory write command, then stores this data in the desired memory location. For the next A to D data conversion, the microprocessor must generate another START A/D signal. An A to D data acquisition can be achieved using only three 9080A instructions.

OUT (to ADC device) –generation of START A/D command
IN (from ADC device) –generation of READ A/D command
STA (to MEMORY) –store digital representation of the acquired analog signal into memory

If the required nine DATA CLOCK periods present a prohibitively long wait state for the processor, the A to D procedure can be more efficiently handled using a suitable interrupt scheme. The logic shown in Figure 25 illustrates the A to D and D to A conversion using three interrupts. The external interrupt signal, $\overline{\text{VALID RECEIVE DATA}}$, which initializes the A to D conversion, is received and processed by the Am9519 Universal Interrupt Controller. It's output, GINT, is recognized by the 9080A Microprocessor logic and generates the $\overline{\text{INTA}}$ signal at the output of the Am8238. The $\overline{\text{VALID RECEIVE DATA}}$ signal will cause the receive S & H circuit to switch into the hold mode after 5μs, via Am26S02 and associated flip-flop circuitry. This delay is needed to satisfy the sample time requirements for the (Am)LF398 S & H circuit, with C_h = 1000pF. This one-shot circuit may be eliminated if the analog input data is maintained unchanged for about 25μs after recognition of the $\overline{\text{VALID RECEIVE DATA}}$ signal. Upon receipt of an $\overline{\text{INTA}}$ signal, the Am9519 provides the address of an appropriate subroutine to the CPU. This subroutine will initiate the A to D conversion by generating the START A/D command. After A to D conversion is complete, the $\overline{\text{DATA READY}}$ signal, identical to the $\overline{\text{CC}}$ signal, generates an interrupt for the 9080A microprocessor to read and store the results of the A to D data conversion via an octal, non-inverting, three-state driver, the Am25LS241A. The $\overline{\text{CC}}$ signal at the same time will switch the receiving S & H circuitry into the sample mode. Two sequences of 9080A instructions which perform the acquisition operations described are detailed in Table 10. The corresponding functional flow charts are shown in general form in Figure 26.

The addition of SSI logic shown in Figure 25 generates signals $\overline{\text{CS2}}$ and $\overline{\text{CS3}}$ which transmit an analog signal generated by the DAC from digital information stored in the system memory. An external interrupt request for transmission of the analog signal, $\overline{\text{TRANSMISSION REQUEST}}$, will initiate the D to A conversion subroutine. A corresponding word in memory will be fetched into the 9080A accumulator and then latched into the Am25LS374, Octal D type register, via signals $\overline{\text{CS2}}$ and $\overline{\text{IOW}}$. At the same time, the non-inverting three-state data bus transceivers, Am8T28, will be turned to the direction which corresponds to the D to A conversion procedure. The latch captures valid 9080A accumulator data, which will be used as the digital inputs throughout the D to A conversion procedure. The next instruction in sequence will be a command to start sampling the Companding DAC's decode outputs, ($\overline{\text{CS3}}$ = 0, $\overline{\text{IOW}}$ = 0), which will be already settled. Assuming that one 9080A I/O instruction takes about 5μs at a system clock frequency of 2MHz, the next command in the instruction sequence may generate a signal $\overline{\text{VALID TRANSMISSION DATA}}$, (CS3 = 0, IOR = 0), which will put the transmission S & H circuitry into the hold mode and return the data transceivers, Am8T28, to the direction which corresponds to the A to D conversion procedure. Input data for the Companding DAC is supplied by the SAR circuitry. A sequence of 9080A instructions which could handle the D to A conversion procedure and analog signal transmission through the programming I/O interrupt scheme shown, is presented in Table 10. The corresponding functional flow chart is shown in Figure 26.

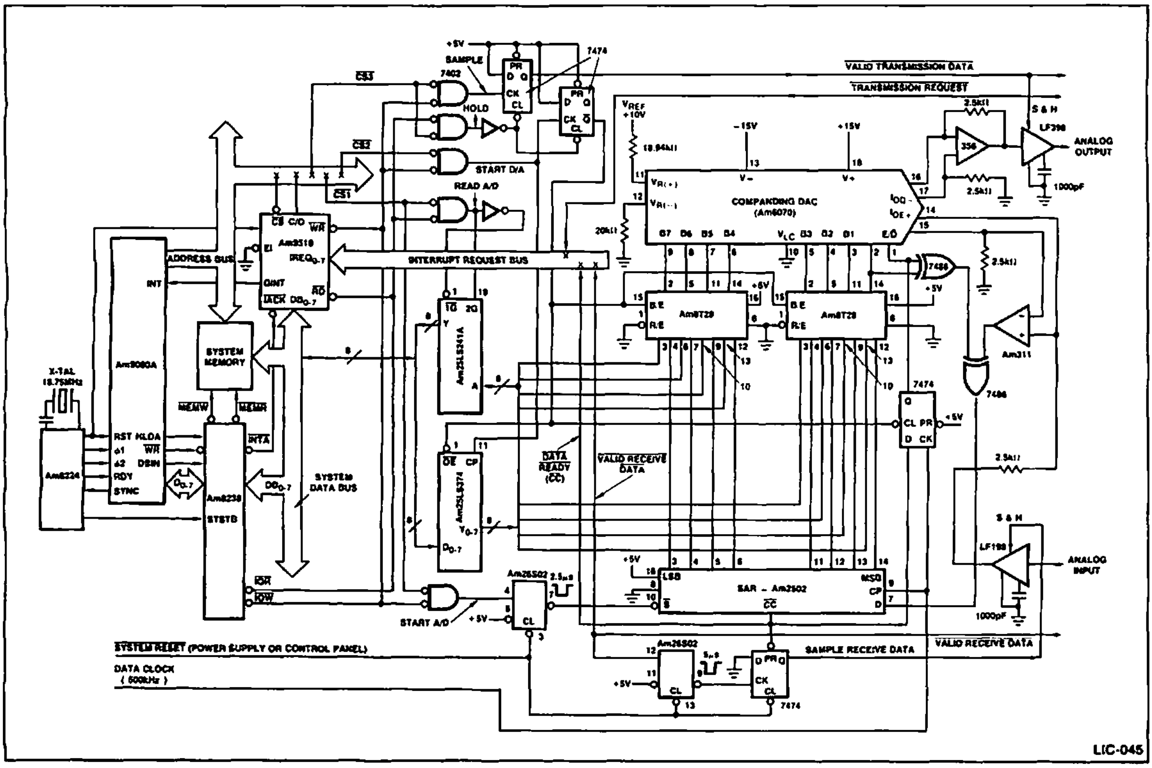


Fig. 25. Microprocessor Controlled Single Channel Transceiver Converter System.

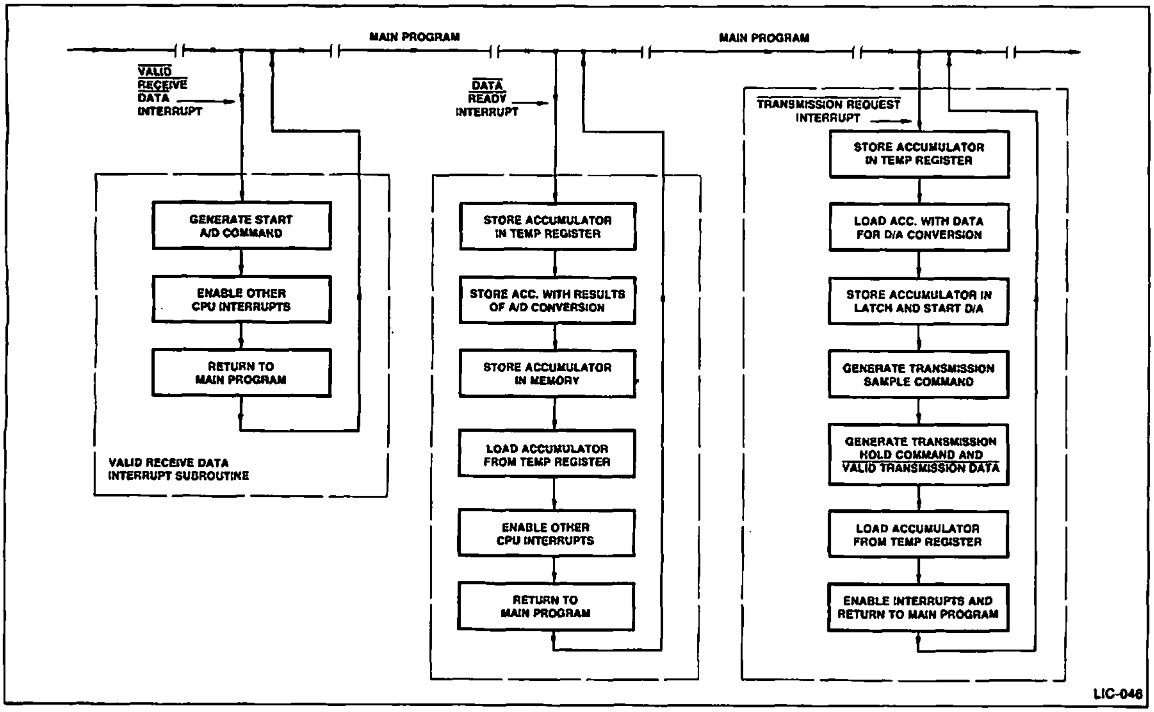


Fig. 26. Functional Interrupt Subroutine Flow Charts for Data Transceiving Converter.

TABLE 10
INTERRUPT SUBROUTINES FOR SINGLE CHANNEL DATA TRANSCEIVING CONVERTER SYSTEM IMPLEMENTED WITH 9080A INSTRUCTIONS

VALID RECEIVE DATA Interrupt Subroutine:

OUT (to ADC)	– Generate START A/D command.
EI	– Enable other CPU interrupts.
RET	– Return to main program.

DATA READY Interrupt Subroutine:

STA (to TEMP)	– Save accumulator content.
IN (from ADC)	– Read digital results from SAR outputs into accumulator.
STA (to Memory)	– Store accumulator's content into memory.
LDA (from TEMP)	– Restore accumulator's content before subroutine.
EI	– Enable other CPU interrupts.
RET	– Return to main program.

TRANSMISSION REQUEST Interrupt Subroutine:

STA (to TEMP)	– Save Accumulator content.
LDA (from DATA)	– Load accumulator with digital data which will be converted to an analog signal.
OUT (to LATCH)	– Output data for D to A conversion to the latch circuit and START D/A conversion.
OUT (to DAC)	– Generate Transmission SAMPLE command for S & H circuitry, $\overline{CS3} = 0$, $\overline{IOW} = 0$.
IN (from DAC)	– Generate Transmission HOLD command for S & H circuitry, and $\overline{\text{VALID TRANSMISSION DATA}}$ signal.
LDA (from TEMP)	– Restore accumulator's content before interrupt subroutine.
EI	– Enable other CPU interrupts.
RET	– Return to main program.

Motion Control Systems Applications

The high resolution and accuracy of the Companding DAC transfer function for small output signal levels provide a very smooth and precise analog control signal to devices whose outputs are voltage or current dependent. However, when major disturbances are detected in the system, the Companding DAC will produce correspondingly larger control analog signals which cause very fast output response of the controlled analog device. Figure 27 shows the Companding DAC used in a feedback loop to provide a small analog error signal to control the speed and direction of a voltage controlled motor in order to properly position the shaft. The shaft encoder generates an 8-bit digital word which represents the current shaft position of the motor.

There are 256 discrete positions of the shaft which can be identified at the shaft encoder's output. This output will be sampled and latched using an 8-bit register, Am25LS273. The sampling rate is determined by dividing the time for one shaft revolution at the motor's highest speed by 256. The maximum rate will be limited by propagation delays through the comparator and ALU chips and by the settling time of the Companding DAC. The output of the shaft position sampling register, data "B", is digitally compared with the desired shaft position, data "A". The magnitude of the difference between digital words "A" and "B" is directly porportional to the error of the motor shaft position. The sign of this digital subtraction provides information about the polarity of the analog error signal which drives the motor in the direction necessary to decrease the error. The speed of the motor is proportional to the magnitude of the error $|A-B|$. The sign and magnitude of the error are determined by two comparator chips, (Am9324 Four-Bit Comparator), and two ALU chips, (Am25LS381

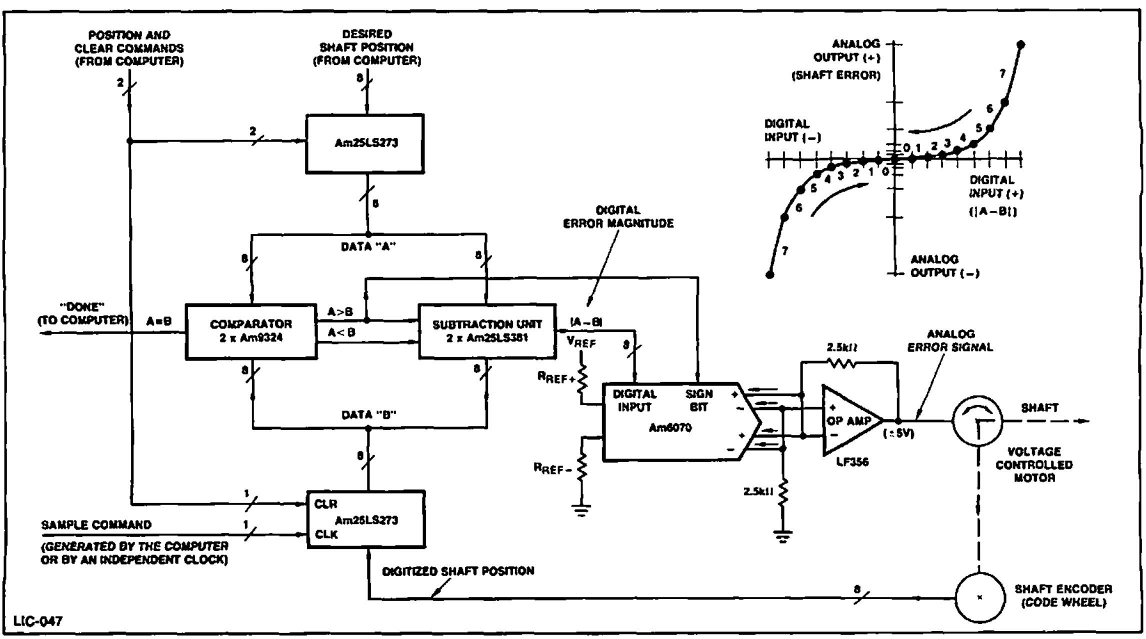


Figure 27. Nonlinear, Computer Controlled, Digital-to-Shaft-Position Conversion System.

Four-Bit Arithmetic Logic Unit). The end of the motor shaft correction procedure is indicated to the computer via the comparator's output "A=B".

The eight digital bits of the error magnitude |A−B| are applied to the seven data inputs of the Am6070 and to the $E/\overline{D}$ input. The Am6070 outputs are connected to provide 32 steps per chord, which totals 256 steps or a 78dB output dynamic range. The smallest and largest step sizes are 0.25μA and 32μA, respectively. The sign bit value is taken from the "A>B" output of the comparator circuit, and determines the polarity of the op-amp, (Am)LF356, output voltage.

The computer function in Figure 27 is mainly confined to initializing the shaft correction procedure by latching the desired shaft position, data "A". Clear commands may be issued during the power-up procedure in order to bring the motor shaft to some initial position. The application of the Companding DAC with its nonlinear transfer characteristic and its nonuniform step sizes which are proportional to the magnitude of the error, |A−B|, significantly reduces system transient response effects such as over-shoots and ringing while minimizing the time required to reach the new shaft position. The system can be programmed to be either critically damped (minimum response time) or under damped (no overshoot).

Figure 28 shows a Companding DAC in a feedback loop which provides small analog error signals for control of the velocity of a voltage controlled motor. This is a paper cutting control system where paper is unwound from a feed roll and cut to size by a mechanical knife. In this application the Companding DAC is in the velocity feedback path and its output is used to generate a velocity profile command signal. The motor rotation is initiated from a front panel by depressing the START button. A COUNT-UP command from a microprocessor sets the binary counter to its count up mode, which drives the Companding DAC inputs. When some predetermined number of counts has been reached, the counter stops and the Companding DAC is held at a constant output value. The incremental encoder produces pulse counts proportional to the distance of paper travel. The desired paper size expressed as a number of incremental encoder pulse counts is stored in a CPU storage register. The outputs of the incremental encoder are constantly accumulated in an internal CPU counter and are compared with the content of the CPU storage register throughout the entire velocity control procedure. When a match is found, the corresponding COUNT DOWN command is issued to the counter, the internal counter is cleared, and a new value is loaded into the internal storage register.

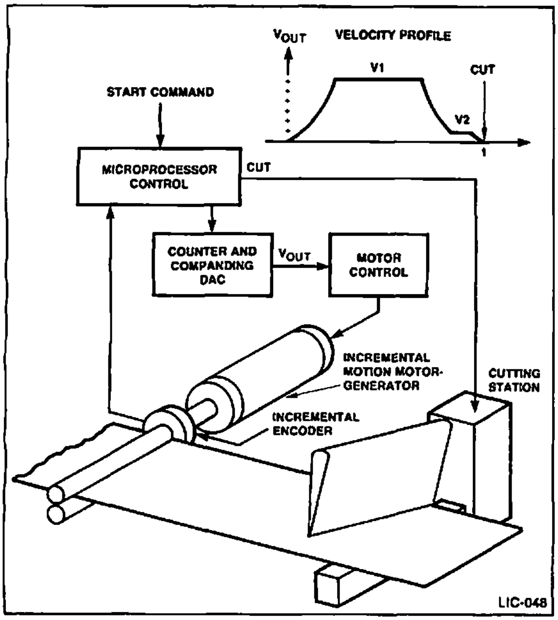


Fig. 28. Paper Cutting Control System.

The values which control the velocity of the motor are stored in a register, external to the CPU, and its content is compared with the outputs of a binary up/down counter during the motor's acceleration and deceleration phases. Whenever a match is achieved, an interrupt signal will be generated and the working mode of the external counter changes. The final stop position is approached in a well controlled manner which stops the paper and cuts it with a minimum of overshoot and error.

Figure 29 shows the necessary logic for generation of the velocity profile control signal. The CPU will first load the external storage register, Am25LS273, via the LOAD signal, to the desired count-up value for the external up/down counter, Am25LS193. Upon recognition of the START request, the CPU issues the COUNT-UP command which enables the 8-bit comparator chip, Am25LS2521. The zero initial digital code at the Companding DAC inputs produces zero voltage at the output, V_{OUT}. Every enabled conversion clock pulse will increase the Companding DAC output current by a corresponding amount, and the V_{OUT} increases in accordance with the Companding DAC transfer characteristic. This portion of the velocity profile control signal corresponds to the motor acceleration phase. When the counter outputs match the content of the external storage register, the interrupt signal $\overline{INT1}$ is generated, and the UP flip-flop is reset.

This stops the up/down counter and the motor continues to rotate with a constant velocity, V1. Duration of the acceleration phase depends on the value initially stored in the external storage register and the frequency of the conversion clock. Upon recognition of the $\overline{INT1}$ signal, the CPU will load a new value into the external storage register, which is used to decelerate the motor from velocity V1 to a lower velocity, V2.

During the constant velocity phase, V1, the encoder pulses accumulate in the CPU counter until the value "m", stored in the CPU internal storage register, is reached. At this time the CPU will issue a COUNT DOWN command and reload the internal storage register with the value "n". The sum of these two values, m+n, should represent the length of the paper expressed in encoder pulses. This value is "p" pulses shorter than the desired ideal paper length.

The COUNT DOWN command initiates the count-down mode of the external up/down counter, PHASE I, and enables the comparator. When the counter outputs match the value stored in the external storage register, the interrupt signal $\overline{INT2}$ is generated and counting stops. The motor continues to rotate with some constant velocity, V2, which is significantly smaller than velocity V1. This velocity, V2, is a function of the conversion clock frequency and the motor's mechanical parameters such as inertia, weight, etc. The mechanical parameters may cause synchronization difficulties between the second deceleration phase of the voltage waveform at V_{OUT} and the actual velocity of the motor. The velocity V2 is much smaller than V1 and allows a smooth, well controlled stop of the motor at the end of the PHASE II of count-down mode, and thus ensures the smallest possible overshoot and error.

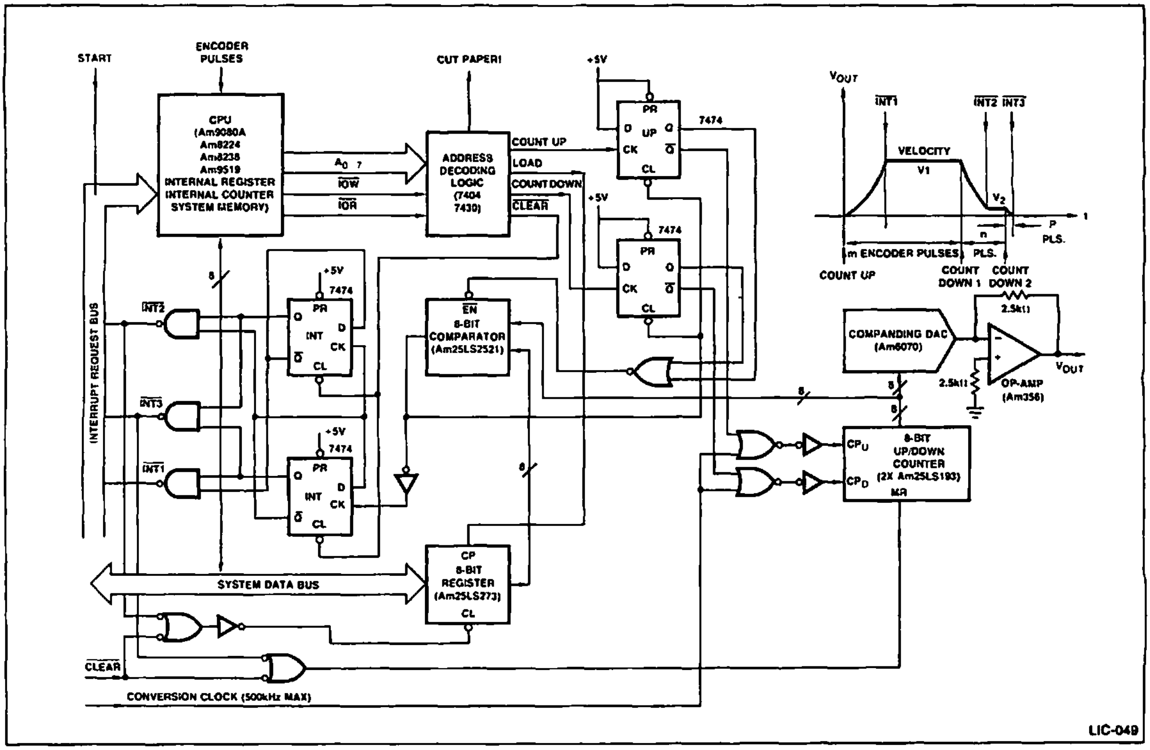


Fig. 29. Microprocessor Controlled Generation of Motor Velocity Control Signal.

The INT2 signal automatically clears the external storage register to all zeros and informs the CPU that the deceleration PHASE I is complete. The CPU continues, internally, to accumulate the encoder pulses until their number becomes "n". At this time the CPU issues a new COUNT DOWN command to initiate PHASE II of the count-down mode, and reloads the internal storage register with a final number "p". This number, when summed with the previous two numbers "m" and "n", determines the final length of paper, m+n+p, and is accumulated in the internal CPU counter during PHASE II of counter's count-down mode. At the end of this phase, the $\overline{\text{INT3}}$ signal is generated and counting stops. The number of encoder pulses in the internal counter will be compared with the number "p" stored in the internal storage register. If a satisfactory match is found, the CPU issues a CUT command to the paper cutting station and the paper is cut to the desired size. Finally, the CPU issues the CLEAR command to initialize the INT flip-flops and clear the internal counter. It also reloads both internal and external storage registers with appropriate values, so that a new velocity profile control signal can be generated. Much of the logic shown could be implemented in software, but this would require that much of the microprocessor resources be dedicated to this speed control function.

Audio System Applications

Audio system equipment applications require signal converters which can process bipolar analog audio signals within a ±10V range. A DAC, in an audio system, provides digital gain and/or attenuation of input audio signals. This requires a multiplying DAC, i.e., it must accept an audio signal either in single ended or differential form, and process it as a function of the digital control inputs. Ideally, an audio level control device provides an equal change, in dB, of relative signal level between any two adjacent digital codes or steps throughout its entire output dynamic range. However, differences between steps which exceed 1dB can be annoying to the human ear. For high quality audio systems, the DAC must have low signal distortion, (on the order 0.05% or less over most of the dynamic range), large working dynamic range, (80dB or more), wide bandwidth, large signal to noise ratio, S/N, (80dB or more), and transient-free output gain-change operation which is independent of digital input states.

The Companding DAC with its multiplying feature and its ability to extend its dynamic range up to 78dB, satisfies or exceeds most of these requirements. It handles audio input signals up to ±10V, and its output signal distortion is 0.02% or less over most of the audio signal range. Its nominal level/step resolution is 0.15dB, and its S/N ratio is 80dB or better when referred to a 1V output. However, its total useful audio dynamic range, with a maximum 1dB difference between two adjacent steps, is only 59dB, and its output exhibits DC gain step transient effects, due to the required DC bias current.

The Companding DAC's DC output current potential "click" effects must be suppressed for applications in audio systems where there are large changes in the digital input code. Figure 30 shows the connection for the necessary DC output current compensation. The output dynamic range can be adjusted by varying the value of resistor R2. To suppress the DC step transients, the current I_2 compensates for all DC changes in current I_1. The I_3 current reflects only the AC changes in current I_1 and the current through resistor R2 due to changes in the V_{IN} signal. This allows the attenuated V_{IN} signal to be DC coupled through op-amp A2. The maximum gain for the circuit is assumed to be unity, (0dB), when all digital inputs are set

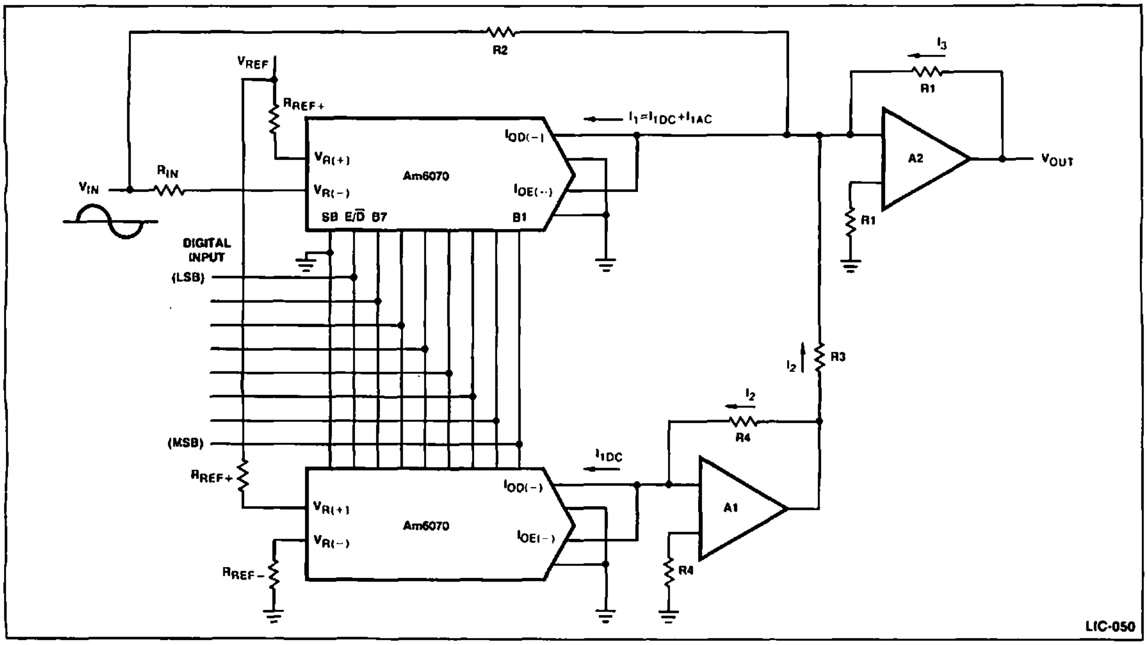


Fig. 30. DC Coupled Digital Attenuator, Adjustable Range.

at logic 1. A determination of the resistor values R_{REF+}, R1 and R2, was discussed in the section on the AC coupled digital attenuator. The R_{REF-} value should be identical to R_{REF+} value and the R3 and R4 values must be equal, so that the current, I_2, will compensate for the DC component of I_1.

The 1dB audio resolution requirement truncates approximately 19dB from the Companding DAC's total dynamic range of 78dB. The level ratio becomes greater than 1dB between the 9th and 8th step of chord 0, (0.25μA/step). If the 1dB resolution criterion is applied to a comparable sign-plus-13 bit linear DAC, the corresponding 1dB requirement also takes off 19dB, and the breakpoint occurs between the 9th and 8th step of the linear 13-bit DAC transfer characteristic. The subtle difference between the 13-bit linear DAC and the sign-plus-8 bit Companding DAC lies in the distribution of the dB ratio values within the steps of the 59dB workable audio dynamic range. For a linearly scaled 13-bit linear DAC, the level ratios in dB among the steps close to the full scale current are very small. The ratios increase as the step numbers decrease toward zero. On the other hand, the sign-plus-8 bit Companding DAC maintains a near constant 0.15dB between steps over the entire dynamic range, with the exception of steps in chord 0.

The 59dB working dynamic range is not wide enough for high quality audio systems which require an 80dB audio control range. To satisfy this requirement, two DACs can be cascaded with their digital inputs driven in parallel. The total dynamic range is now increased to 156dB and the working range, (1dB/step or less), is now approximately 106dB. A cascading scheme for Companding DACs, which also provides for DC transient-free operation, is shown in Figure 31. The advantage of the cascaded Companding DAC's scheme over a similar cascaded linear DAC's scheme is in the number of control bits required to achieve the 106dB range and in the 0.3dB/step uniform attenuation distribution over most of the 106dB range. The audio signal, V_{IN}, is shown in Figure 31 as a single input.

All three Companding DACs in Figure 31 have their SB inputs tied to logic 1. The reference currents for all three DACs should be maintained at positive values throughout the attenuation procedure by proper selection of the input resistor, $R_{IN} = V_{IN}/I_{IN}$, where $I_{IN} < I_{REF}$. In Figure 31, the maximum I_{IN} value is equal to one half of the DC reference current, and the maximum value of V_{IN} is only limited by the output voltage swings of operational amplifiers A2 and A3. The DC transient effects in the cascaded DACs are compensated for by using a Companding DAC followed by the A1 op-amp. The DC compensation circuitry is completely isolated and independent of the AC effects of the applied audio signal V_{IN}, and the only critical requirement is matching R_1 and $R_{REF(+)}$. The step sizes in all chords should be matched for all three Companding DACs. For audio signals with amplitudes not more negative than −5V, (Companding DAC's maximum negative output voltage is −5V), the A1 op-amp can be eliminated, and the positive inputs of the A2 and A3 op-amps can be driven by the DC compensating DAC directly.

Companding DACs, with their logarithmic transfer function, are natural generators for the attack and decay analog signal waveforms used in electronic organs and musical synthesizers. A waveform's attack, sustain, and decay times, together with additional harmonic content information, determine the sounds of a particular musical instrument. For example, woodwinds have very short attack and decay times. The circuit shown in Figure 32 generates trapezoidal-like waveforms with exponential rise and fall times under the control of an 8-bit microprocessor, Am9080A. Digital inputs are supplied by two pairs of 4-bit binary counters, Am25LS191, which are set to the Count Down mode. All of the counters are simultaneously loaded by the LOAD command which is decoded from the microprocessor's

Companding DAC

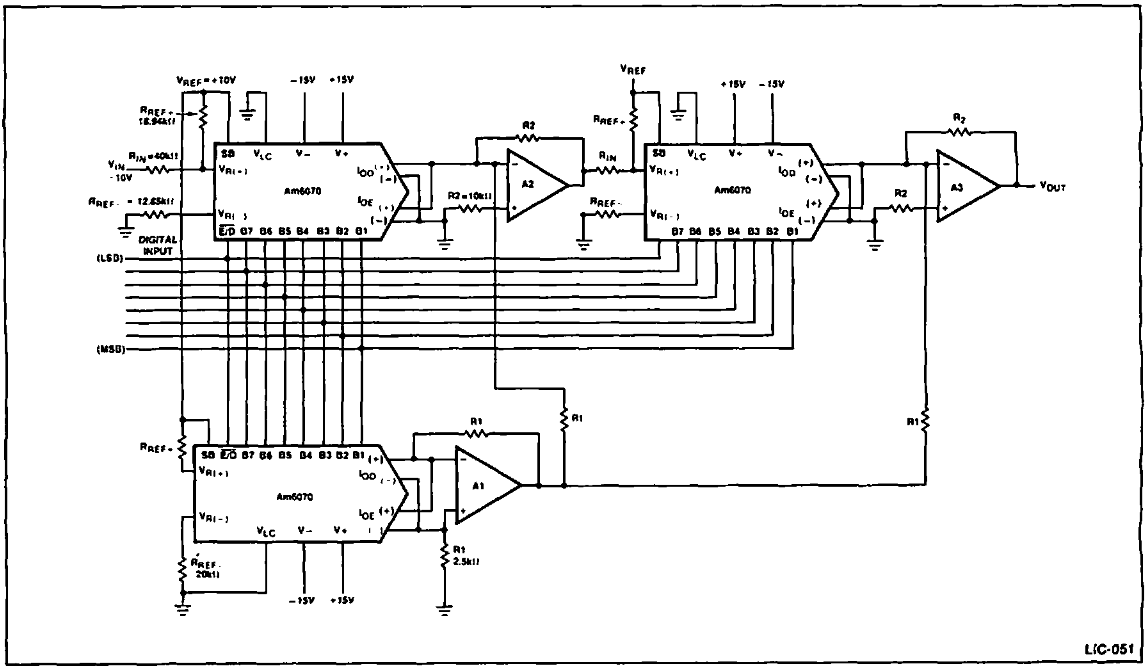


Fig. 31. DC Coupled Cascaded Digital Attenuator.

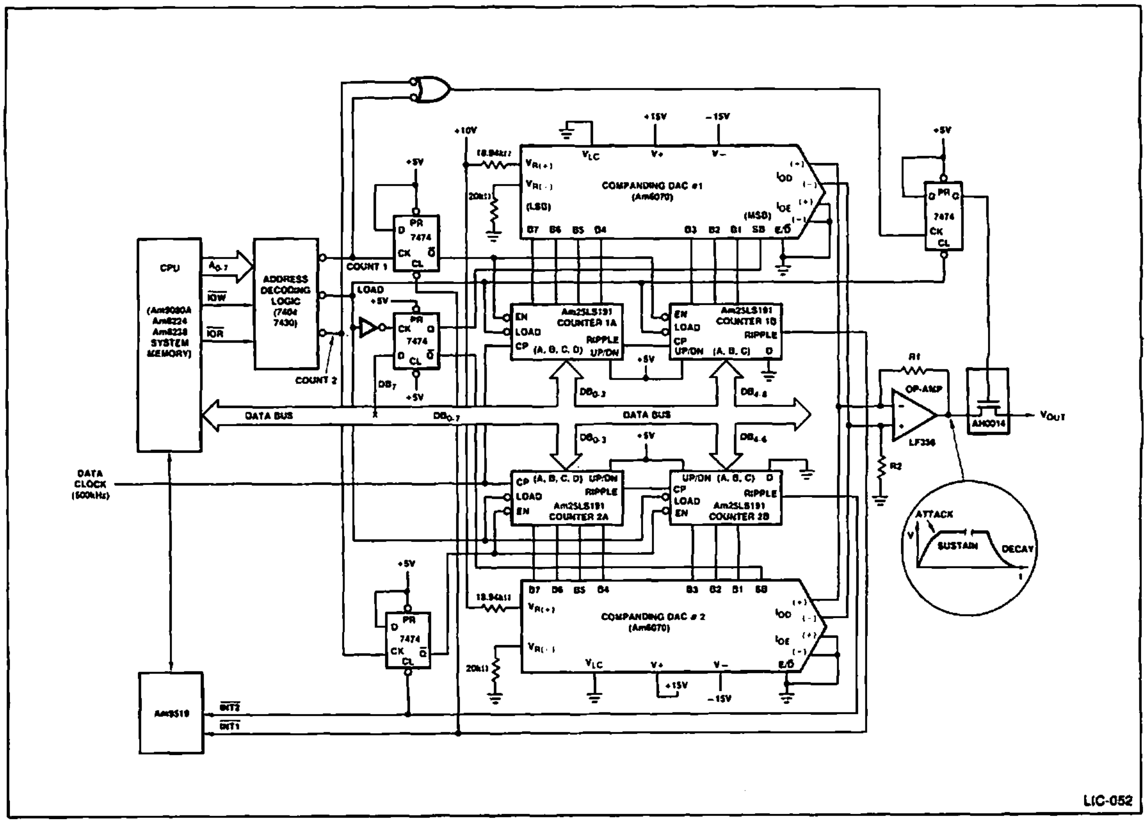


Fig. 32. Microprocessor Controlled Waveform Generator, Attack, Sustain and Decay Signal Waveforms.

address signal combination. Companding DACs 1 and 2 are in the decode mode. The SB inputs are determined by the most significant data bit, DB7, which is stored in the flip-flop during counter loading. The Companding DACs' decode outputs which have the same polarity are tied together and fed into an LF356 operational amplifier. After the settling time required for the Companding DAC's outputs, the currents at the op-amp's inputs should be equal, and its output, V_{OUT}, should be 0V. A command COUNT #1 closes the analog switch, AH0014, and enables counters 1A and 1B via their ENABLE inputs. The 500kHz clock frequency allows sufficient settling time for the Companding DAC's outputs. The initial rise of the op-amp output voltage, V_{OUT}, depends on the number initially stored in the counters, i.e., it depends on the starting point of the Companding DAC transfer characteristic. When Counter #1 reaches zero, the $\overline{\text{INT1}}$ signal indicates underflow, further counting stops, and the microprocessor is informed about the end of Counter #1 operation. After a certain sustain time, which can be preprogrammed, the microprocessor issues the COUNT #2 command and the V_{OUT} waveform starts its decay portion. The time duration of the Attack and Decay slopes generated by the logic in Figure 32 are equal and is specified by the starting count in Counters #1 and #2.

Note that the microprocessor can control the counting functions and the external counter could be replaced with simple, octal data latches. With the increased use of digital techniques and microprocessors for control functions in complex audio systems, microprocessor controlled analog waveforms, similar to those generated by the logic in Figure 32, may become very desirable and attractive tools for the generation of various audio effects. However, it is important to remember that the output from the Companding DAC consists of discrete, non-uniform steps and is not continuous. To obtain a real, continuous signal from the output, some filtering or integration may be required.

Telecommunication System Applications

Digital PCM transmission systems compress analog speech signals into a train of 8 digital bits for each sample. They transmit this information and then decode and expand it back into analog signals. The Companding DAC represents a monolithic solution for most requirements of the PCM *encoding* and decoding procedures. This device replaces a considerable number of discrete and hybrid components in existing PCM transmission schemes. At the same time, the Companding DAC provides increased signal-to-noise ratio in the system, reduces system signal distortions and stimulates further development and wider usage of digital channel switching techniques.

Currently, most transmission systems in the United States follow the Bell D3 communication channel bank specifications, where each channel bank consists of 24 voice channels and the necessary transmission equipment. The entire signal sampling, encoding and multiplexing procedure in the 24 channel bank system must be performed within 125µs. The PCM channel time slot distribution, within a one 125µs time frame, is shown in Figure 33. Each slot contains an 8-bit digital representation of a particular signal sampled from a corresponding voice channel. The total number of bits in the D3 channel bank time frame is calculated as follows: (24 channels x 8 bit/channel)+ 1 signalling bit = 193 bits. The additional single bit is used to identify the beginning of a frame, and data is transmitted at 1.544MHz (193 bits/samples x 8000 samples/sec). In addition, in every sixth frame the

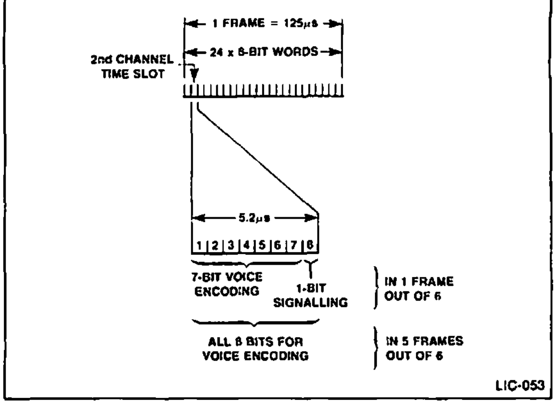


Fig. 33. PCM Channel Timing Frame Format.

least significant bit in each channel slot is used for communication signalling purposes. Consequently, the signal samples in every sixth frame are represented with only 7 digital bits. The increase in signal distortions in this time frame is slight and is not considered significant for PCM voice transmission performance. When the Companding DAC is used as a simple decoder at the receiving side of a system, the connection shown in Figure 19 can be used to minimize distortion caused by the absence of the least significant bit, B7, during these signalling frames. When the signalling frame is recognized, the Companding DAC output is increased by a half step from its corresponding decode output value by switching the $E/\overline{D}$ input from a logic 0 level to a logic 1. However, the European systems, using A-law devices, have 32 channels per bank where the 2 channels are used for signalling information. Each frame requires 256 (32 x 8) bits. The corresponding data transmission rate is 2.048MHz (256 bits/sample x 8000 sample/sec).

In a two-way PCM communication system, a single Companding DAC can perform the time shared encoder and decoder functions known as the CODEC function. The logic state of the $E/\overline{D}$ input determines the operating mode of the Companding DAC and switches the output current to the appropriate outputs. The Companding DAC digital inputs during the encode operation are generated by the successive approximation procedure. In the decode mode, the eight digital inputs are supplied from an external source, either in serial or parallel. The basic diagram for a typical CODEC is shown in Figure 34.

The logic in Figure 34 provides automatic handling of the $E/\overline{D}$ signal levels during the CODEC's XMT mode of operation. The first task of the system is to initialize the SAR circuit by proper manipulation of the $\overline{\text{START}}$ input for the successive approximation procedure. The XMT COMMAND should be synchronized with the low-to-high transition of the $\overline{\text{START}}$ pulse, and its level must be held at logic 1 for the next 8 CLOCK pulses to keep the three-state XMT buffer, 74126, in the low impedance state. During the A to D conversion period, a serial train of 8 digital bits, which represent the sample at the TRANSMIT ANALOG INPUT in Figure 34, appears on the XMT DATA line. XMT and $\overline{\text{RECEIVE}}$ commands are mutually exclusive.

The CODEC in Figure 34 is set to the receive mode of operation by setting the $\overline{\text{RECEIVE}}$ command signal to a logic

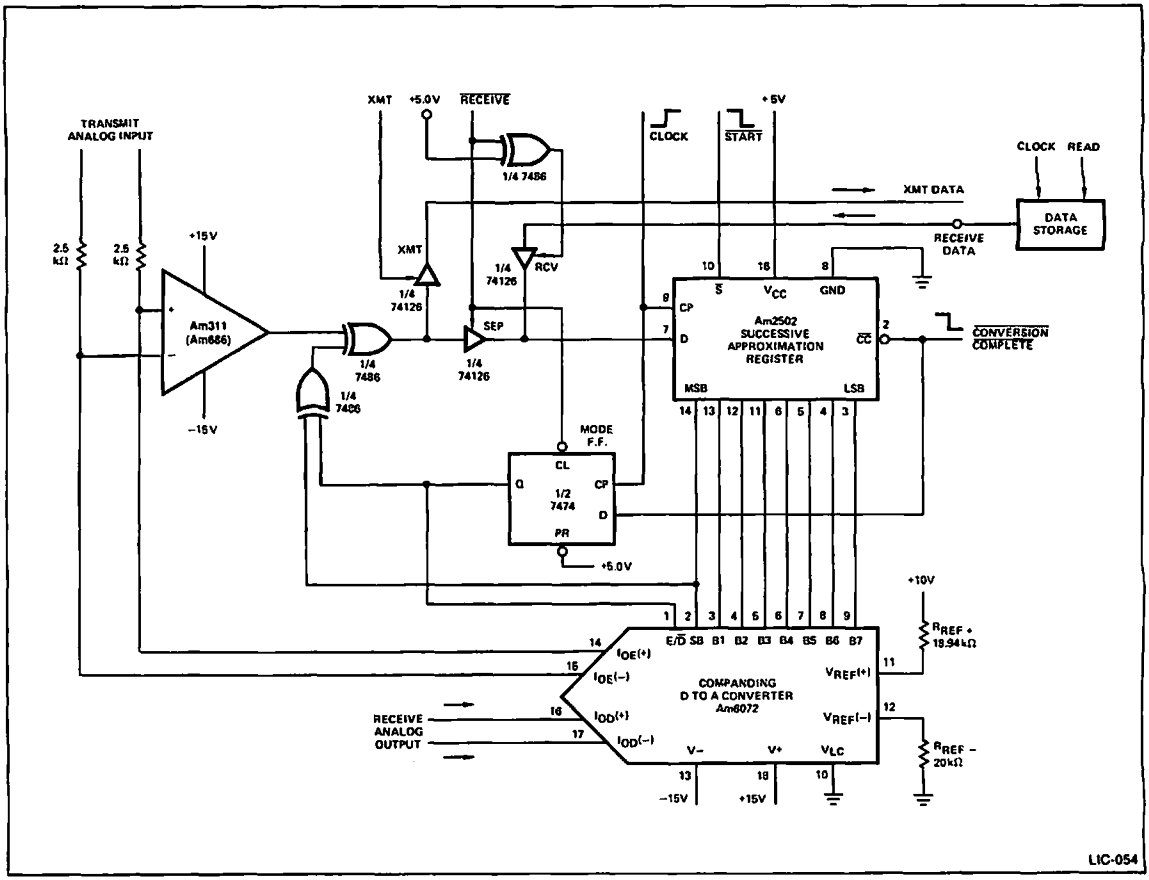


Fig. 34. PCM Encoder/Decoder or Transceiving Converter.

0 level after the $\overline{\text{START}}$ pulse returns to its positive level. A serial data source, DATA STORAGE, supplies a digital train of 8 bits to the serial input D of the SAR circuit via the three-state buffer, RCV, 74126. At the same time, the $\overline{\text{RECEIVE}}$ command signal level keeps the exclusive-or gate output separated from the same SAR's serial D input via another three-state buffer, SEP. The same command also keeps the E/$\overline{\text{D}}$ input of the Companding DAC at logic 0 throughout the entire D to A procedure via the MODE flip-flop in the successive approximation logic. In this CODEC's receive mode, the SAR circuit acts as a serial-to-parallel shift register for the incoming data on the RECEIVE DATA line. After the 8 clock pulses, the outputs of the SAR are ready for the D to A conversion. An analog current representation of the RECEIVE DATA train appears at the RECEIVE ANALOG OUTPUT, after an appropriate settling time. During this time the SAR outputs must remain unchanged and the START signal must remain at logic 1. The $\overline{\text{RECEIVE}}$ command signal must be held at logic 0 for the entire D to A conversion time which includes the Companding DAC's settling time. The CODEC must sample the analog input prior to each A/D conversion. During this sampling period the analog input signal will be changing and the Companding DAC cannot be used to encode this signal. The total encoding time must include the sampling time and the A/D conversion time. If the sampling time period is greater than the time required for the decoding procedure, the Companding DAC can be used as a decoder during this time period and thus, the decoding operation will not require any additional system time.

The CODEC operations in PCM communication systems can be performed on a single channel or on multiple channels in a multiplexed channel switching scheme. The final number of multiplexed channels which can be served by a single Companding DAC with a data sampling rate of 8kHz is limited by the CODEC's sampling and settling times.

Two examples of a single channel PCM CODEC are shown in Figure 35 and 36. The major difference is in the structure of the XMT and RECEIVE data bus. The parallel data I/O CODEC in Figure 35 transmits and receives digital data in parallel form. The parallel data CODEC contains data bus transceivers, (Am)8T26, for handling data in communications systems which might be controlled by one of the popular 8-bit microprocessors. A parallel data I/O CODEC has a considerably shorter D to A conversion time than a serial I/O CODEC.

The circuits shown in Figures 35 and 36 are controlled asynchronously with START, XMT, RECEIVE and their corresponding SAMPLE COMMANDS, which are generated and supplied externally by a communication system. The CLOCK signal is also externally supplied, and in the case of a serial data I/O CODEC, it must be synchronized with the incoming

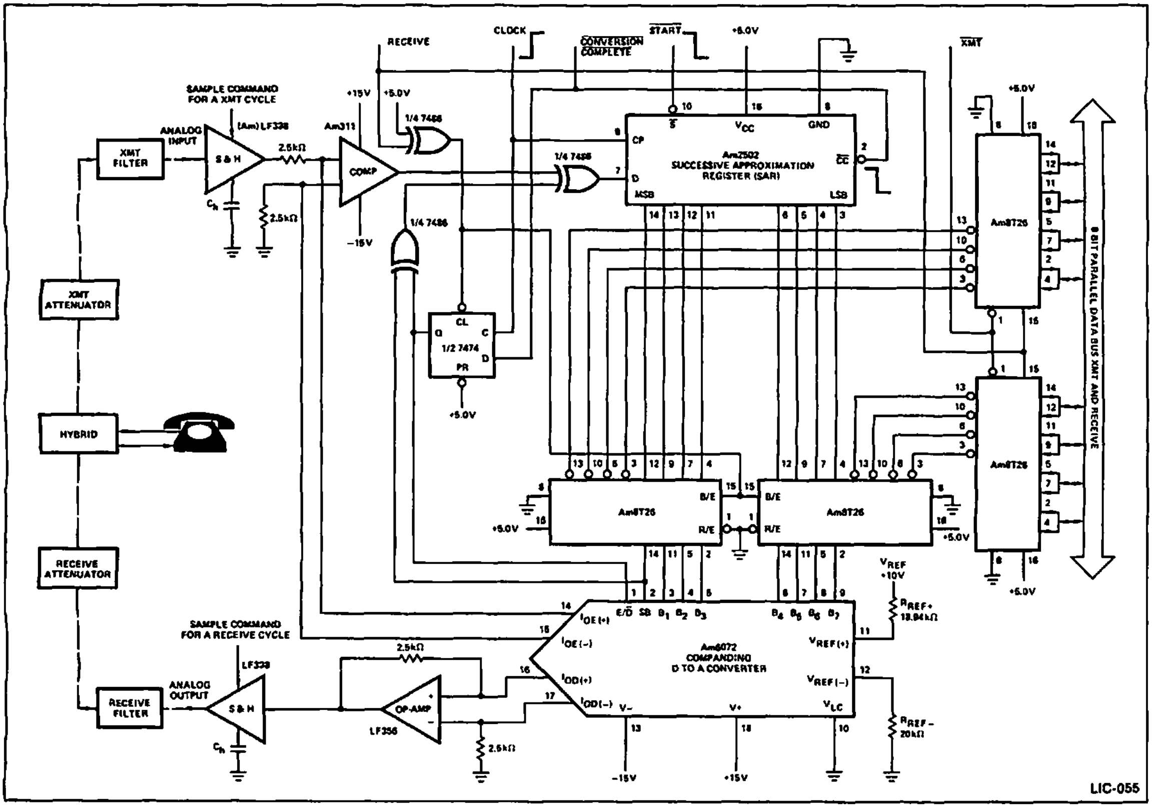


Fig. 35. Single Channel PCM Codec Parallel Data I/O.

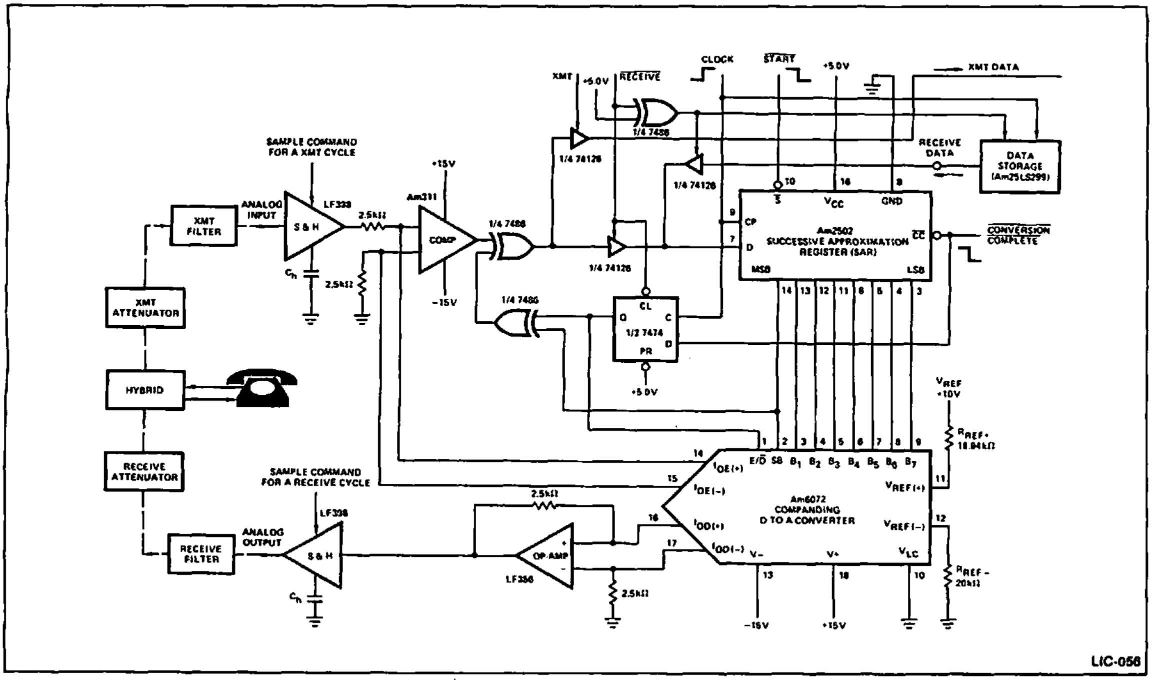


Fig. 36. Single Channel PCM Codec Serial Data I/O.

and outgoing serial data train. The CODEC's only output control signal, $\overline{\text{CONVERSION COMPLETE}}$, $\overline{\text{CC}}$, provides the external communication system with information necessary to generate a XMT signal during the encoding procedure. XMT and RECEIVE commands are mutually exclusive. The transmit and receive data transfers can be performed either alternately or simultaneously. In the latter case the external communication system must employ separate transmit and receive data buses. In addition, storage devices external to the CODEC logic must be provided for the receive data. The code assignment for outgoing or incoming parallel data provides uncomplemented binary values for sign and magnitude. The DAC data bus, as a result, yields "high zeros" density for small output signal amplitudes.

To perform a transmit operation cycle, the START pulse must be held low for one clock cycle. Data conversion for a transmit operation is completed in 9 clock cycles, where the ninth cycle initializes the SAR for the next successive approximation procedure.

The RECEIVE operation in parallel data I/O CODEC is performed without using SAR logic, and the corresponding D to A data conversion does not require a CLOCK signal. Duration of the RECEIVE command signal must accommodate the Companding DAC's settling time, plus the sampling time ($\approx 5\mu s$) required by the S & H circuit, used at the CODEC's analog output. The typical settling time for the worst case input code transition from all ones to all zeros is about $4\mu s$. The receiving data must not change during this time. A XMT command must be issued after a high-to-low transition of the $\overline{\text{CC}}$ signal, and its duration depends on the time required by the external system logic to sample the correct content from the 8-bit parallel data bus. A sample command pulse for a transmit operation can coincide with the START pulse; its duration depends on the sample and hold circuit used at the CODEC's analog input. A sample command pulse for a receive operation must be delayed from a low-to-high transition of the RECEIVE command signal by an amount equal to the Companding DAC's settling time. Its termination can coincide with a high-to-low transition of the RECEIVE command signal.

In the serial CODEC the duration of XMT and RECEIVE command signals must similarly accommodate all signal propagation delays, as well as the settling and sampling times, necessary for conversion of an outgoing or an incoming series of 8 digital bits. During the receive operation, the SAR is acting as a serial-in to parallel-out shift register for data supplied from an external serial source. Shifting data into the SAR requires 9 clock pulses. A sample command pulse for a transmit cycle must be issued before an XMT command signal; its duration depends on the S & H sampling time used at the CODEC analog input. A sample command pulse for a receive cycle must be delayed by a time equal to the Companding DAC's settling time after a high-to-low transition of the $\overline{\text{CC}}$ signal occurs. The data transmission rate at the receive line is limited only by the shifting speed of the SAR which is rated at 15MHz. The data transmission rate at the serial CODEC's data XMT line is limited by the settling time of the Companding DAC and propagation delays through the comparator, exclusive-or, buffer (74126), and SAR devices.

In a one-way PCM communication system the Companding DAC can be used as the decoder at the receiver end of a system or as a part of the encoder at the transmission end of a system. The transmission data bit rate for 24 communication channels sampled at 8kHz is 1.544 megabits/sec. This transmission rate allocates $0.64\mu s$ for each of 193 bits within a $125\mu s$ long 24-channel time frame. A 24-channel PCM decoder which is capable of handling this transmission bit rate is shown in Figure 37. This schematic does not show the logic necessary for recognition of frame and signalling bits. To handle a single bit in $0.64\mu s$ the total signal propagation time through the 8-bit D-type register, Am25LS273, the Companding DAC, Am6072, and the op-amp must not exceed 8 x $0.64\mu s = 5.12\mu s$. This corresponds to the total shifting time of 8 bits through the serial-in, parallel-out, *shift register*, Am25LS164. The most critical propagation delay is caused by Companding DAC's worst case settling time which corresponds to the worst possible input transition of 1111111 to 0000000, which can occur during D to A conversion. If $4\mu s$ are taken for the worst case settling times of the DAC and op-amp, only $1.12\mu s$ are left to be distributed to all other time delays in the system. The 4-bit counter, Am25LS161, and 8-bit shift register, Am25LS164, are synchronized with the system supplied data clock at 1.544MHz. The additional logic in Figure 37 consists of analog switches AH0014 and AM9712, and the corresponding SSI control logic. This switching scheme provides a minimum of crosstalk between output analog channels which may occur due to a possible break-before-make switching problem. The output analog channel hold capacitor values depend a lot on the type of a load at these outputs. The Bell D3 specification specifies system performance down to signal levels of −50dB (00000111 code on the transfer curve). Worst case settling time from full scale to −50dB is about $2.5\mu s$. Decoders in excess of 24 channels, can be built using this settling time but they will have somewhat higher distortion for signal levels below −50dB.

In the PCM encoder schematic shown in Figure 38, the maximum settling time for the Am6072 is assumed to be $1.2\mu s$ for the worst input bit change. The Bell D3 specification can be satisfied using a settling time of $1.2\mu s$, which is the worst case settling time in the successive approximation procedure for signals near −50dB (lowest level on D3 specification). There will be some additional error for very low level signals, but the overall system will meet the D3 specification. The additional logic delay in the feedback path is estimated to be 100ns maximum, and is distributed among the comparator, Am686, the digital 2:1 multiplexer, Am74S258, the exclusive-or circuit, 74LS86, and the SAR, Am2502. This yields $1.3\mu s$ for one successive approximation iteration. Further timing analysis shows that, with no additional delays, 12 channels can be encoded within the $125\mu s$:

$$1.3\mu s \cdot 8 \cdot 12 = 10.4\mu s \cdot 12 = 124.8\mu s$$
$$\text{Clock} = 1/1.3\mu s = 769.23\text{kHz}$$

Two methods are used in the schematics in Figure 38, to prevent additional delays. First, a special switching scheme of analog input signals is employed to sample a channel from one group while a channel from the other group is encoded. This sampling scheme saves the time required for sampling of an analog input and provides a solution for encoding a maximum number of channels for the given "one-bit iteration" time. This design uses analog multiplexers, AM9712, and sample and hold circuits, (Am)LF398. The analog multiplexer at the Companding DAC output, AH0014, switches to another comparator during the time allocated for the first bit iteration, when the sign bit of a sample is established and no current flows through I_{OE} outputs. Secondly, a one shot circuit is used to modulate the positive period of the first data clock pulse, after the SAR's $\overline{\text{CC}}$ signal is generated. The one shot pulse should split the positive portion of this first clock pulse into

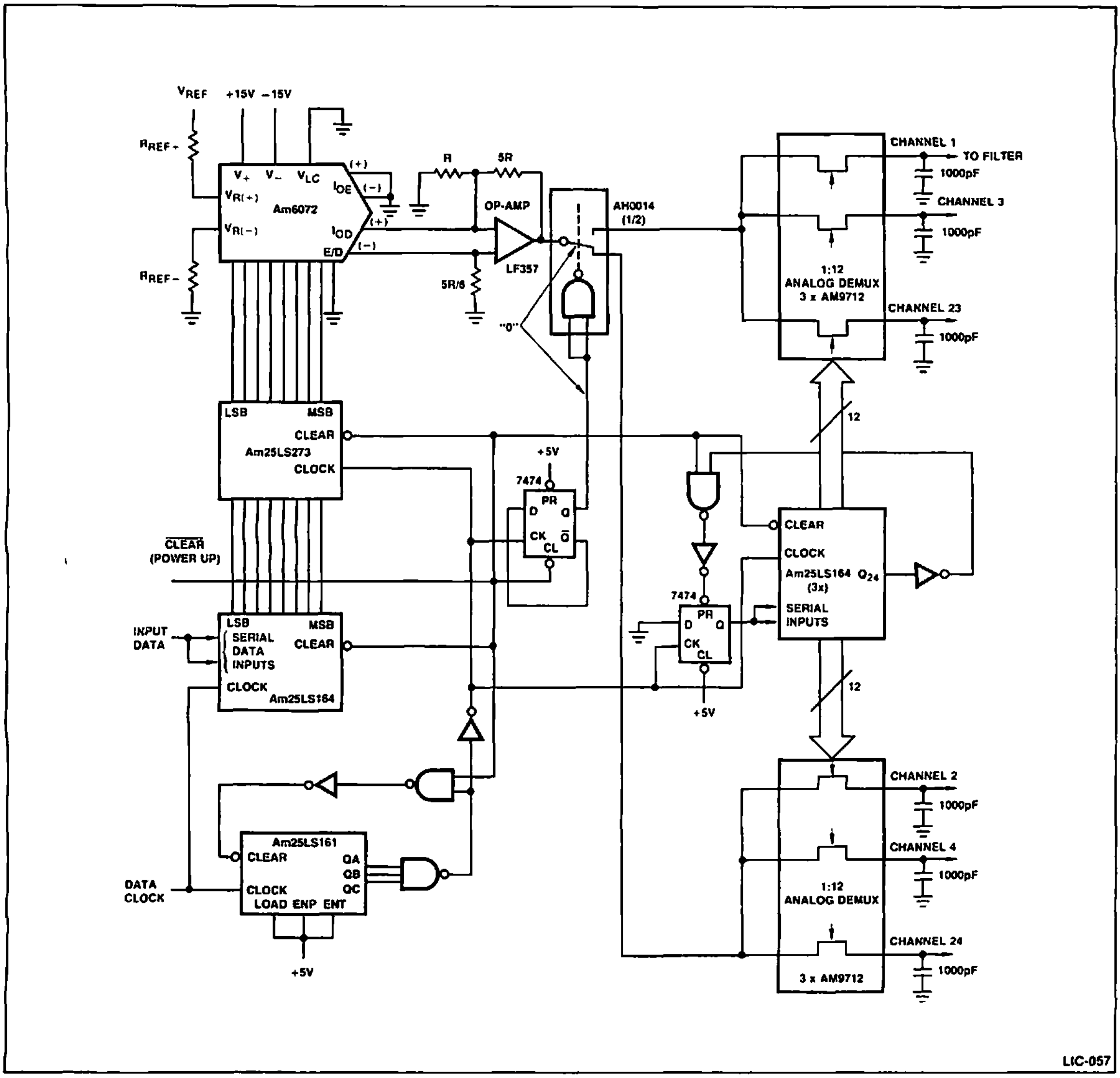
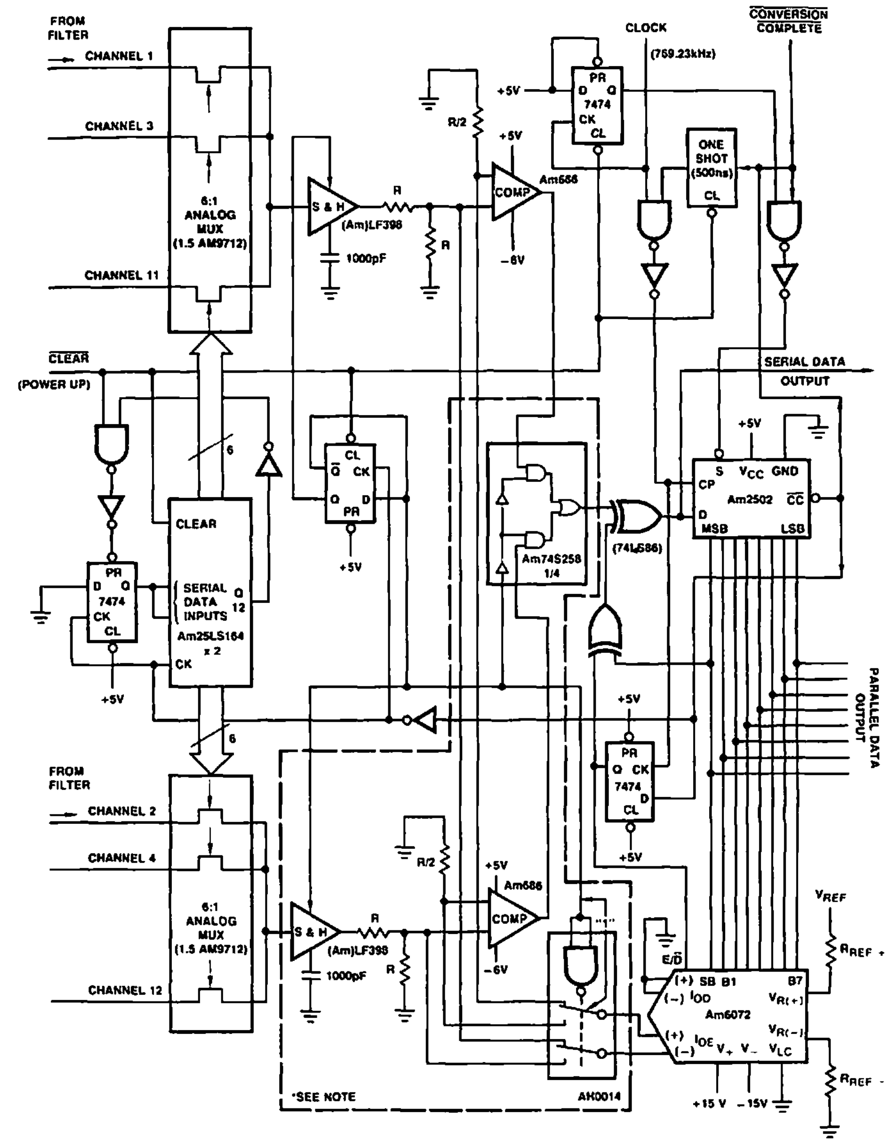


Fig. 37. 24-Channel PCM Decoder.

two positive pulses, and the positive edge of the second pulse will initialize the SAR and eliminate the need for a ninth pulse. The net effect of this pulse modulation is a reduction of the time available to the SAR for the determination of the sign bit value and reduction of the time available for recording the SAR outputs with the correct least significant bit value. However, the time for sign bit evaluation is 1μs, and the LSB value can be taken from the SAR's serial data input D at the time of conversion completion. The encoding logic in Figure 38 is fully synchronized with the system supplied data clock which is input at a frequency of 769.23kHz. A similar encoding scheme provides encoding of 8 channels within the 125μs time without the circuits which are enclosed by dotted lines in Figure 38. Only one S & H circuit and one comparator can be used, and the AH0014 and 74S258 circuits can be eliminated. This D3 system's 8-channel PCM encoder has 15.6μs for an A/D conversion, which allows 5.2μs for the analog multiplexer, (AM9712), and S & H, (LF398), to switch and settle prior to the actual A/D conversion which takes 10.4μs.

One multiplexed CODEC using a single Companding DAC is shown in Figure 39. The CODEC's entire activity is synchronized with a data clock which drives the RECEIVING REGISTER, Am25LS22 (8-bit Serial/Parallel Register), the SAR, Am2502, and the 4-bit binary counter, Am25LS161. Maximum clock frequency is limited by the delays involved in the encoding path and by the data transfer protocol chosen for the XMT and RECEIVE data lines. Using 1.8μs for the Companding DAC's longest settling time and 150ns for all other propagation delays in the encoding path, the minimum time for eight iterations amounts to 8 x 1.95μs = 15.6μs. The corresponding Data Clock frequency is 512.82kHz. A time frame of 125μs contains eight time-slots of 15.6μs each.



•Note: Circuits enclosed by a dotted line may be eliminated in an 8-channel encoder for the D3 communication system which uses 5.2 μs for the input switching and sampling times, (Am9712 and LF398), and 10.4μs for one A/D conversion.

Fig. 38. 12-Channel PCM Encoder.

The CODEC in Figure 39 has four multiplexed channels, and uses the data conversion protocol illustrated in Figure 40. This protocol allocates equal time to the encoding and decoding procedures. Although this is not the most economical timing scheme, it significantly simplifies the CODEC's logic. The value of the most significant bit, MSB, of the 4-bit counter controls the switching between the encode and decode functions, and the switching of the input and output analog channels in the analog multiplexers, AM9712, via 1 of 4 decoder circuit, Am25LS2539, (Dual 1 of 4 decoder). During the negative half of the MSB period, the S & H circuit is placed in the hold mode, the DATA CLOCK and the outputs of BUFFER REGISTER, Am25LS373, (Octal Transparent Latch), are enabled and the Companding DAC is placed in the encode mode. At the same time, the RECEIVING REGISTER, Am25LS22, is receiving data with its outputs in the high impedance state. All analog switches, XMT and RECEIVE, are open during this negative portion of the MSB signal.

During the positive half of the MSB signal period, data clock inputs to the SAR and RECEIVING REGISTER, and START input to the SAR, are kept at logic 0. The S & H circuit is put into the sample mode, the BUFFER REGISTER is put in the high Z state, the RECEIVING REGISTER outputs are enabled, and the Companding DAC is put into the decode mode. During this positive period, the currently addressed XMT and RECEIVE analog switches are closed. The positive going edge of the MSB signal also updates the address code for the analog switches.

Additional timing analysis reveals that by using different and reduced maximum settling times, for the encode and decode portions of the above described data conversion protocol, the number of multiplexed channels can be significantly increased. However, the necessary logic for control and timing of unequal encode and decode data conversion time periods will be more complex than the logic shown in Figure 39. The same encode/decode alternating timing procedure, with 1.1μs allocated for the A/D settling time, and with only 5.6μs allowed for D to A conversion, (not limited by the DAC), will result in eight multiplexed channels. Systems requiring more than eight channels can be built using multi sample and hold circuits to reduce the input sampling time period. The maximum number of channels, limited by the Companding DAC's settling times, can be further increased by adjusting data clock frequency to its optimal values for each of the successive approximation bit-iterations, repeatedly, for every A/D data conversion.

SUMMARY

The Companding DAC was originally developed for the needs and requirements of PCM communication systems. When used to perform a decoder function, at an 8kHz sampling rate, a single Companding DAC can comfortably serve up to 24 voice channels. As a part of the encoding scheme, the Companding DAC can accommodate 12 D3 communication channels. For implementation in CODEC functions, the Companding DAC is ideal for single channel CODEC schemes. The length of the output current's settling time is the most important parameter to be considered for the Companding DAC's implementation in multiple channel CODEC schemes. An 8 channel CODEC is probably an optimum number of channels which can be served by a single Companding DAC.

The timing restrictions are not of such importance in industrial systems. A logarithmic-like, piece-wise transfer function and the very fine resolution and accuracy of a 12-bit linear DAC which are achievable in the Companding DAC's chord 0, provides industrial systems with a very sensitive tool. In addition, the Companding DAC's compatibility with 8-bit microprocessors offers a very powerful control vehicle in the areas of data acquisition and instrumentation systems. A wide dynamic range of 78dB which can be extended by a cascading scheme to 156dB or more, and a high signal-to-distortion ratio of 80dB, allow usage of the Companding DACs for attenuation functions even in a high fidelity audio system. Industrial applications represent a large potential market for Companding DACs and they should be given serious consideration by industrial system designers.

3

REFERENCES

Transmission Systems for Communications, Bell Telephone Labs, Revised Fourth Edition, December 1971.

The International Telegraph and Telephone Consultative Committee, CCITT, Green Book, Volume III – 2, 1973.

American Telephone and Telegraph Company: The D3 Channel Bank Compatibility Specification, Issue 2, 1974.

PCM Update – Parts 1 and 2, GTE Lenkurt, San Carlos, CA, 1975.

A User's Handbook of D/A and A/D Converters, E.R. Hnatek, John Wiley & Sons, 1976.

A Versatile Integrated CODEC for PCM Systems, J.A. Schoeff, 1976 International Zurich Seminar on Digital Communications.

Applicaton Considerations for IC Data Converters Useful in Audio Signal Processing, W.G. Jung, 55th Convention of the Audio Engineering society, 1976, An Audio Engineering Society preprint.

A Monolithic Companding D/A Converter, J.A. Schoeff, 1977 ISSC Conference, Digest of Technical Papers, Philadelphia, PA, USA.

The Am6070, Am6071, Am6072 and Am6073 Data Sheets, Advanced Micro Devices, Sunnyvale, CA, 1977.

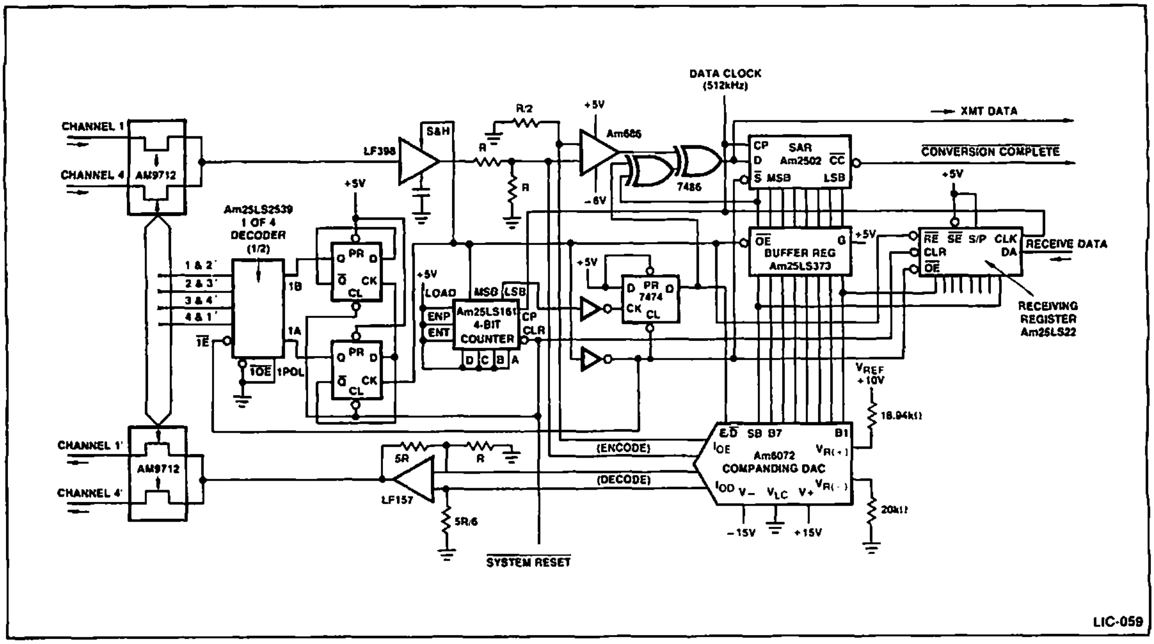


Fig. 39. 4-Channel PCM CODEC with Simultaneous XMT and Receive Data Transfers.

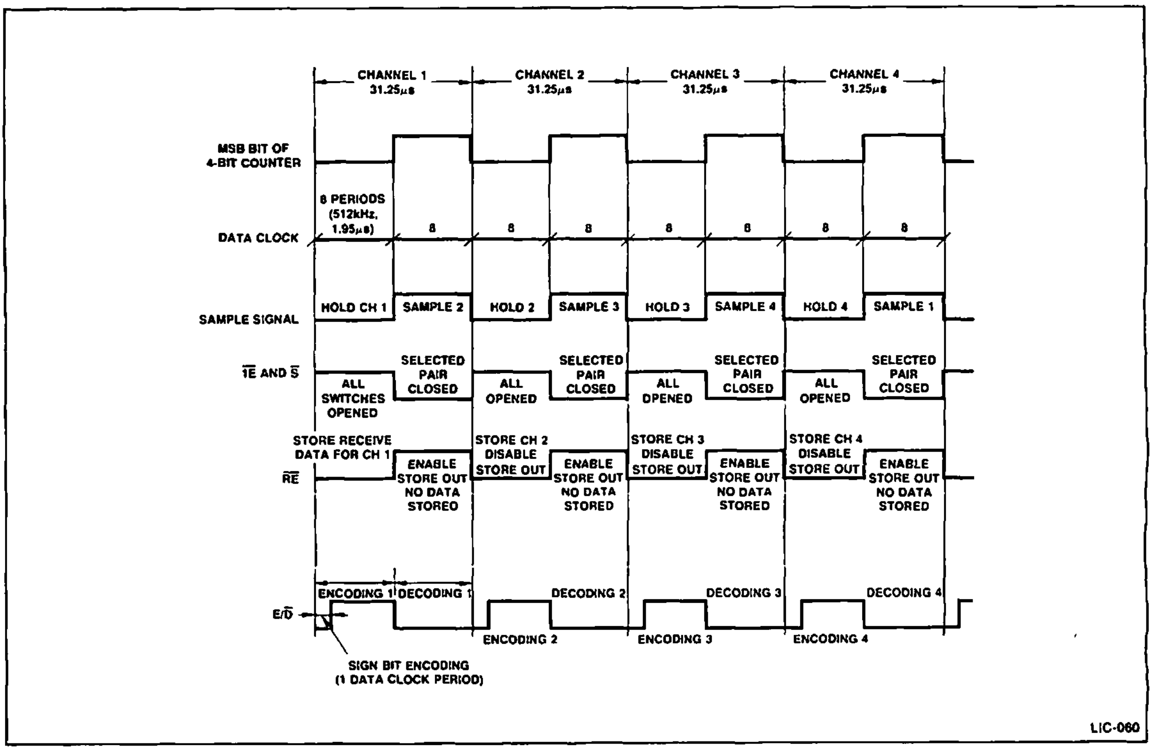


Fig. 40. Ideal Timing Diagrams for 4-Channel PCM CODEC.

Line Drivers/Receivers – Section IV

Line Drivers/Receivers — Section IV (Cont.)

Application Notes

Am1488

Quad RS-232C Line Driver

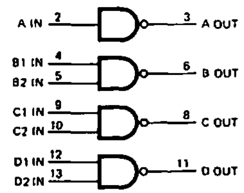
Distinctive Characteristics:

- Conforms to EIA specification RS-232C
- Short circuit protected output
- Simple slew rate control with external capacitor
- 100% reliability assurance testing in compliance with MIL STD 883
- TTL/DTL compatible input

FUNCTIONAL DESCRIPTION

The Am1488 is a quad line driver that conforms to EIA specification RS-232C. Each driver accepts one or two TTL/DTL inputs and produces a high-level logic signal on its output. The HIGH and LOW logic levels on the output are defined by the positive and negative power supplies to the drivers. For power supplies of plus and minus nine volts, the output levels are guaranteed to meet the ±6-volt specification with a 3kΩ load. There is an internal 300Ω resistor in series with the output to provide current limiting in both the HIGH and LOW logic levels. The Am1488 driver is intended for use with the Am1489 or Am1489A quad line receivers.

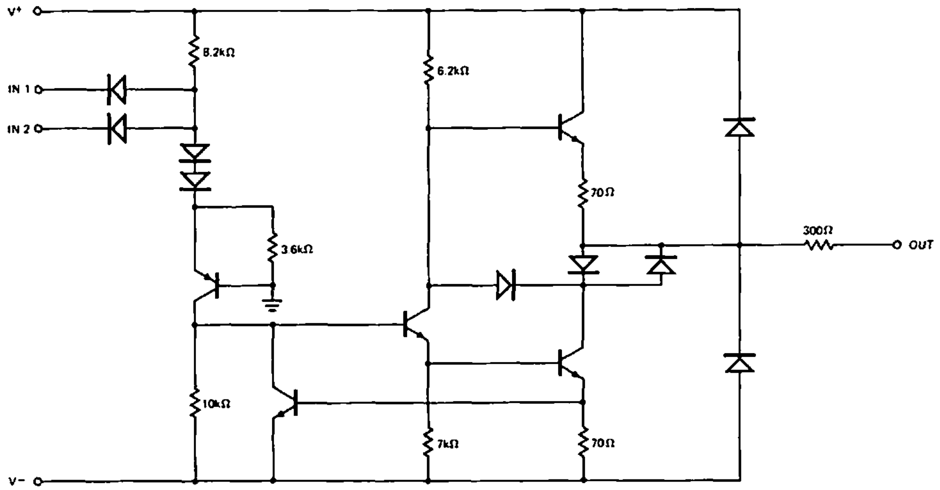
LOGIC SYMBOL



V– = Pin 1
= Pin 14
GND = Pin 7

LIC-316

CIRCUIT DIAGRAM
(one driver shown)

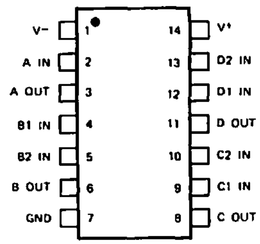


LIC-317

Am1488 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +75°C	MC1488L
Molded DIP	0°C to +75°C	AM1488PC
Dice	0°C to +75°C	AM1488XC

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

LIC-318

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +175°C
Temperature (Ambient) Under Bias	0°C to +75°C
Supply Voltage to Ground Potential	V^+ +15V V^- −15V
DC Voltage Applied to Outputs for High Output State	$(V^+ +5.0V) \geq V_o \geq (V^- -5.0V)$
DC Input Voltage	±15V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The following conditions apply unless otherwise specified:
T_A = 0°C to +75°C, V^+ = +9.0V, V^- = −9.0V

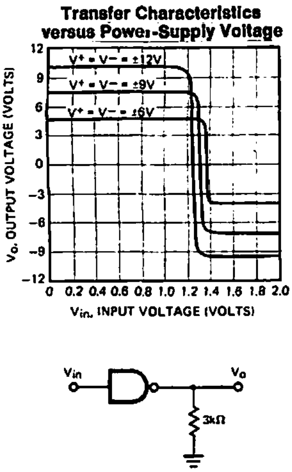
Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
I_{IL}	Logical "0" Input Current	V_{IN} = 0V			−1.0	−1.6	mA
I_{IH}	Logical "1" Input Current	V_{IN} = +5.0V			0.005	10.0	μA
V_{OH}	High Level Output Voltage	R_L = 3.0kΩ,	V^+ = 9.0V, V^- = −9.0V	6.0	7.0		Volts
		V_{IN} = 0.8V	V^+ = 13.2V, V^- = −13.2V	9.0	10.5		Volts
V_{OL}	Low Level Output Voltage	R_L = 3.0kΩ,	V^+ = 9.0V, V^- = −9.0V	−6.0	−6.8		Volts
		V_{IN} = 1.9V	V^+ = 13.2V, V^- = −13.2V	−9.0	−10.5		Volts
$I_{SC}+$	High Level Output Short-Circuit Current	V_{OUT} = 0V, V_{IN} = 0.8V		−6.0	−10.0	−12.0	mA
$I_{SC}-$	Low Level Output Short-Circuit Current	V_{OUT} = 0V, V_{IN} = 1.9V		6.0	10.0	12.0	mA
R_{OUT}	Output Resistance	$V^+ = V^-$ = 0V, V_{OUT} = ±2.0V		300			Ω
$I_{CC}+$	Positive Supply Current (Output Open)	V_{IN} = 1.9V	V^+ = 9.0V, V^- = −9.0V		15.0	20.0	mA
			V^+ = 12V, V^- = −12V		19.0	25.0	mA
			V^+ = 15V, V^- = −15V		25.0	34.0	mA
		V_{IN} = 0.8V	V^+ = 9.0V, V^- = 9.0V		4.5	6.0	mA
			V^+ = 12V, V^- = −12V		5.5	7.0	mA
			V^+ = 15V, V^- = −15V		8.0	12.0	mA
$I_{CC}-$	Negative Supply Current (Output Open)	V_{IN} = 1.9V	V^+ = 9.0V, V^- = −9.0V		−13.0	−17.0	mA
			V^+ = 12V, V^- = −12V		−18.0	−23.0	mA
			V^+ = 15V, V^- = −15V		−25.0	−34.0	mA
		V_{IN} = 0.8V	V^+ = 9.0V, V^- = −9.0V		−1.0	−15	μA
			V^+ = 12V, V^- = −12V		−1.0	−15	μA
			V^+ = 15V, V^- = −15V		−0.01	−2.5	mA
P_d	Power Dissipation	V^+ = 9.0V, V^- = −9.0V			252	333	mW
		V^+ = 12V, V^- = −12V			444	576	mW

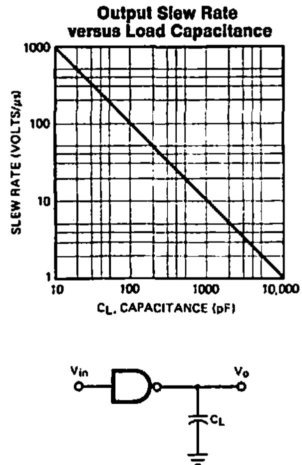
Switching Characteristics (T_A = 25°C, V^+ = +9.0V, V^- = −9.0V)

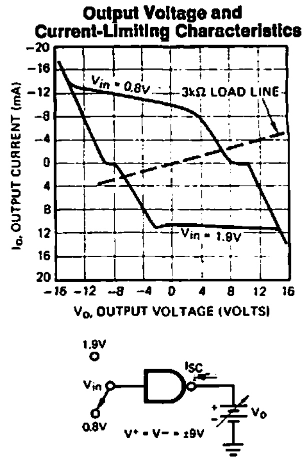
Parameters	Definition	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Delay from input LOW to output HIGH	Z_L = 3.0 kΩ and 15 pF		275	350	ns
t_{PHL}	Delay from input HIGH to output LOW			110	175	ns
t_r	Output rise time			55	100	ns
t_f	Output fall time			45	75	ns

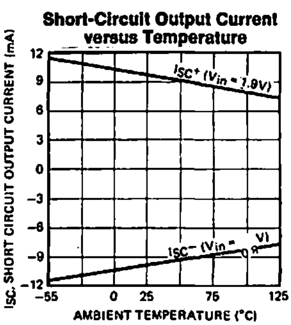
Note 1. Typical values are for T_A = 25°C.

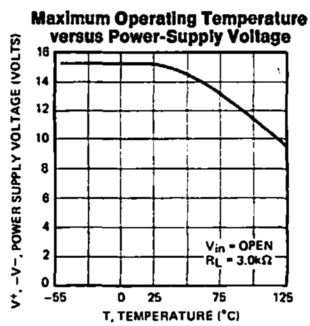
TYPICAL CHARACTERISTICS





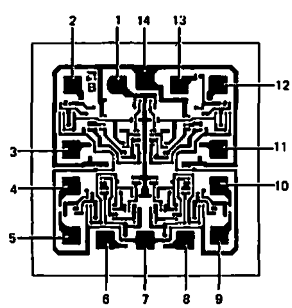






LIC-319

Metallization and Pad Layout



DIE SIZE 0.053" X 0.054"

Am1489 • Am1489A

Quad RS-232C Line Receivers

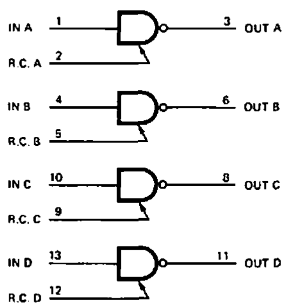
Distinctive Characteristics:

- Compatible with EIA specification RS-232C
- Input signal range ±30 volts
- 100% reliability assurance testing in compliance with MIL STD 883
- Includes response control input and built-in hysterisis

FUNCTIONAL DESCRIPTION:

The Am1489 and Am1489A are quad line receivers whose electrical characteristics conform to EIA specification RS-232C. Each receiver has a single data input that can accept signal swings of up to ±30 V. The output of each receiver is TTL/DTL compatible, and includes a 2kΩ resistor pull-up to V_{CC}. An internal feedback resistor causes the input to exhibit hysterisis so that AC noise immunity is maintained at a high level even near the switching thresholds. For both devices, when a receiver is in a LOW state on the output, the input may drop as LOW as 1.25 volts without affecting the output. Both devices are guaranteed to switch to the HIGH state when the input voltage is below 0.75 V. Once the output has switched to the HIGH state, the input may rise to 1.0 V for the Am1489 or 1.75 V for the Am1489A without causing a change in the output. The Am1489 is guaranteed to switch to a LOW output when its input reaches 1.5 V and, the Am1489A is guaranteed to switch to a LOW output when its input reaches 2.25 V. Because of this hysterisis in switching thresholds, the devices can receive signals with superimposed noise or with slow rise and fall times without generating oscillations on the output. The threshold levels may be offset by a constant voltage by applying a DC bias to the response control input. A capacitor added to the response control input will reduce the frequency response of the receiver for applications in the presence of high frequency noise spikes. The companion line driver is the *Am1488.*

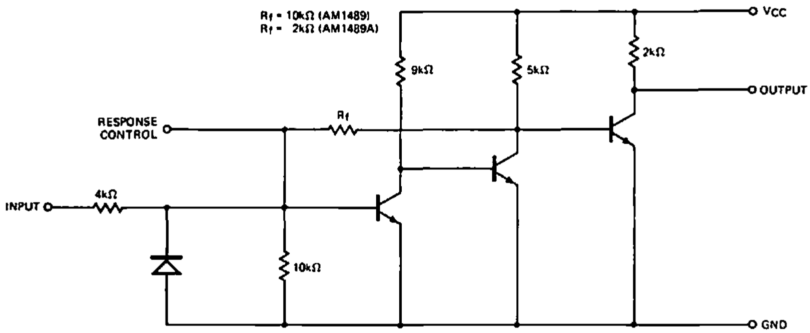
LOGIC SYMBOL



V_{CC} = PIN 14
GND = PIN 7

LIC-320

CIRCUIT DIAGRAM
(one receiver)

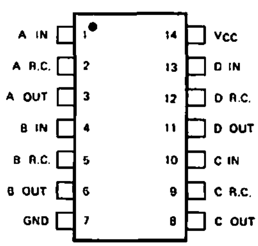


LIC-321

Am1489/Am1489A ORDERING INFORMATION

Package Type	Temperature Range	Am1489 Order Number	Am1489A Order Number
14-pin Molded DIP	0°C to +75°C	AM1489PC	AM1489APC
14-pin Hermetic DIP	0°C to +75°C	MC1489L	MC1489AL
Dice	0°C to +75°C	AM1489XC	AM1489AXC

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

LIC-322

4

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +175°C
Temperature (Ambient) Under Bias	0°C to +75°C
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous	−0.5 V to +10 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to $+V_{CC}$ max
Input Signal Range	−30 V to +30 V
Output Current, Into Outputs	30 mA
DC Input Current	Defined by Input Voltage Limits

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am1489, Am1489A $T_A = 0°C$ to $+75°C$ $V_{CC} = 5.0\ V \pm 1\%$ Response control pin open

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -0.5$ mA, $V_{IN} = +0.75$ V or open		2.6	4.0		Volts
V_{OL}	Output LOW Voltage	$I_{OL} = 10$ mA, $V_{IN} = 3.0$ V			0.2	0.45	Volts
V_{IH}	Input HIGH Level Threshold	$T_A = 25°C$, $V_{OL} = 0.45$ V	Am1489	1.0	1.25	1.5	Volts
			Am1489A	1.75	1.95	2.25	
V_{IL}	Input LOW Level Threshold	$T_A = 25°C$, $V_{OH} = +2.5$ V		0.75		1.25	Volts
I_{IL}	Input LOW Current	$V_{IN} = -3.0$ V		−0.43			mA
		$V_{IN} = -25$ V		−3.6		−8.3	
I_{IH}	Input HIGH Current	$V_{IN} = +3.0$ V		0.43			mA
		$V_{IN} = +25$ V		3.6		8.3	
I_{SC}	Output Short Circuit Current	$V_{IN} = 0.0$ V, $V_{OUT} = 0.0$ V			3.0		mA
I_{CC}	Power Supply Current	$V_{CC} = $ MAX.			20	26	mA

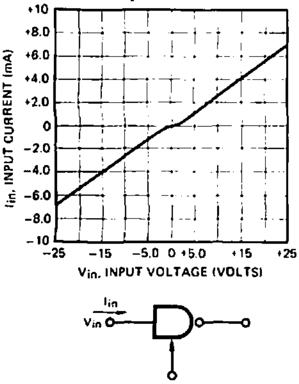
Note: 1) Typical Limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.

Switching Characteristics ($T_A = 25°C$, response control pin open, $C_L = 15$ pF)

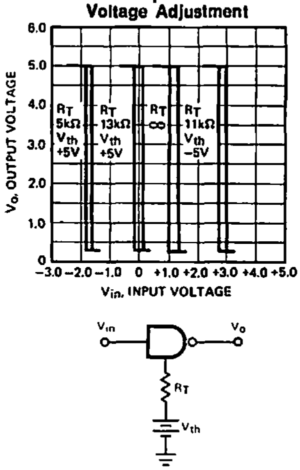
Parameters	Definition	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Delay from Input LOW to Output HIGH	$R_L = 3.9$ kΩ		25	85	ns
t_{PHL}	Delay from Input HIGH to output LOW	$R_L = 390$ Ω		25	50	ns
t_r	Output Rise Time (10% to 90%)	$R_L = 3.9$ kΩ		120	175	ns
t_f	Output Fall Time (90% to 10%)	$R_L = 390$ Ω		10	20	ns

TYPICAL CHARACTERISTICS

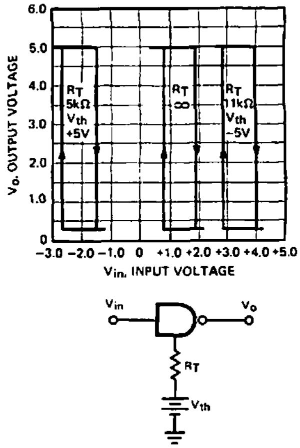
Input Current



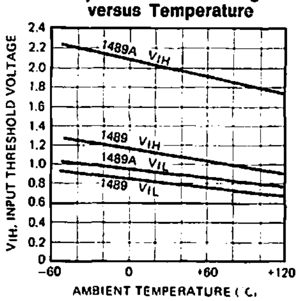
Am1489 Input Threshold Voltage Adjustment



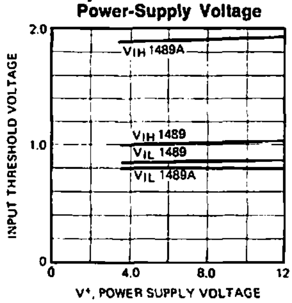
Am1489A Input Threshold Voltage Adjustment



Input Threshold Voltage versus Temperature

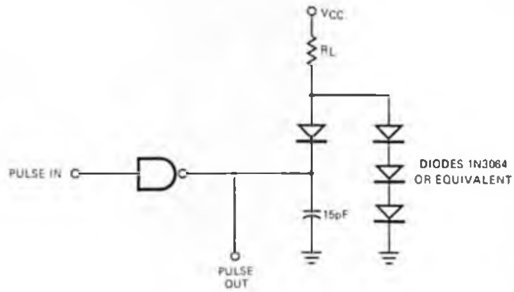


Input Threshold versus Power-Supply Voltage

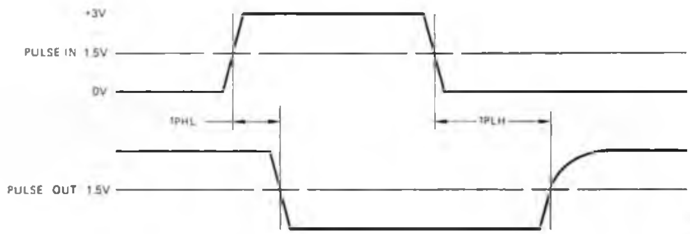


LIC-323

SWITCHING TIME TEST CIRCUIT & WAVEFORMS

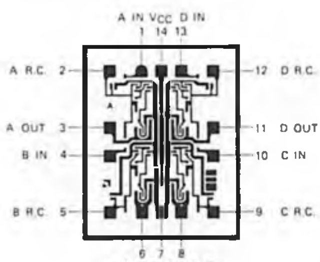


LIC-324



LIC-325

Metallization and Pad Layout



DIE SIZE 0.047" X 0.059"

Am1692/3692

Three-State Differential Line Drivers

DISTINCTIVE CHARACTERISTICS

- Individual three-state enables for each driver
- Dual differential driver or quad single ended line driver
- Short circuit protection for both source and sink outputs
- Individual rise time control for each output
- 50Ω transmission line drive capability
- High capacitive load drive capability
- Low I_{CC} and I_{EE} power consumption
  Differential mode 35mW/driver
  Single-ended mode 26mW/driver
- Low current PNP inputs compatible with TTL, MOS and CMOS
- Advanced low power Schottky processing
- 100% reliability assurance screening to MIL-STD-883 requirements

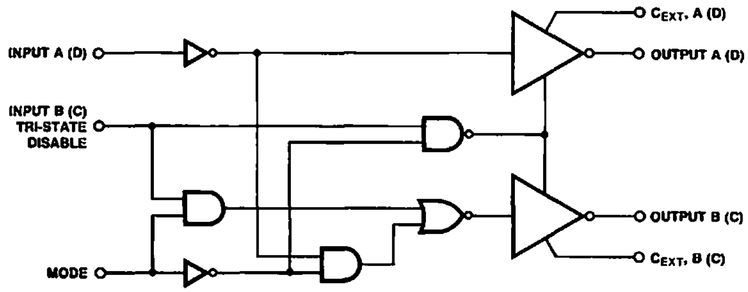
FUNCTIONAL DESCRIPTION

The Am1692/Am3692 are low power Schottky TTL line drivers with three-state outputs. They feature ±10V output common mode range in three-state and 0V output unbalance when operated with ±5V power supplies. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection.

A mode control input provides a choice of operation either as four independent line drivers or two differential line drivers. A rise time control pin allows the use of an external capacitor to reduce rise time for suppression of near end crosstalk to other receivers in the cable.

The Am1692/3692 is constructed using advanced low-power Schottky processing.

LOGIC DIAGRAM
(1/2 Circuit Shown)

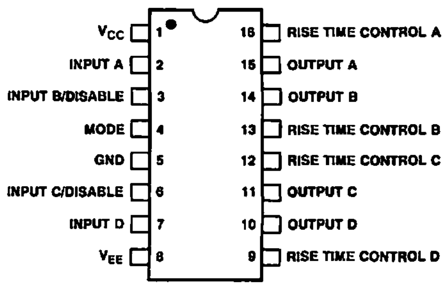


LIC-326

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	DS1692J
Hermetic Flat Pak	−55°C to +125°C	DS1692F
Hermetic DIP	0°C to +70°C	DS3692J
Molded DIP	0°C to +70°C	DS3692N

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-327

4

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Supply Voltage V+	7.0V
V−	−7.0V
Power Dissipation	600mW
Input Voltage	−0.5 to +15V
Output Voltage (Power Off)	±15V
Lead Soldering Temperature (10 seconds)	300°C

ELECTRICAL CHARACTERISTICS over the operating temperature range

The following conditions apply unless otherwise specified:

Am1692 (MIL) T_A = −55°C to +125°C V_{CC} = 5.0V ±10%, V_{EE} = GND
Am3692 (COM'L) T_A = 0°C to +70°C V_{CC} = 5.0V ±5%, V_{EE} = GND
Mode Voltage ≤ 0.8V

DC CHARACTERISTICS over the operating temperature range

Parameters	Description	Test Conditions (Note 2)		Min.	Typ. (Note 1)	Max.	Units
V_O	Differential Output Voltage, $V_{A,B}$	$R_L = \infty$	V_{IN} = 2.0V	2.5	3.6	6.0	Volts
$\overline{V_O}$			V_{IN} = 0.8V	−2.5	−3.6	−6.0	Volts
V_T	Differential Output Voltage, $V_{A,B}$	R_L = 100Ω	V_{IN} = 2.0V	2	2.6		Volts
$\overline{V_T}$			V_{IN} = 0.8V	−2	−2.6		Volts
V_{OS}, $\overline{V_{OS}}$	Common-Mode Offset Voltage	R_L = 100Ω			2.5	3	Volts
$\|V_T\| - \|\overline{V_T}\|$	Difference in Differential Output Voltage	R_L = 100Ω			0.05	0.4	Volts
$\|V_{OS}\| - \|\overline{V_{OS}}\|$	Difference in Common-Mode Offset Voltage	R_L = 100Ω			0.05	0.4	Volts
V_{SS}	$\|V_T - \overline{V_T}\|$	R_L = 100Ω		4.0	4.8		Volts
I_{XA}	Output Leakage Current	V_{CC} = 0	V_O = 15V		10	150	μA
I_{XB}			V_O = −15V		−10	−150	μA
I_{OX}	Three-State Output Current	V_{IN} = 2.4V, $V_O \geq$ −10V				−150	μA
		V_{IN} = 0.4V, $V_O \leq$ 15V				150	μA
I_{SA}	Output Short Circuit Current	V_{IN} = 2.4V	V_{OA} = 6.0V		80	150	mA
			V_{OB} = 0V		−80	−150	mA
I_{SB}		V_{IN} = 0.4V	V_{OA} = 0V		−80	−150	mA
			V_{OB} = 6.0V		80	150	mA
I_{CC}	Supply Current				18	30	mA

Notes: 1. Typical limits are at V_{OC} = 5.0V, V_{EE} = GND, 25°C ambient and maximum loading.
2. R_L connected between each output and its complement.

ELECTRICAL CHARACTERISTICS over the operating temperature range
The following conditions apply unless otherwise specified:

Am1692 (MIL)	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%, V_{EE} = −5.0V ±10%
Am3692 (COM'L)	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%, V_{EE} = −5.0V ±5%
Mode Voltage ≤ 0.8V		

DC CHARACTERISTICS over the operating temperature range unless otherwise noted

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_O	Output Voltage	$R_L = \infty$	V_{IN} = 2.4V	7	8.5	12	Volts
V_O			V_{IN} = 0.4V	−7	−8.5	−12	Volts
V_T	Output Voltage	R_L = 200Ω	V_{IN} = 2.4V	6	7.3		Volts
V_T			V_{IN} = 0.4V	−6	−7.3		Volts
$\lvert V_T \rvert - \lvert V_T \rvert$	Output Unbalance	$\lvert V_{CC} \rvert = \lvert V_{EE} \rvert$, R_L = 200Ω			0.02	0.4	Volts
I_X^+	Output Leakage Power OFF	$V_{CC} = V_{EE}$ = 0V	V_O = 15V		20	150	μA
I_X^-			V_O = −15V		−20	−150	μA
I_{OX}	Three-State Output Current	V_{IN} = 2.4V, V_O ≥ −10V				−150	μA
		V_{IN} = 0.4V, V_O ≤ 10V				150	μA
I_S^+	Output Short Circuit Current	V_O = 0V	V_{IN} = 2.4V		−80	−150	mA
I_S^-			V_{IN} = 0.4V		80	150	mA
I_{SLEW}	Slew Control Current				±140		μA
I_{CC}	Positive Supply Current	V_{IN} = 0.4V, $R_L = \infty$			18	30	mA
I_{EE}	Negative Supply Current	V_{IN} = 0.4V, $R_L = \infty$			−10	−22	mA
V_{IH}	High Level Input Voltage	±5.25 ≤ V_{EE} ≤ 0V		2			Volts
V_{IL}	Low Level Input Voltage					0.8	Volts
I_{IH}	High Level Input Current		V_{IN} = 2.4V		1	40	μA
			V_{IN} ≤ 15V		10	100	μA
I_{IL}	Low Level Input Current		V_{IN} = 0.4V		−30	−200	μA
V_I	Input Clamp Voltage		I_{IN} = −12mA			−1.5	Volts

Note: Typical values are at V_{CC} = 5.0V, V_{EE} = −5.0V, 25°C ambient and maximum loading.

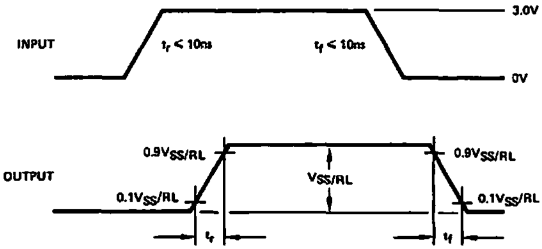
AC CHARACTERISTICS T_A = 25°C

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{CC} = 5.0V, Mode Select = 8.0V						
t_r	Differential Output Rise Time	R_L = 100Ω, C_L = 500pF, (Fig. 1)		120	200	ns
t_f	Differential Output Fall Time	R_L = 100Ω, C_L = 500pF, (Fig. 1)		120	200	ns
t_{PDH}	Output Propagation Delay	R_L = 100Ω, C_L = 500pF, (Fig. 1)		120	200	ns
t_{PDL}	Output Propagation Delay	R_L = 100Ω, C_L = 500pF, (Fig. 1)		120	200	ns
t_{PZL}	Three-State Delay	R_L = 100Ω, C_L = 500pF, (Fig. 2)		180	250	ns
t_{PZH}	Three-State Delay	R_L = 100Ω, C_L = 500pF, (Fig. 2)		180	250	ns
t_{PLZ}	Three-State Delay	R_L = 100Ω, C_L = 500pF, (Fig. 2)		80	150	ns
t_{PHZ}	Three-State Delay	R_L = 100Ω, C_L = 500pF, (Fig. 2)		80	150	ns
V_{CC} = 5.0V, V_{EE} = −5.0V, Mode Select = 0.8V						
t_r	Differential Output Rise Time	R_L = 200Ω, C_L = 500pF, (Fig. 1)		190	300	ns
t_f	Differential Output Fall Time	R_L = 200Ω, C_L = 500pF, (Fig. 1)		190	300	ns
t_{PDL}	Output Propagation Delay	R_L = 200Ω, C_L = 500pF, (Fig. 1)		190	300	ns
t_{PDH}	Output Propagation Delay	R_L = 200Ω, C_L = 500pF, (Fig. 1)		190	300	ns
t_{PZL}	Three-State Delay	R_L = 200Ω, C_L = 500pF, (Fig. 2)		180	250	ns
t_{PZH}	Three-State Delay	R_L = 200Ω, C_L = 500pF, (Fig. 2)		180	250	ns
t_{PLZ}	Three-State Delay	R_L = 200Ω, C_L = 500pF, (Fig. 2)		80	150	ns
t_{PHZ}	Three-State Delay	R_L = 200Ω, C_L = 500pF, (Fig. 2)		80	150	ns

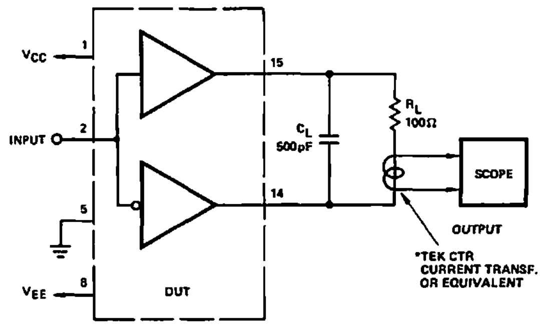
Am1692/3692 FUNCTIONAL TABLE

Mode	Inputs A(D)	Inputs B(C)	Outputs A(D)	Outputs B(C)
0	0	0	0	1
0	0	1	Z	Z
0	1	0	1	0
0	1	1	Z	Z
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUIT



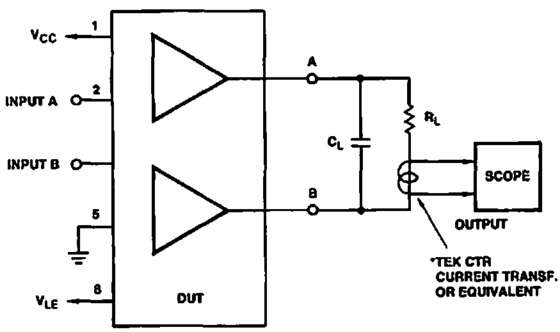
BLI-008



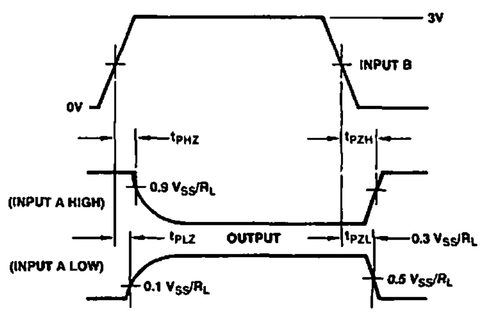
BLI-009

*Current probe is the easiest way to display a differential waveform.

Figure 1. Rise and Fall Time



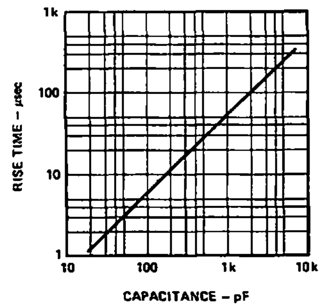
LIC-328



LIC-329

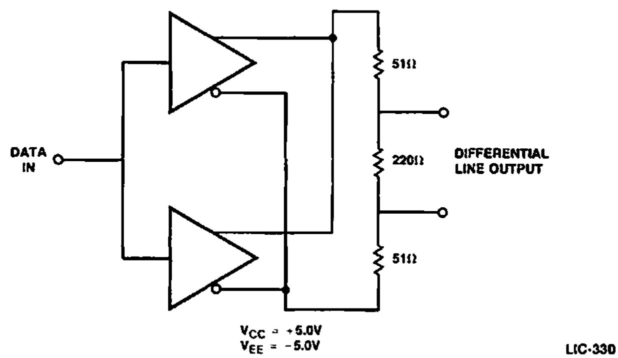
Figure 2. Three State Delays

Slew Rate (Rise or Fall Time) Versus External Capacitor



APPLICATION

Am1692/3692 USED AS A DRIVER MEETING MIL-STD-188-114



Am25LS240 • Am54LS/74LS240

Octal Three-State Inverting Drivers

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- Data-to-output propagation delay times – 18ns MAX.
- Enable-to-output – 30ns MAX.
- Am25LS240 specified at 48mA output current
- 20 pin hermetic and molded DIP packages
- 100% product assurance testing to MIL-STD-883 requirements

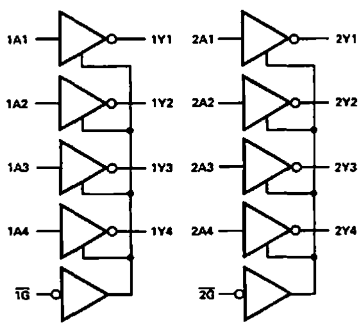
FUNCTIONAL DESCRIPTION

The 'LS240 is an octal inverting line driver fabricated using advanced low-power Schottky technology. The 20-pin package provides improved printed circuit board density for use in memory address and clock driver applications.

Three-state outputs are provided to drive bus lines directly. The Am25LS240 is specified at 48mA and 24mA output sink current, while the Am54/74LS240 is guaranteed at 12mA over the military range and 24mA over the commercial range. Four buffers are enabled from one common line and the other four from a second enable line.

Improved noise rejection and high fan-out are provided by input hysteresis and low current PNP inputs.

LOGIC DIAGRAM

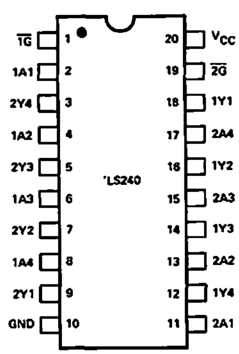


INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Note: All devices have input hysteresis.

LIC-331

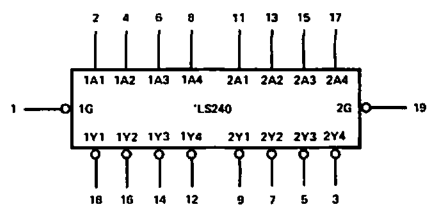
CONNECTION DIAGRAM
Top View



LIC-332

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LIC-333

Am25LS240
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	High-Level Output Voltage	V_{CC} = MIN., V_{IH} = 2.0V, I_{OH} = −3.0mA, V_{IL} = V_{IL}MAX.		2.4	3.4		Volts
		V_{CC} = MIN., V_{IL} = 0.5V	MIL, I_{OH} = −12mA	2.0			
			COM'L, I_{OH} = −15mA	2.0			
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN.	All I_{OL} = 12mA		0.25	0.4	Volts
			All I_{OL} = 24mA		0.35	0.5	
			COM'L I_{OL} = 48mA			0.55	
V_{IH}	High-Level Input Voltage	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Low-Level Input Voltage — COM'L					0.8	Volts
	Low-Level Input Voltage — MIL					0.7	
V_{IK}	Input Clamp Voltage	V_{CC} = MIN., I_I = −18mA				−1.5	Volts
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN.		0.2	0.4		Volts
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = MAX., V_{IH} = 2.0V, V_{IL} = V_{IL}MAX.	V_O = 2.7V			20	μA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied		V_O = 0.4V			−20	
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX., V_I = 7.0V				0.1	mA
I_{IH}	High-Level Input Current, Any Input	V_{CC} MAX., V_{IH} = 2.7V				20	μA
I_{IL}	Low-Level Input Current	V_{CC} = MAX., V_{IL} = 0.4V				−200	μA
I_{SC}	Short Circuit Output Current (Note 3)	V_{CC} = MAX.		−40		−225	mA
I_{CC}	Supply Current — V_{CC} = MAX. Outputs open	All Outputs HIGH			13	23	mA
		All Outputs LOW			26	44	
		Outputs at Hi-Z			29	50	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current	150mA
DC Input Current	−30mA to +5.0mA

Am54LS/74LS240
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

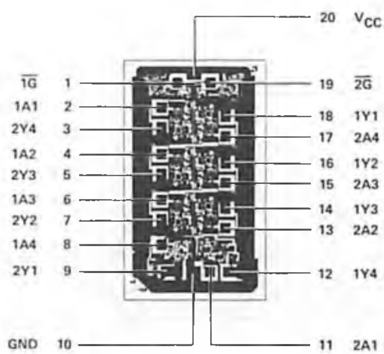
MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V_{OH}	High-Level Output Voltage	V_{CC} = MIN., V_{IH} = 2.0V, I_{OH} = −3.0mA, V_{IL} = V_{IL}MAX.	2.4	3.4		Volts
		V_{CC} = MIN., V_{IL} = 0.5V; MIL, I_{OH} = −12mA	2.0			
		V_{CC} = MIN., V_{IL} = 0.5V; COM'L, I_{OH} = −15mA	2.0			
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN.; All, I_{OL} = 12mA		0.25	0.4	Volts
		V_{CC} = MIN.; COM'L, I_{OL} = 24mA		0.35	0.5	
V_{IH}	High-Level Input Voltage	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Low-Level Input Voltage — COM'L				0.8	Volts
	Low-Level Input Voltage — MIL				0.7	
V_{IK}	Input Clamp Voltage	V_{CC} = MIN., I_I = −18mA			−1.5	Volts
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN.	0.2	0.4		Volts
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = MAX., V_{IH} = 2.0V, V_{IL} = V_{IL}MAX.; V_O = 2.7V			20	μA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied	V_{CC} = MAX., V_{IH} = 2.0V, V_{IL} = V_{IL}MAX.; V_O = 0.4V			−20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX., V_I = 7.0V			0.1	mA
I_{IH}	High-Level Input Current, Any Input	V_{CC} MAX., V_{IH} = 2.7V			20	μA
I_{IL}	Low-Level Input Current	V_{CC} = MAX., V_{IL} = 0.4V			−200	μA
I_{SC}	Short Circuit Output Current (Note 3)	V_{CC} = MAX.	−40		−225	mA
I_{CC}	Supply Current	V_{CC} = MAX. Outputs open; All Outputs HIGH		13	23	mA
		V_{CC} = MAX. Outputs open; All Outputs LOW		26	44	
		V_{CC} = MAX. Outputs open; Outputs at Hi-Z		29	50	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Metallization and Pad Layout



DIE SIZE 0.060" X 0.103"

SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

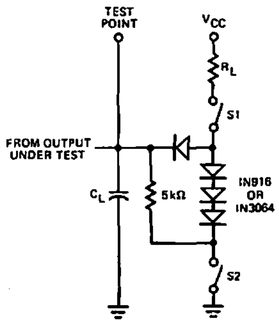
Parameters	Description	Am25LS240 Min.	Am25LS240 Typ.	Am25LS240 Max.	Am54LS/74LS240 Min.	Am54LS/74LS240 Typ.	Am54LS/74LS240 Max.	Units	Test Conditions (Notes 1–5)
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output		8.0	12		9.0	14	ns	C_L = 45pF R_L = 667Ω
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		12	16		12	18	ns	
t_{PZL}	Output Enable Time to Low Level		19	27		20	30	ns	
t_{PZH}	Output Enable Time to High Level		14	20		15	23	ns	
t_{PLZ}	Output Disable Time from Low Level		14	23		15	25	ns	C_L = 5.0pF
t_{PHZ}	Output Disable Time from High Level		10	18		10	18	ns	R_L = 667Ω

Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	Max.	Am25LS MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	Max.	Units	Test Conditions
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output		16		19	ns	C_L = 45pF R_L = 667Ω
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		22		25	ns	
t_{PZL}	Output Enable Time to Low Level		37		42	ns	
t_{PZH}	Output Enable Time to High Level		27		31	ns	
t_{PLZ}	Output Disable Time from Low Level		31		36	ns	C_L = 5.0pF
t_{PHZ}	Output Disable Time from High Level		25		28	ns	R_L = 667Ω

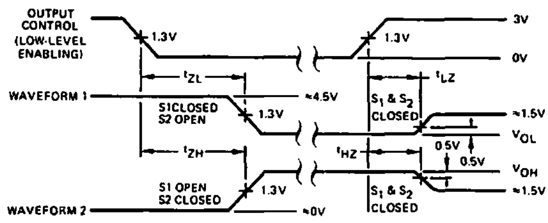
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



LIC-334

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



LIC-335

Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily. PRR ≤ 1.0MHz, Z_{OUT} ≈ 50Ω and t_r ≤ 2.5ns, t_f ≤ 2.5ns.

Am25LS241 • Am54LS/74LS241
Am25LS244 • Am54LS/74LS244

Octal Three-State Buffers

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- Data-to-output propagation delay times – 18ns MAX.
- Enable-to-output – 30ns MAX.
- Am25LS241 and 244 specified at 48mA output current
- 20 pin hermetic and molded DIP packages
- 100% product assurance testing to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The 'LS241 and 'LS244 are octal buffers fabricated using advanced low-power Schottky technology. The 20-pin package provides improved printed circuit board density for use in memory address and clock driver applications.

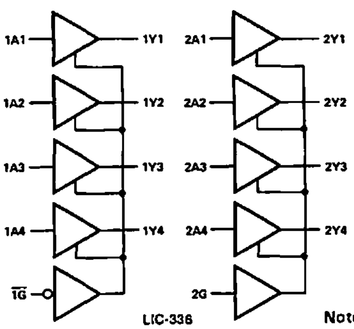
Three-state outputs are provided to drive bus lines directly. The Am25LS241 and Am25LS244 are specified at 48mA and 24mA output sink current, while the Am54LS/74LS241 and Am54LS/74LS244 are guaranteed at 12mA over the military range and 24mA over the commercial range. Four buffers are enabled from one common line and the other four from a second enable line.

The 'LS241 has enable inputs of opposite polarity to allow use as a transceiver without overlap. The 'LS244 enables are of similar polarity for use as a unidirectional buffer in which both halves are enabled simultaneously.

Improved noise rejection and high fan-out are provided by input hysteresis and low current PNP inputs.

LOGIC DIAGRAMS

'LS241



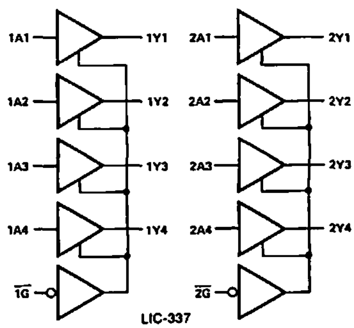
LIC-336

'LS241

INPUTS			OUTPUTS
$\overline{1G}$	2G	A	Y
H	L	X	Z
L	H	H	H
L	H	L	L

Note: All devices have input hysteresis.

'LS244



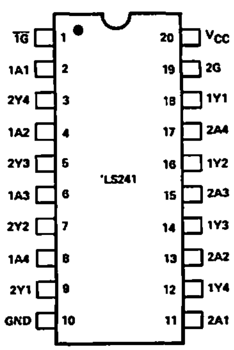
LIC-337

'LS244

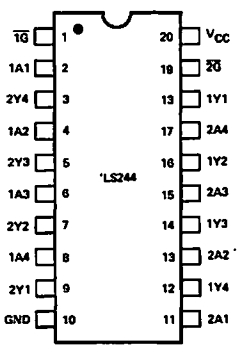
INPUTS		OUTPUT
$\overline{G}$	A	
H	X	Z
L	H	H
L	L	L

CONNECTION DIAGRAMS

Top Views



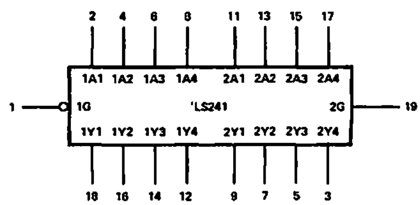
LIC-338



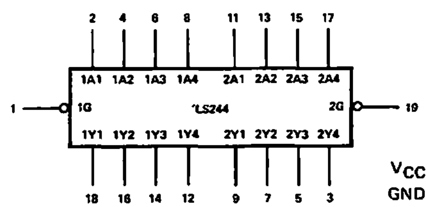
Note: Pin 1 is marked for orientation.

LIC-339

LOGIC SYMBOLS



LIC-340



LIC-341

V_{CC} = Pin 20
GND = Pin 10

Am25LS241 • Am25LS244
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V_{OH}	High-Level Output Voltage	V_{CC} = MIN., V_{IH} = 2.0V, I_{OH} = −3.0mA, V_{IL} = V_{IL}MAX.	2.4	3.4		Volts
		V_{CC} = MIN., V_{IL} = 0.5V; MIL, I_{OH} = −12mA	2.0			
		V_{CC} = MIN., V_{IL} = 0.5V; COM'L, I_{OH} = −15mA	2.0			
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN.; All I_{OL} = 12mA		0.25	0.4	Volts
		V_{CC} = MIN.; All I_{OL} = 24mA		0.35	0.5	
		V_{CC} = MIN.; COM'L, I_{OL} = 48mA			0.55	
V_{IH}	High-Level Input Voltage	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Low-Level Input Voltage — COM'L				0.8	Volts
	Low-Level Input Voltage — MIL				0.7	
V_{IK}	Input Clamp Voltage	V_{CC} = MIN., I_I = −18mA			−1.5	Volts
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN.	0.2	0.4		Volts
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = MAX., V_{IH} = 2.0V, V_{IL} = V_{IL}MAX.; V_O = 2.7V			20	μA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied	V_{CC} = MAX., V_{IH} = 2.0V, V_{IL} = V_{IL}MAX.; V_O = 0.4V			−20	
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX., V_I = 7.0V			0.1	mA
I_{IH}	High-Level Input Current, Any Input	V_{CC} = MAX., V_{IH} = 2.7V			20	μA
I_{IL}	Low-Level Input Current	V_{CC} = MAX., V_{IL} = 0.4V			−200	μA
I_{SC}	Short Circuit Output Current (Note 3)	V_{CC} = MAX.	−40		−225	mA
I_{CC}	Supply Current, V_{CC} = MAX., Outputs open	All Outputs HIGH		13	23	mA
		All Outputs LOW		27	46	
		Outputs at Hi-Z		32	54	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to $+V_{CC}$ max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current	150mA
DC Input Current	−30mA to +5.0mA

Am54LS/74LS241 • Am54LS/74LS244
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

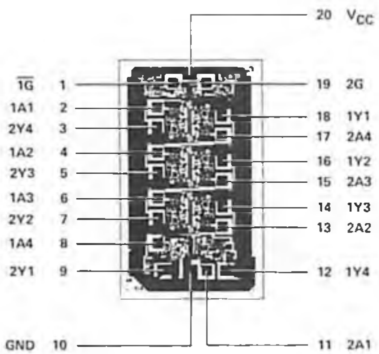
DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V_{OH}	High-Level Output Voltage	V_{CC} = MIN., V_{IH} = 2.0V, I_{OH} = −3.0mA, V_{IL} = V_{IL}MAX.	2.4	3.4		Volts
		V_{CC} = MIN., V_{IL} = 0.5V; MIL, I_{OH} = −12mA	2.0			
		V_{CC} = MIN., V_{IL} = 0.5V; COM'L, I_{OH} = −15mA	2.0			
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN.; All, I_{OL} = 12mA		0.25	0.4	Volts
		V_{CC} = MIN.; COM'L, I_{OL} = 24mA		0.35	0.5	
V_{IH}	High-Level Input Voltage	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Low-Level Input Voltage, COM'L				0.8	Volts
	Low-Level Input Voltage, MIL				0.7	
V_{IK}	Input Clamp Voltage	V_{CC} = MIN., I_I = −18mA			−1.5	Volts
	Hysteresis (V_{T+} − V_{T-})	V_{CC} = MIN.	0.2	0.4		Volts
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = MAX., V_{IH} = 2.0V, V_{IL} = V_{IL}MAX.; V_O = 2.7V			20	μA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied	V_{CC} = MAX., V_{IH} = 2.0V, V_{IL} = V_{IL}MAX.; V_O = 0.4V			−20	
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX., V_I = 7.0V			0.1	mA
I_{IH}	High-Level Input Current, Any Input	V_{CC} = MAX., V_{IH} = 2.7V			20	μA
I_{IL}	Low-Level Input Current	V_{CC} = MAX., V_{IL} = 0.4V			−200	μA
I_{SC}	Short Circuit Output Current (Note 3)	V_{CC} = MAX.	−40		−225	mA
I_{CC}	Supply Current, V_{CC} = MAX. Outputs open	All Outputs HIGH		13	23	mA
		All Outputs LOW		27	46	
		Outputs at Hi-Z		32	54	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

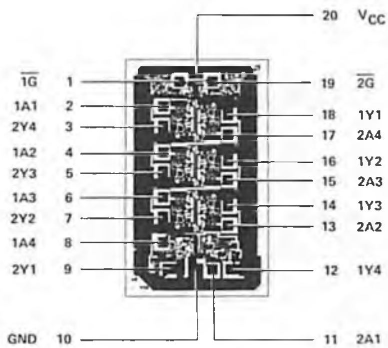
Metallization and Pad Layouts

'LS241



DIE SIZE 0.060" X 0.103"

'LS244



DIE SIZE 0.060" X 0.103"

SWITCHING CHARACTERISTICS
($T_A = +25°C$, $V_{CC} = 5.0V$)

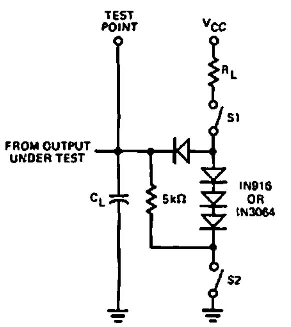
Parameters	Description	Am25LS241 Am25LS244 Min.	Typ.	Max.	Am54LS/74LS241 Am54LS/74LS244 Min.	Typ.	Max.	Units	Test Conditions (Notes 1–5)
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output		10	15		12	18	ns	$C_L = 45pF$ $R_L = 667\Omega$
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		12	18		12	18	ns	
t_{PZL}	Output Enable Time to Low Level		20	30		20	30	ns	
t_{PZH}	Output Enable Time to High Level		15	23		15	23	ns	
t_{PLZ}	Output Disable Time from Low Level		15	25		15	25	ns	$C_L = 5.0pF$ $R_L = 667\Omega$
t_{PHZ}	Output Disable Time from High Level		10	18		10	18	ns	

Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ Min.	Max.	Am25LS MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ Min.	Max.	Units	Test Conditions
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output		21		24	ns	$C_L = 45pF$ $R_L = 667\Omega$
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		25		28	ns	
t_{PZL}	Output Enable Time to Low Level		41		47	ns	
t_{PZH}	Output Enable Time to High Level		31		47	ns	
t_{PLZ}	Output Disable Time from Low Level		34		36	ns	$C_L = 5.0pF$ $R_L = 667\Omega$
t_{PHZ}	Output Disable Time from High Level		25		28	ns	

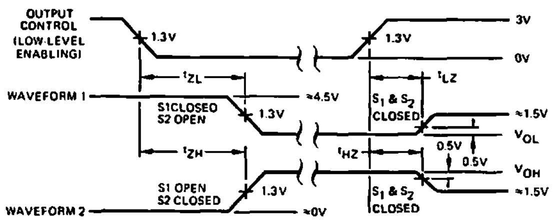
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



LIC-342

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



LIC-343

Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
4. Pulse generator characteristics: PRR ≤ 1.0MHz, $Z_{OUT} \approx 50\Omega$, $t_r \le 15ns$, $t_f \le 6ns$.
5. When measuring t_{PLH} and t_{PHL}, switches S_1 and S_2 are closed.

Am25LS242 • Am54LS/74LS242
Am25LS243 • Am54LS/74LS243

Quad Bus Transceivers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- Data to output propagation delay times – 18ns MAX.
- Enable to output – 30ns MAX.
- Am25LS242 and Am25LS243 are specified at 48mA output current
- 100% product assurance testing to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The 'LS242 and 'LS243 are quad bus transceivers designed for asynchronous two-way communications between data buses.

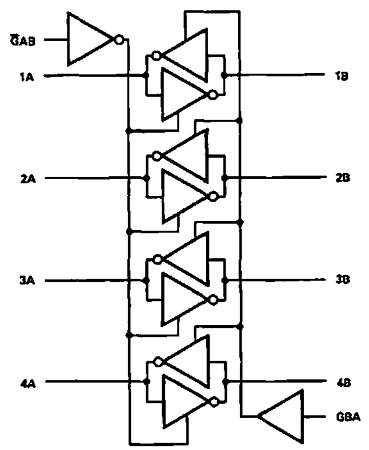
The 'LS242 and 'LS243 have the two 4-line data paths connected input-to-output on both sides to form an asynchronous transceiver/buffer with complementing enable inputs. The 'LS242 is inverting, while the 'LS243 presents non-inverting data at the outputs.

Three-state outputs are provided to drive bus lines directly. The Am25LS242 and Am25LS243 are specified at 48mA and 24mA output sink current, while the Am54/74LS242 and 243 are guaranteed at 12mA over the military range and 24mA over the commercial range.

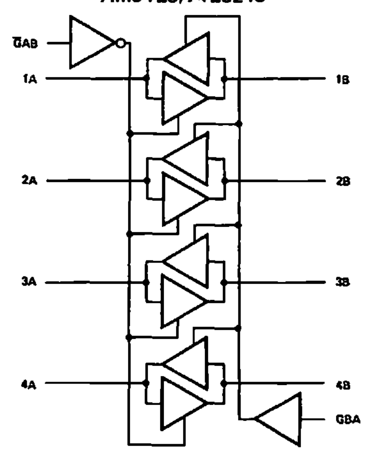
Improved noise rejection and high fan-out are provided by input hysteresis and low current PNP inputs.

LOGIC DIAGRAMS

Am54LS/74LS242



Am54LS/74LS243



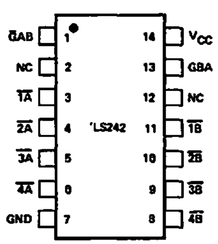
LIC-344

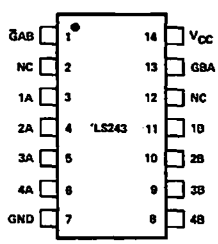
Note: All devices have input hysteresis.

LIC-345

CONNECTION DIAGRAMS

Top Views



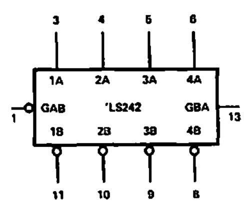


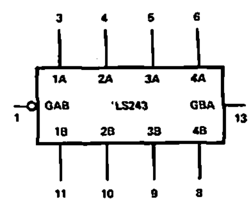
LIC-346

LIC-347

Note: Pin 1 is marked for orientation

LOGIC SYMBOLS





LIC-348

V_{CC} = Pin 14
GND = Pin 7

LIC-349

Am25LS242 • Am25LS243
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	High-Level Output Voltage	V_{CC} = MIN., V_{IH} = 2.0V, I_{OH} = −3.0mA, V_{IL} = V_{IL}MAX.		2.4	3.4		Volts
		V_{CC} = MIN., V_{IL} = 0.5V	MIL, I_{OH} = −12mA	2.0			Volts
			COM'L, I_{OH} = −15mA	2.0			Volts
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN.	All I_{OL} = 12mA		0.25	0.4	Volts
			All I_{OL} = 24mA		0.35	0.5	Volts
			COM'L, I_{OL} = 48mA			0.55	Volts
V_{IH}	High-Level Input Voltage	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Low-Level Input Voltage COM'L					0.8	Volts
	Low-Level Input Voltage MIL					0.7	Volts
V_{IK}	Input Clamp Voltage	V_{CC} = MIN., I_I = −18mA				−1.5	Volts
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN.		0.2	0.4		Volts
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = MAX., V_{IH} = 2.0V, V_{IL} = V_{IL}MAX.	V_O = 2.7V			40	μA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied		V_O = 0.4V			−200	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX.	V_I = 7.0V, $\overline{G}$AB or GBA			0.1	mA
			V_I = 5.5V, A or B			0.1	mA
I_{IH}	High-Level Input Current, Any Input	V_{CC} = MAX., V_{IH} = 2.7V				20	μA
I_{IL}	Low-Level Input Current	V_{CC} = MAX., V_{IL} = 0.4V				−200	μA
I_{SC}	Short Circuit Output Current (Note 3)	V_{CC} = MAX.		−40		−225	mA
I_{CC}	Supply Current (V_{CC} = MAX. Outputs open (Note 4))	All Outputs HIGH	'LS242, 'LS243		22	38	mA
		All Outputs LOW	'LS242, 'LS243		29	50	mA
		Outputs at Hi-Z	'LS242		29	50	mA
			'LS243		32	54	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
4. For 'LS242 and 'LS243 I_{CC} is measured with transceivers enabled in one direction only, or with all transceivers disabled.

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current	150mA
DC Input Current	−30mA to +5.0mA

Am54LS/74LS242 • Am54LS/74LS243
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

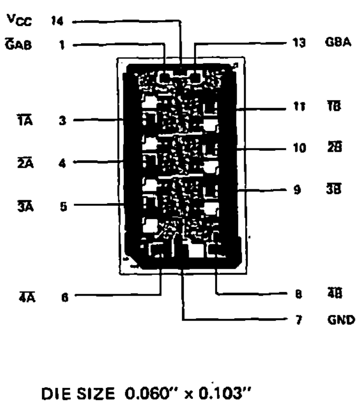
MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

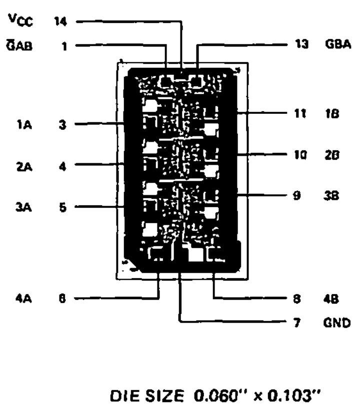
Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V_{OH}	High-Level Output Voltage	V_{CC} = MIN., V_{IH} = 2.0V, I_{OH} = −3.0mA, V_{IL} = V_{IL}MAX.	2.4	3.4		Volts
		V_{CC} = MIN., V_{IL} = 0.5V; MIL, I_{OH} = −12mA	2.0			
		V_{CC} = MIN., V_{IL} = 0.5V; COM'L, I_{OH} = −15mA	2.0			
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN.; All, I_{OL} = 12mA		0.25	0.4	Volts
		V_{CC} = MIN.; COM'L, I_{OL} = 24mA		0.35	0.5	
V_{IH}	High-Level Input Voltage	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Low-Level Input Voltage, COM'L				0.8	Volts
	Low-Level Input Voltage, MIL				0.7	
V_{IK}	Input Clamp Voltage	V_{CC} = MIN., I_I = −18mA			−1.5	Volts
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN.	0.2	0.4		Volts
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = MAX., V_{IH} = 2.0V, V_{IL} = V_{IL}MAX.; V_O = 2.7V			40	μA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied	V_{CC} = MAX., V_{IH} = 2.0V, V_{IL} = V_{IL}MAX.; V_O = 0.4V			−200	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX.; V_I = 7.0V, $\overline{G}$AB or GBA			0.1	mA
		V_{CC} = MAX.; V_I = 5.5V, A or B			0.1	mA
I_{IH}	High-Level Input Current, Any Input	V_{CC} MAX., V_{IH} = 2.7V			20	μA
I_{IL}	Low-Level Input Current	V_{CC} = MAX., V_{IL} = 0.4V			−200	μA
I_{SC}	Short Circuit Output Current (Note 3)	V_{CC} = MAX.	−40		−225	mA
I_{CC}	Supply Current	V_{CC} = MAX. Outputs open (Note 4); All Outputs HIGH; 'LS242, 'LS243		22	38	mA
		All Outputs LOW; 'LS242, 'LS243		29	50	
		Outputs at Hi-Z; 'LS242		29	50	
		Outputs at Hi-Z; 'LS243		32	54	

Notes: 1. For conditions shown as MIN' or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
4. For 'LS242 and 'LS243 I_{CC} is measured with transceivers enabled in one direction only, or with all transceivers disabled.

Metallization and Pad Layouts



DIE SIZE 0.060" x 0.103"



DIE SIZE 0.060" x 0.103"

Am25LS242 • Am54LS/74LS242 SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Am25LS242 Min.	Am25LS242 Typ.	Am25LS242 Max.	Am54LS/74LS242 Min.	Am54LS/74LS242 Typ.	Am54LS/74LS242 Max.	Units	Test Conditions (Notes 1–5)
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output		8.0	12		9.0	14	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		12	16		12	18	ns	
t_{PZL}	Output Enable Time to Low Level		20	30		20	30	ns	
t_{PZH}	Output Enable Time to High Level		15	23		15	23	ns	
t_{PLZ}	Output Disable Time from Low Level		15	25		15	25	ns	C_L = 5.0pF, R_L = 667Ω
t_{PHZ}	Output Disable Time from High Level		10	18		10	18	ns	

Am25LS242 ONLY SWITCHING CHARACTERISTICS OVER OPERATION RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output		16		19	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		22		25	ns	
t_{PZL}	Output Enable Time to Low Level		37		42	ns	
t_{PZH}	Output Enable Time to High Level		29		33	ns	
t_{PLZ}	Output Disable Time from Low Level		33		38	ns	C_L = 5.0pF, R_L = 667Ω
t_{PHZ}	Output Disable Time from High Level		25		28	ns	

Am25LS243 • Am54LS/74LS243 SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

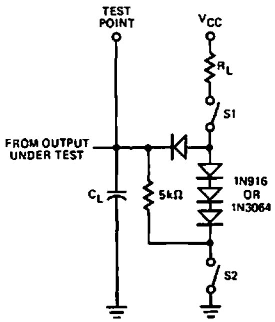
Parameters	Description	Am25LS243 Min.	Am25LS243 Typ.	Am25LS243 Max.	Am54LS/74LS243 Min.	Am54LS/74LS243 Typ.	Am54LS/74LS243 Max.	Units	Test Conditions (Notes 1–5)
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output		10	15		12	18	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		12	18		12	18	ns	
t_{PZL}	Output Enable Time to Low Level		20	30		20	30	ns	
t_{PZH}	Output Enable Time to High Level		15	23		15	23	ns	
t_{PLZ}	Output Disable Time from Low Level		15	25		15	25	ns	C_L = 5.0pF, R_L = 667Ω
t_{PHZ}	Output Disable Time from High Level		10	18		10	18	ns	

Am25LS243 ONLY SWITCHING CHARACTERISTICS OVER OPERATION RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output		21		24	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		25		28	ns	
t_{PZL}	Output Enable Time to Low Level		41		47	ns	
t_{PZH}	Output Enable Time to High Level		33		49	ns	
t_{PLZ}	Output Disable Time from Low Level		36		38	ns	C_L = 5.0pF, R_L = 667Ω
t_{PHZ}	Output Disable Time from High Level		25		28	ns	

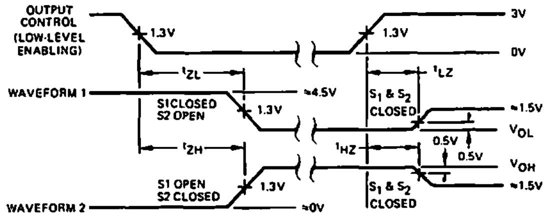
SWITCHING CHARACTERISTICS TEST CONDITIONS

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



LIC-350

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



LIC-351

Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
4. Pulse generator characteristics: PRR < 1MHz, $Z_{OUT} \approx 50\Omega$, $t_r < 15ns$, $t_f < 6ns$.
5. When measuring t_{PLH} and t_{PHL}, switches S_1 and S_2 are closed.

FUNCTION TABLES

Am54LS/74LS242

CONTROL INPUTS		DATA OUTPUTS	
$\overline{G}$AB	GBA	A	B
H	H	$\overline{O}$	I
L	H	*	*
H	L	ISOLATED	
L	L	I	$\overline{O}$

I = Input
O = Output
$\overline{O}$ = Inverting Output

H = HIGH
L = LOW

Am54LS/74LS243

CONTROL INPUTS		DATA OUTPUTS	
$\overline{G}$AB	GBA	A	B
H	H	O	I
L	H	*	*
H	L	ISOLATED	
L	L	I	O

*Possible destructive oscillation may occur if the transceivers are enable in both directions at once.

Am26LS29

Quad Three-State Single Ended RS-423 Line Driver

DISTINCTIVE CHARACTERISTICS

- Four single ended line drivers in one package for maximum package density
- Output short-circuit protection
- Individual rise time control for each output
- 50Ω transmission line drive capability
- High capacitive load drive capability
- Low I_{CC} and I_{EE} power consumption (26mW/driver typ.)
- Meets all requirements of RS-423
- Three-state outputs for bus oriented systems
- Outputs do not clamp line with power off or in hi-impedance state over entire transmission line voltage range of RS-423
- Low current PNP inputs compatible with TTL, MOS and CMOS
- Available in military and commercial temperature range
- Advanced low power Schottky processing
- 100% reliability assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

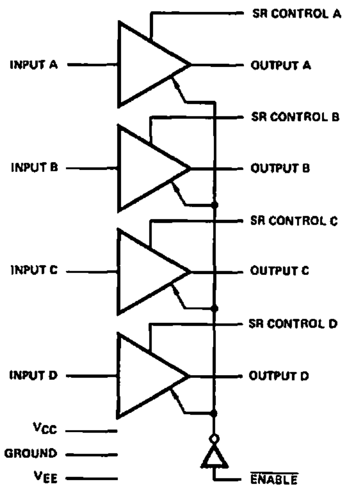
The Am26LS29 is a quad single ended line driver, designed for digital data transmission. The Am26LS29 meets all the requirements of EIA Standard RS-423 and Federal STD 1030. It features four buffered outputs with high source and sink current, and output short circuit protection.

A slew rate control pin allows the use of an external capacitor to control slew rate for suppression of near end cross talk to receivers in the cable.

The Am26LS29 has three-state outputs for bus oriented systems. The outputs in the hi-impedance state will not clamp the line over the transmission line voltage of RS-423. A typical full duplex system would use the Am26LS29 line driver and up to twelve Am26LS32 line receivers or an Am26LS32 line receiver and up to thirty-two Am26LS29 line drivers with only one enabled at a time and all others in the three-state mode.

The Am26LS29 is constructed using advanced low-power Schottky processing.

LOGIC DIAGRAM

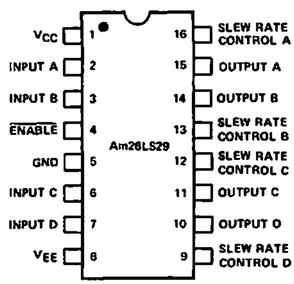


BLI-001

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	AM26LS29DM
Hermetic Flat Pak	−55°C to +125°C	AM26LS29FM
Dice	−55°C to +125°C	AM26LS29XM
Hermetic DIP	0°C to +70°C	AM26LS29DC
Molded DIP	0°C to +70°C	AM26LS29PC
Dice	0°C to +70°C	AM26LS29XC

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLI-004

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Supply Voltage	
V+	7.0V
V–	–7.0V
Power Dissipation	600mW
Input Voltage	–0.5 to +15.0V
Output Voltage (Power Off)	±15V
Lead Soldering Temperature (10 seconds)	300°C

ELECTRICAL CHARACTERISTICS over the operating temperature range

The following conditions apply unless otherwise specified:

Am26LS29XM (MIL) T_A = –55°C to +125°C V_{CC} = 5.0V +10, –5%, V_{EE} = –5.0V –10, +5%

Am26LS29XC (COM'L) T_A = 0°C to +70°C V_{CC} = 5.0V ±5%, V_{EE} = –5.0V ±5%

DC CHARACTERISTICS over the operating temperature range (Notes 1 and 2)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_O	Output Voltage	$R_L = \infty$	V_{IN} = 2.4V	4.0	4.4	6.0	Volts
$\overline{V_O}$			V_{IN} = 0.4V	–4.0	–4.4	–6.0	Volts
V_T	Output Voltage	R_L = 450Ω	V_{IN} = 2.4V	3.6	4.1		Volts
$\overline{V_T}$			V_{IN} = 0.4V	–3.6	–4.1		Volts
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Output Unbalance	$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert$, R_L = 450Ω			0.02	0.4	Volts
I_X+	Output Leakage Power Off	$V_{CC} = V_{EE}$ = 0V	V_O = 10V		2.0	100	μA
I_X-			V_O = –10V		–2.0	–100	μA
I_S+	Output Short Circuit Current	V_O = 0V	V_{IN} = 2.4V		–70	–150	mA
I_S-			V_{IN} = 0.4V		60	150	mA
I_{Slew}	Slew Control Current	$V_{SLEW} = V_{EE}$ + 0.9V			±110		μA
I_{CC}	Positive Supply Current	V_{IN} = 0.4V, $R_L = \infty$			18	30	mA
I_{EE}	Negative Supply Current	V_{IN} = 0.4V, $R_L = \infty$			–10	–22	mA
I_O	Off State (High Impedance) Output Current	V_{CC} = MAX.	V_O = 10V		2.0	100	μA
			V_O = –10V		–2.0	–100	μA
V_{IH}	High Level Input Voltage			2.0			Volts
V_{IL}	Low Level Input Voltage					0.8	Volts
I_{IH}	High Level Input Current	V_{IN} = 2.4V			1.0	40	μA
		V_{IN} < 15V			10	100	μA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			–30	–200	μA
V_I	Input Clamp Voltage	I_{IN} = –12mA				–1.5	Volts

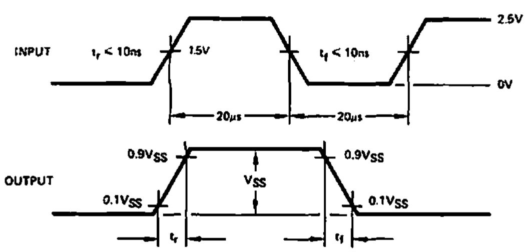
AC CHARACTERISTICS

V_{CC} = 5.0V, V_{EE} = –5.0V, T_A = 25°C

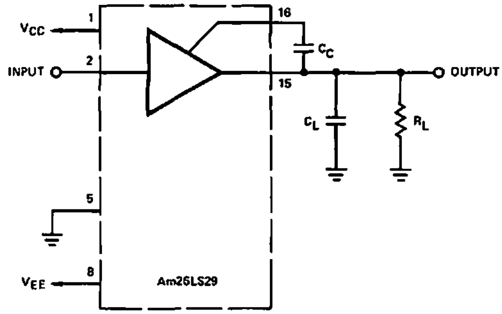
Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
t_r	Rise Time	R_L = 450Ω, C_L = 500pF, Fig. 1	C_C = 50pF		3.0		μs
			C_C = 0pF		120	300	ns
t_f	Fall Time	R_L = 450Ω, C_L = 500pF, Fig. 1	C_C = 50pF		3.0		μs
			C_C = 0pF		120	300	ns
Src	Slew Rate Coefficient	R_L = 450Ω, C_L = 500pF, Fig. 1			.06		μs/pF
t_{LZ}	Output Enable to Output	R_L = 450Ω, C_L = 500pF, C_C = 0pF, Fig. 2			180	300	ns
t_{HZ}					250	350	ns
t_{ZL}		R_L = 450Ω, C_L = 500pF, C_C = 0pF, Fig. 2			250	350	ns
t_{ZH}					180	300	ns

Notes: 1. Typical limits are at V_{CC} = 5.0V, V_{EE} = –5.0V, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-423 where applicable.

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS

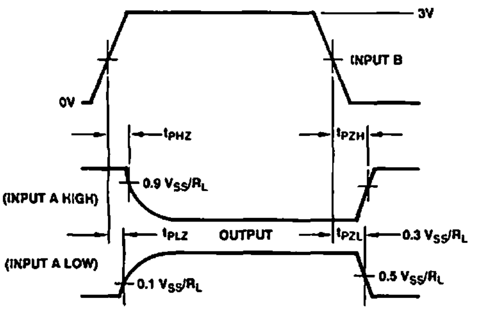


BLI-006



BLI-007

Figure 1. Rise Time Control.



LIC-329

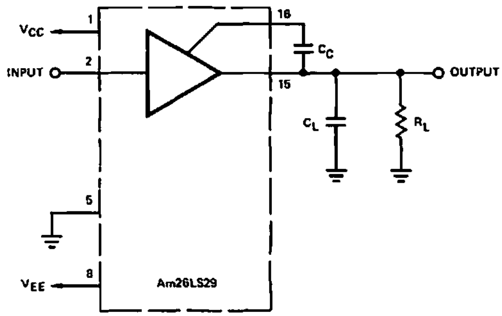
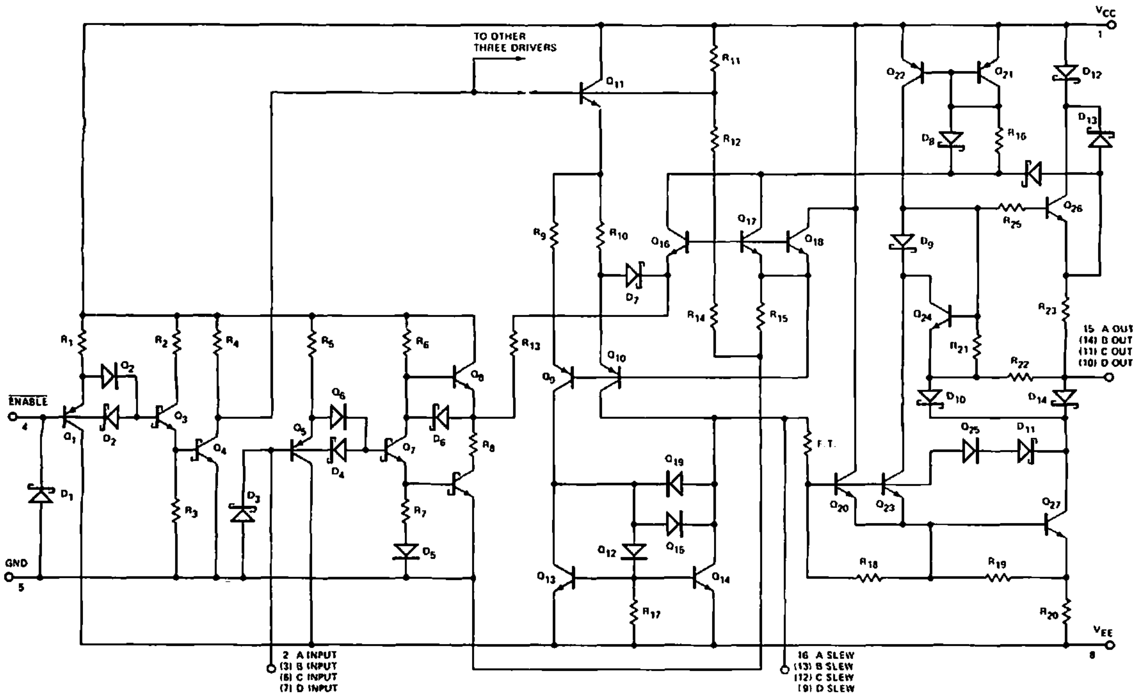


Figure 2. Three State Delays.

BLI-007

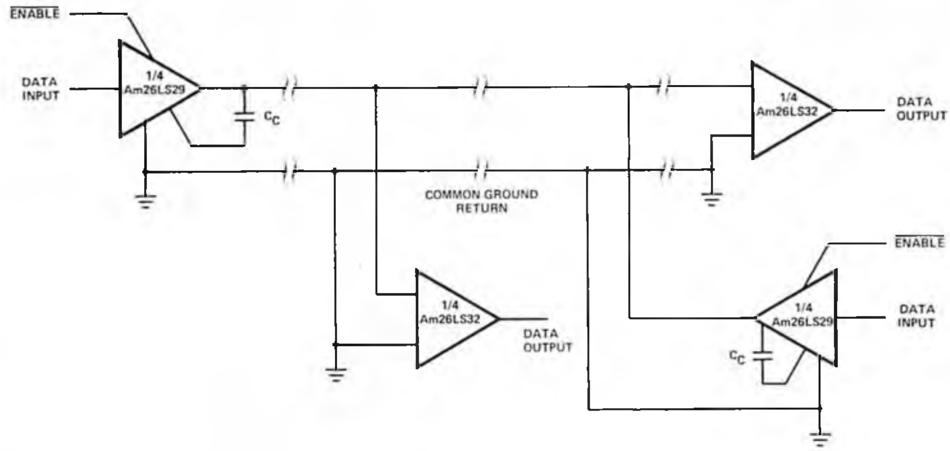
Am26LS29 EQUIVALENT CIRCUIT



BLI-011

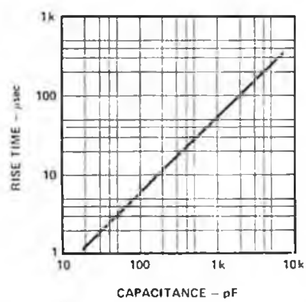
4

TYPICAL APPLICATION



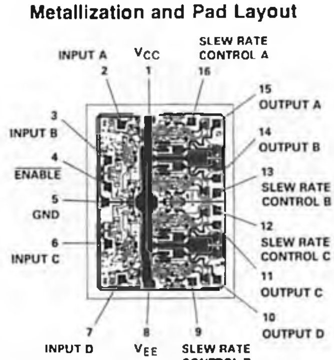
BLI-012

Slew Rate (Rise or Fall Time) Versus External Capacitor



BLI-010

Metallization and Pad Layout



DIE SIZE 0.070" X 0.094"

Am26LS30

Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver

DISTINCTIVE CHARACTERISTICS

- Dual RS-422 line driver or quad RS-423 line driver
- Driver outputs do not clamp line with power off or in hi-impedance state
- Individually three-state drivers when used in differential mode
- Low I_{CC} and I_{EE} power consumption
  - RS-422 differential mode 35mW/driver typ.
  - RS-423 single-ended mode 26mW/driver typ.
- Individual slew rate control for each output
- 50Ω transmission line drive capability (RS-422 into virtual ground)
- Low current PNP inputs compatible with TTL, MOS and CMOS
- High capacitive load drive capability
- Exact replacement for DS16/3691
- Advanced low power Schottky processing
- 100% reliability assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am26LS30 is a line driver designed for digital data transmission. A mode control input provides a choice of operation either as two differential line drivers which meet all of the requirements of EIA Standard RS-422 or four independent single-ended RS-423 line drivers.

In the differential mode the outputs have individual three-state controls. In the hi-impedance state these outputs will not clamp the line over a common mode transmission line voltage of ±10V. A typical full duplex system would be the Am26LS30 differential line driver and up to twelve Am26LS32 line receivers or an Am26LS32 line receiver and up to thirty-two Am26LS30 differential drivers.

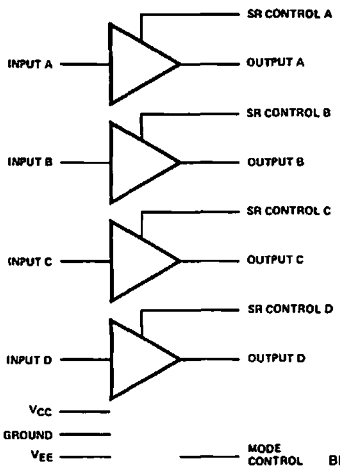
A slew rate control pin allows the use of an external capacitor to control slew rate for suppression of near end cross talk to receivers in the cable.

The Am26LS30 is constructed using Advanced Low Power Schottky processing.

4

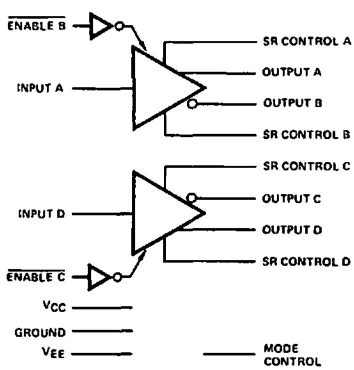
LOGIC DIAGRAMS

Logic for Am26LS30 with Mode Control HIGH (RS-423)



BLI-002

Logic for Am26LS30 with Mode Control LOW (RS-422)

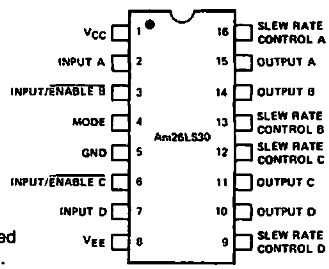


BLI-003

ORDERING INFORMATION

Package Type	**Temperature Range**	**Order Number**
Hermetic DIP	−55°C to +125°C	AM26LS30DM
Hermetic Flat Pak	−55°C to +125°C	AM26LS30FM
Dice	−55°C to +125°C	AM26LS30XM
Hermetic DIP	0°C to +70°C	AM26LS30DC
Molded DIP	0°C to +70°C	AM26LS30PC
Dice	0°C to +70°C	AM26LS30XC

CONNECTION DIAGRAM – Top View



Note:
Pin 1 is marked for orientation.

BLI-005

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Supply Voltage	
V+	7.0V
V−	−7.0V
Power Dissipation	600mW
Input Voltage	−0.5 to +15.0V
Output Voltage (Power Off)	±15V
Lead Soldering Temperature (10 seconds)	300°C

ELECTRICAL CHARACTERISTICS over the operating temperature range

The Following Conditions Apply Unless Otherwise Specified:

Am26LS30XM (MIL) T_A = −55°C to +125°C V_{CC} = 5.0V ±10%, V_{EE} = GND
Am26LS30XC (COM'L) T_A = 0°C to +70°C V_{CC} = 5.0V ±5%, V_{EE} = GND
EIA RS-422 Connection, Mode Voltage = 0.8V

DC CHARACTERISTICS over the operating temperature range

Parameters	Description	Test Conditions (Note 3)		Min.	Typ. (Note 1)	Max.	Units
V_O	Differential Output Voltage, $V_{A,B}$	$R_L = \infty$	V_{IN} = 2.0V		3.6	6.0	Volts
$\overline{V_O}$			V_{IN} = 0.8V		−3.6	−6.0	Volts
V_T	Differential Output Voltage, $V_{A,B}$	R_L = 100Ω	V_{IN} = 2.0V	2.0	2.4		Volts
$\overline{V_T}$			V_{IN} = 0.8V	−2.0	−2.4		Volts
$V_{OS}, \overline{V_{OS}}$	Common Mode Offset Voltage	R_L = 100Ω			2.5	3.0	Volts
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in Differential Output Voltage	R_L = 100Ω			0.005	0.4	Volts
$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$	Difference in Common Mode Offset Voltage	R_L = 100Ω			0.005	0.4	Volts
V_{SS}	$\lvert V_T - \overline{V_T} \rvert$	R_L = 100Ω		4.0	4.8		Volts
V_{CMR}	Output Voltage Common Mode Range	$V_{\overline{ENABLE}}$ = 2.4V		±10			Volts
I_{XA}	Output Leakage Current	V_{CC} = 0V	V_{CMR} = 10V			100	μA
I_{XB}			V_{CMR} = −10V			−100	μA
I_{OX}	Off State (High Impedance) Output Current	V_{CC} = MAX.	$V_{CMR} \leq$ 10V			100	μA
			$V_{CMR} \geq$ −10V			−100	μA
I_{SA}, I_{SB}	Output Short Circuit Current	V_{IN} = 2.4V	V_{OA} = 6.0V		80	150	mA
			V_{OB} = 0V		−80	−150	mA
		V_{IN} = 0.4V	V_{OA} = 0V		−80	−150	mA
			V_{OB} = 6.0V		80	150	mA
I_{CC}	Supply Current				18	30	mA
V_{IH}	High Level Input Voltage			2.0			Volts
V_{IL}	Low Level Input Voltage					0.8	Volts
I_{IH}	High Level Input Current	V_{IN} = 2.4V			1.0	40	μA
		$V_{IN} \leq$ 15V			10	100	μA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−30	−200	μA
V_I	Input Clamp Voltage	I_{IN} = −12mA				−1.5	Volts

AC CHARACTERISTICS

EIA RS-422 Connection, V_{CC} = 5.0V, V_{EE} = GND, Mode = 0.4V, T_A = 25°C

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_r	Differential Output Rise Time	Fig. 2, R_L = 100Ω, C_L = 500pF		120	200	ns
t_f	Differential Output Fall Time	Fig. 2, R_L = 100Ω, C_L = 500pF		120	200	ns
t_{PDH}	Output Propagation Delay	Fig. 2, R_L = 100Ω, C_L = 500pF		120	200	ns
t_{PDL}	Output Propagation Delay	Fig. 2, R_L = 100Ω, C_L = 500pF		120	200	ns
t_{LZ}	Output Enable to Output	R_L = 450Ω, C_L = 500pF, C_C = 0pF, Fig. 3		180	300	ns
t_{HZ}				250	350	
t_{ZL}		R_L = 450Ω, C_L = 500pF, C_C = 0pF, Fig. 3		250	350	
t_{ZH}				180	300	

Notes: 1. Typical limits are at V_{CC} = 5.0V, V_{EE} = GND, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-422 where applicable.
3. R_L connected between each output and its complement.

ELECTRICAL CHARACTERISTICS over the operating temperature range
The following conditions apply unless otherwise specified:

Am26LS30XM (MIL) T_A = −55°C to +125°C V_{CC} = 5.0V ±10%, V_{EE} = −5.0V ±10%
Am26LS30XC (COM'L) T_A = 0°C to +70°C V_{CC} = 5.0V ±5%, V_{EE} = −5.0V ±5%
RS-423 Connection, Mode Voltage > 2.0V

DC CHARACTERISTICS over the operating temperature range (Notes 1 and 2)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_O	Output Voltage	$R_L = \infty$,	V_{IN} = 2.4V	4.0	4.4	6.0	Volts
$\overline{V_O}$		$\|V_{CC}\| = \|V_{EE}\|$ = 4.75V	V_{IN} = 0.4V	−4.0	−4.4	−6.0	Volts
V_T	Output Voltage	R_L = 450Ω,	V_{IN} = 2.4V	3.6	4.1		Volts
$\overline{V_T}$		$\|V_{CC}\| = \|V_{EE}\|$ = 4.75V	V_{IN} = 0.4V	−3.6	−4.1		Volts
$\|V_T\| - \|\overline{V_T}\|$	Output Unbalance	$\|V_{CC}\| = \|V_{EE}\|$, R_L = 450Ω			0.02	0.4	Volts
I_{X+}	Output Leakage Power Off	$V_{CC} = V_{EE}$ = 0V	V_O = 6.0V		2.0	100	μA
I_{X-}			V_O = −6.0V		−2.0	−100	μA
I_{S+}	Output Short Circuit Current	V_O = 0V	V_{IN} = 2.4V		−80	−150	mA
I_{S-}			V_{IN} = 0.4V		80	150	mA
I_{Slew}	Slew Control Current	$V_{SLEW} = V_{EE}$ + 0.9V			±140		μA
I_{CC}	Positive Supply Current	V_{IN} = 0.4V, $R_L = \infty$			18	30	mA
I_{EE}	Negative Supply Current	V_{IN} = 0.4V, $R_L = \infty$			−10	−22	mA
V_{IH}	High Level Input Voltage			2.0			Volts
V_{IL}	Low Level Input Voltage					0.8	Volts
I_{IH}	High Level Input Current	V_{IN} = 2.4V			1.0	40	μA
		V_{IN} < 15V			10	100	μA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−30	−200	μA
V_I	Input Clamp Voltage	I_{IN} = −12mA				−1.5	Volts

4

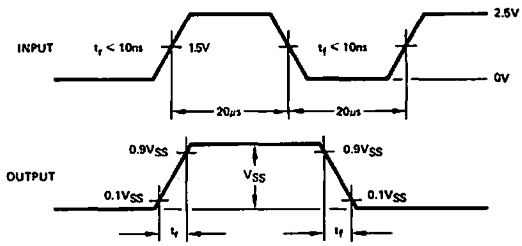
AC CHARACTERISTICS

RS-423 Connection, V_{CC} = 5.0V, V_{EE} = −5.0V, Mode = 2.4V, T_A = 25°C

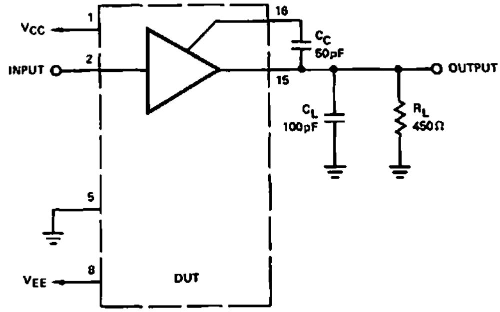
Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
t_r	Rise Time	Fig. 1, R_L = 450Ω, C_L = 500pF	C_C = 50pF		3.0		μs
			C_C = 0		120	300	ns
t_f	Fall Time	Fig. 1, R_L = 450Ω, C_L = 500pF	C_C = 50pF		3.0		μs
			C_C = 0		120	300	ns
Src	Slew Rate Coefficient	Fig. 1, R_L = 450Ω, C_L = 500pF			.06		μs/pF
t_{PDH}	Output Propagation Delay	Fig. 1, R_L = 450Ω, C_L = 500pF, C_C = 0			180	300	ns
t_{PDL}	Output Propagation Delay	Fig. 1, R_L = 450Ω, C_L = 500pF, C_C = 0			180	300	ns

Notes: 1. Typical limits are at V_{CC} = 5.0V, V_{EE} = −5.0V, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-423 where applicable.

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS FOR EIA RS-423 CONNECTION



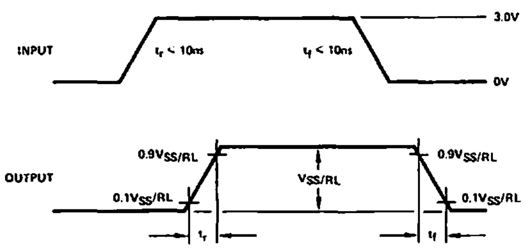
BLI-006



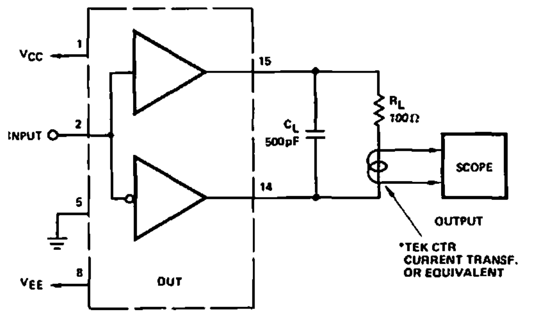
BLI-007

Figure 1. Rise Time Control for RS-423.

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUIT FOR RS-422 CONNECTION



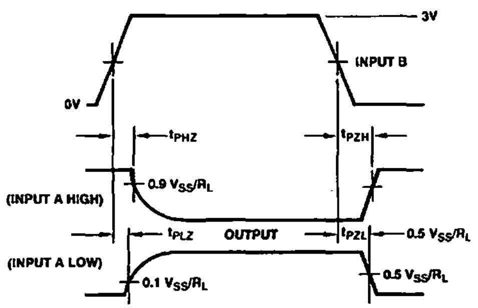
BLI-008



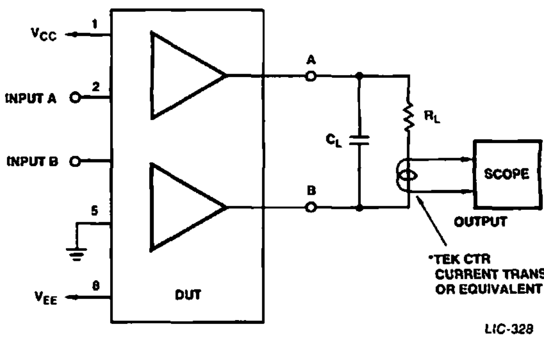
BLI-009

*Current probe is the easiest way to display a differential waveform.

Figure 2.



LIC-329



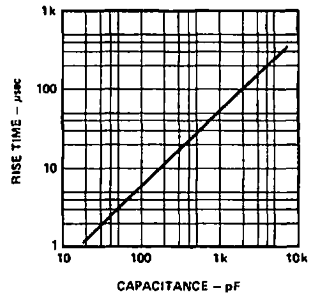
LIC-328

Figure 3. Three-State Delays.

Am26LS30 FUNCTION TABLE

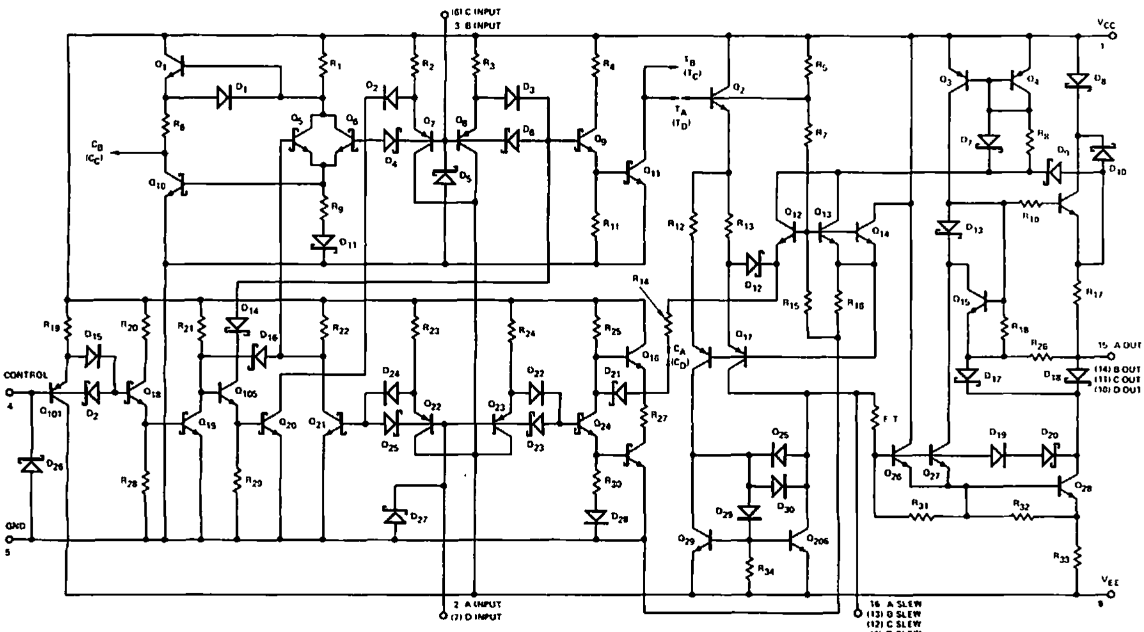
MODE	INPUTS		OUTPUTS	
	A(D)	B(C)	A(D)	B(C)
0	0	0	0	1
0	0	1	Z	Z
0	1	0	1	0
0	1	1	Z	Z
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

Slew Rate (Rise or Fall Time) Versus External Capacitor



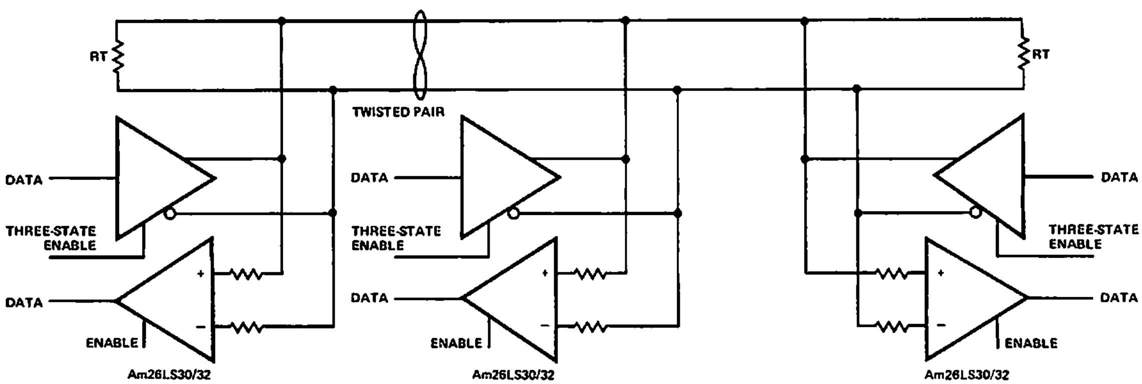
BLI-010

Am26LS30 EQUIVALENT CIRCUIT



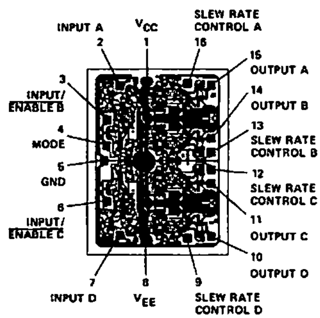
BLI-020

TYPICAL APPLICATION



BLI-032

Metallization and Pad Layout



DIE SIZE 0.070" X 0.094"

Am26LS31

Quad High Speed Differential Line Driver

DISTINCTIVE CHARACTERISTICS

- Output skew – 2.0ns typical
- Input to output delay – 12ns
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Outputs won't load line when V_{CC} = 0
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines
- Available in military and commercial temperature range
- Advanced low-power Schottky processing
- 100% reliability assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

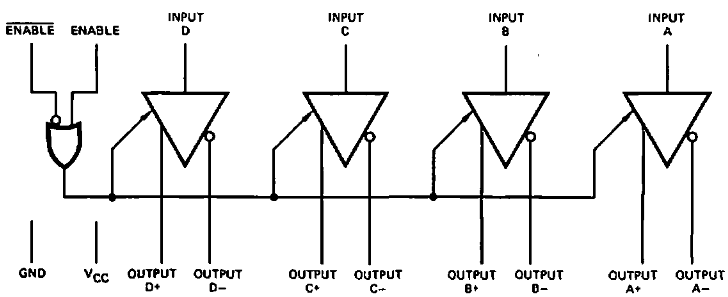
The Am26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The Am26LS31 meets all the requirements of EIA standard RS-422 and federal standard 1020. Is is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The Am26LS31 features 3-state outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

The Am26LS31 is constructed using advanced low-power Schottky processing.

4

LOGIC DIAGRAM

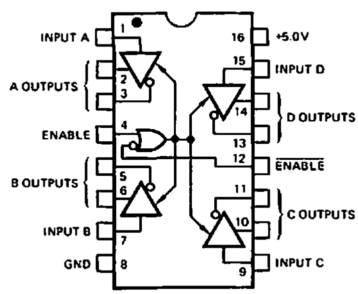


LIC-352

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	-55°C to +125°C	AM26LS31DM
Flat Pak	-55°C to +125°C	AM26LS31FM
Dice	-55°C to +125°C	AM26LS31XM
Hermetic DIP	0°C to +70°C	AM26LS31DC
Molded DIP	0°C to +70°C	AM26LS31PC
Dice	0°C to +70°C	AM26LS31XC

CONNECTION DIAGRAM
(Top View)



Note: Pin 1 is marked for orientation.

LIC-353

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage	7.0V
Input Voltage	7.0V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS over the operating temperature range

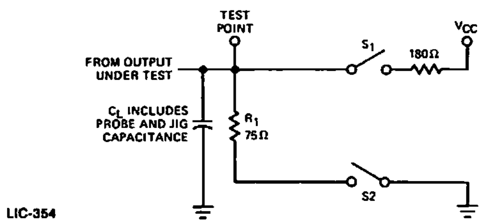
The following conditions apply unless otherwise specified:

Am26LS31XM (MIL) T_A = −55°C to +125°C V_{CC} = 5V ± 10%
Am26LS31XC (COM'L) T_A = 0°C to +70°C V_{CC} = 5V ± 5%

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −20mA		2.5	3.2		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 20mA			0.32	0.5	Volts
V_{IH}	Input HIGH Voltage	V_{CC} = Min.		2.0			Volts
V_{IL}	Input LOW Voltage	V_{CC} = Max.				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4V			−0.20	−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7V			0.5	20	μA
I_I	Input Reverse Current	V_{CC} = Max., V_{IN} = 7.0V			0.001	0.1	mA
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max.	V_O = 5.5V		0.5	20	μA
			V_O = 0.5V		0.5	−20	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = 18mA			−0.8	−1.5	Volts
I_{SC}	Output Short Circuit Current	V_{CC} = Max.		−30	−60	−150	mA
I_{CC}	Power Supply Current	V_{CC} = Max., all outputs disabled			60	80	mA
t_{PLH}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			12	20	ns
t_{PHL}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			12	20	ns
SKEW	Output to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			2.0	6.0	ns
t_{LZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10pF			23	35	ns
t_{HZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10pF			17	30	ns
t_{ZL}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			35	45	ns
t_{ZH}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			30	40	ns

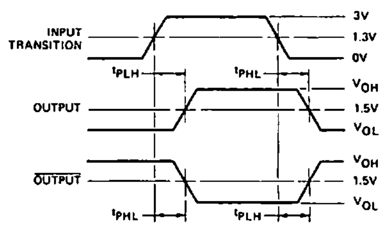
Notes: 1. All typical values are V_{CC} = 5.0V, T_A = 25°C.
2. C_L = 30pF, V_{IN} = 1.3V to V_{OUT} = 1.3V, V_{PULSE} = 0V to +3.0V, See Below.

AC LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



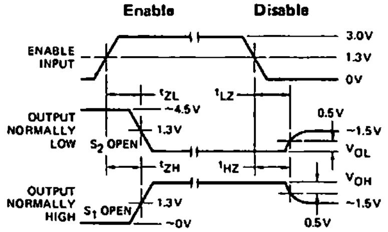
LIC-354

PROPAGATION DELAY (Notes 1 and 3)



LIC-355

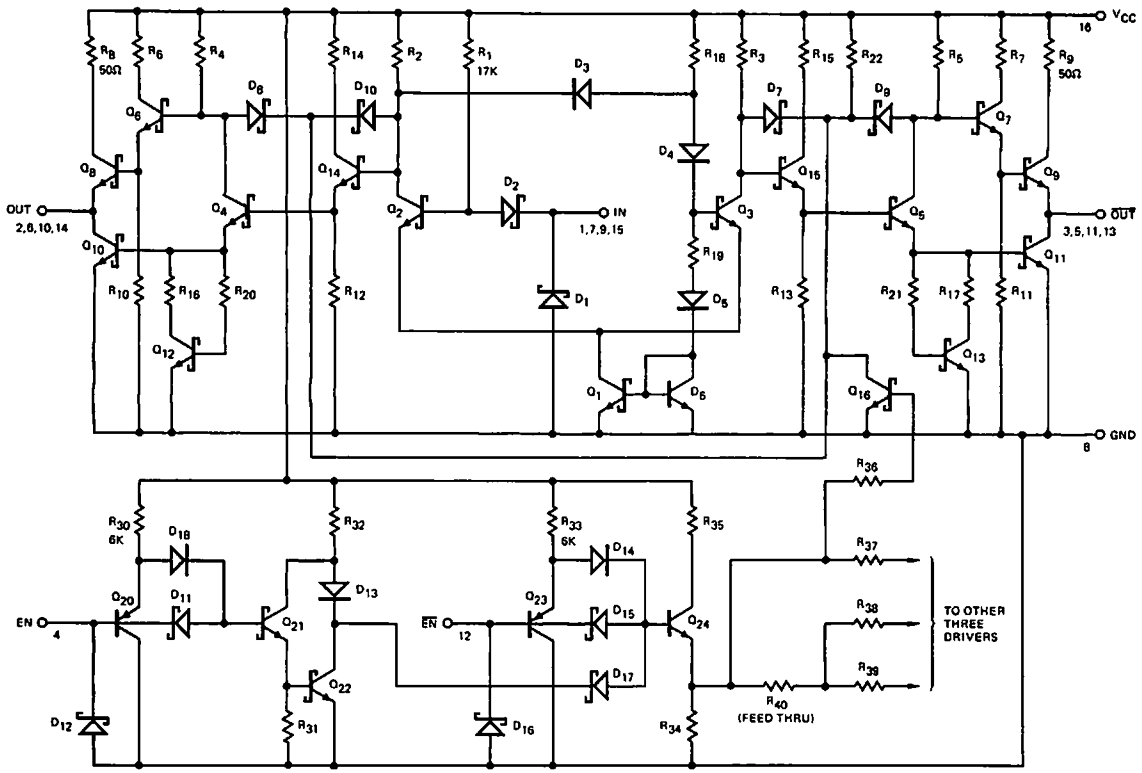
ENABLE AND DISABLE TIMES (Notes 2 and 3)



LIC-356

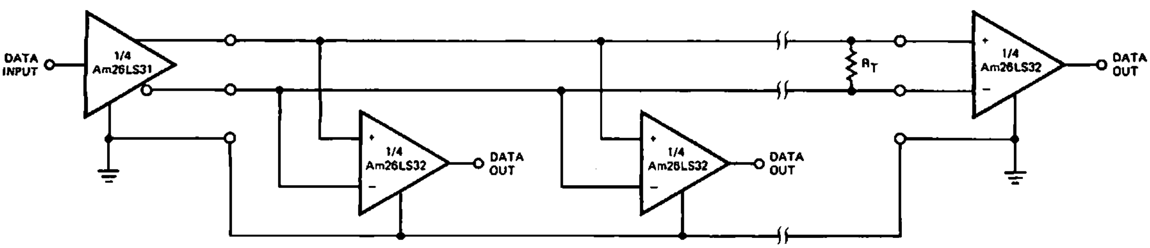
Notes: 1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 15ns; t_f ≤ 6.0ns.

EQUIVALENT CIRCUIT (1/4 Am26LS31)



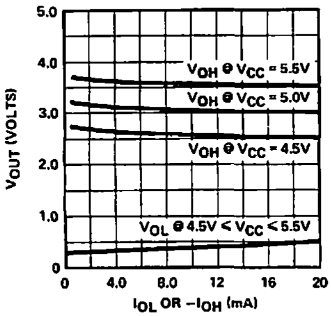
BLI-023

TYPICAL APPLICATION



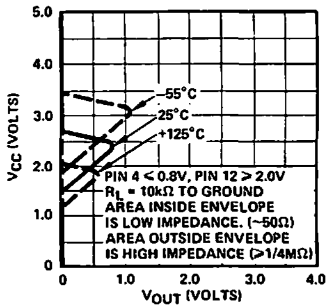
LIC-357

Guaranteed V_{OH} and V_{OL}
(T_A = −55°C to +125°C)



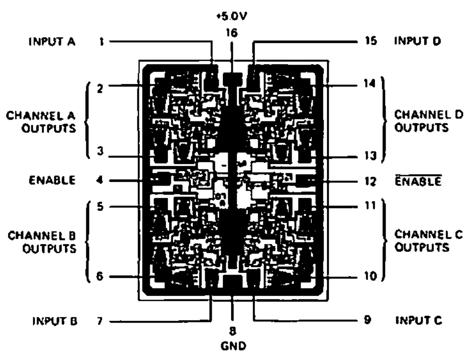
LIC-358

V_{OUT} Versus V_{CC}



LIC-359

Metallization and Pad Layout



DIE SIZE 0.067" X 0.084"

Am26LS32 • Am26LS33

Quad Differential Line Receivers

DISTINCTIVE CHARACTERISTICS

- Input voltage range of 15V (differential or common mode) on Am26LS33; 7V (differential or common mode) on Am26LS32
- ±0.2V sensitivity over the input voltage range on Am26LS32; ±0.5V sensitivity on Am26LS33
- The Am26LS32 meets all the requirements of RS-422 and RS-423
- 6k minimum input impedance
- 30mV input hysteresis
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Fail safe input-output relationship. Output always high when inputs are open.
- Three-state drive, with choice of complementary output enables, for receiving directly onto a data bus.
- Propagation delay 17ns typical
- Available in military and commercial temperature range
- Advanced low-power Schottky processing
- 100% reliability assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am26LS32 is a quad line receiver designed to meet the requirements of RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The Am26LS32 features an input sensitivity of 200mV over the input voltage range of ±7V.

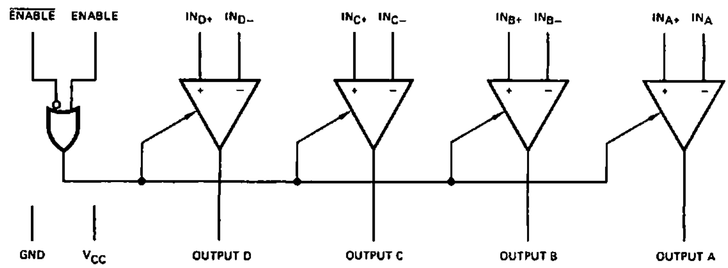
The Am26LS33 features an input sensitivity of 500mV over the input voltage range of ±15V.

The Am26LS32 and Am26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-state outputs with 8mA sink capability and incorporate a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 and Am26LS33 are constructed using Advanced Low-Power Schottky processing.

4

LOGIC DIAGRAM



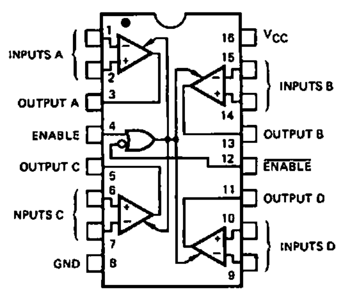
BLI-024

ORDERING INFORMATION

Package Type	Temperature Range	Am26LS32 Order Number	Am26LS33 Order Number
Hermetic DIP	−55°C to +125°C	AM26LS32DM	AM26LS33DM
Flat Pak	−55°C to +125°C	AM26LS32FM	AM26LS33FM
Dice	−55°C to +125°C	AM26LS32XM	AM26LS33XM
Hermetic DIP	0°C to +70°C	AM26LS32DC	AM26LS33DC
Molded DIP	0°C to +70°C	AM26LS32PC	AM26LS33PC
Dice	0°C to +70°C	AM26LS32XC	AM26LS33XC

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

LIC-360

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage	7.0V
Common Mode Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7.0V
Output Sink Current	50mA
Storage Temperature Range	−65°C to +165°C

ELECTRICAL CHARACTERISTICS Over the operating temperature range

The following conditions apply unless otherwise specified:

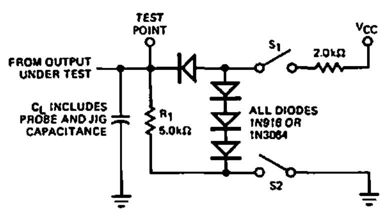
Am26LS32XM, Am26LS33XM (MIL) T_A = −55°C to +125°C V_{CC} = 5.0V ± 10%

Am26LS32XC, Am26LS33XC (COM'L) T_A = 0°C to +70°C V_{CC} = 5.0V ± 5%

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OL}$ or V_{OH}	Am26LS32, −7V ≤ V_{CM} ≤ +7V	0.2	0.06	0.2	Volts
			Am26LS33, −15V ≤ V_{CM} ≤ +15V	0.5	0.12	0.5	
R_{IN}	Input Resistance	−15V ≤ V_{CM} ≤ +15V (One input AC ground)		6.0k	8.5k		Ω
I_{IN}	Input Current (Under Test)	V_{IN} = +15V, Other Input −15V ≤ V_{IN} ≤ +15V				2.3	mA
I_{IN}	Input Current (Under Test)	V_{IN} = −15V, Other Input −15V ≤ V_{IN} ≤ +15V				−2.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., ΔV_{IN} = +1.0V	COM'L	2.7	3.4		Volts
		$V_{\overline{ENABLE}}$ = 0.8V, I_{OH} = −440µA	MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., ΔV_{IN} = −1.0V	I_{OL} = 4.0mA			0.4	Volts
		$V_{\overline{ENABLE}}$ = 0.8V	I_{OL} = 8.0mA			0.45	
V_{IL}	Enable LOW Voltage					0.8	Volts
V_{IH}	Enable HIGH Voltage			2.0			Volts
V_I	Enable Clamp Voltage	V_{CC} = Min., I_{IN} = −18mA				−1.5	Volts
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max.	V_O = 2.4V			20	µA
			V_O = 0.4V			−20	
I_{IL}	Enable LOW Current	V_{IN} = 0.4V			−0.2	−0.36	mA
I_{IH}	Enable HIGH Current	V_{IN} = 2.7V			0.5	20	µA
I_I	Enable Input High Current	V_{IN} = 5.5V			1	100	µA
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max., ΔV_{IN} = +1.0V		−15	−50	−85	mA
I_{CC}	Power Supply Current	V_{CC} = Max., All V_{IN} = GND, Outputs Disabled			52	70	mA
V_{HYST}	Input Hysteresis	T_A = 25°C, V_{CC} = 5.0V, V_{CM} = 0V			30		mV
t_{PLH}	Input to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF, see test cond. below			17	25	ns
t_{PHL}	Input to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF, see test cond. below			17	25	ns
t_{LZ}	Enable to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 5pF, see test cond. below			20	30	ns
t_{HZ}	Enable to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 5pF, see test cond. below			15	22	ns
t_{ZL}	Enable to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF, see test cond. below			15	22	ns
t_{ZH}	Enable to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF, see test cond. below			15	22	ns

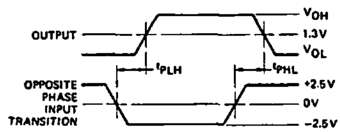
Note: 1. All typical values are V_{CC} = 5.0V, T_A = 25°C.

LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



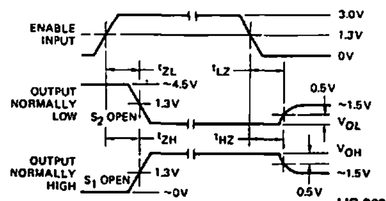
LIC-361

PROPAGATION DELAY (Notes 1 and 3)



LIC-362

ENABLE AND DISABLE TIMES (Notes 2 and 3)

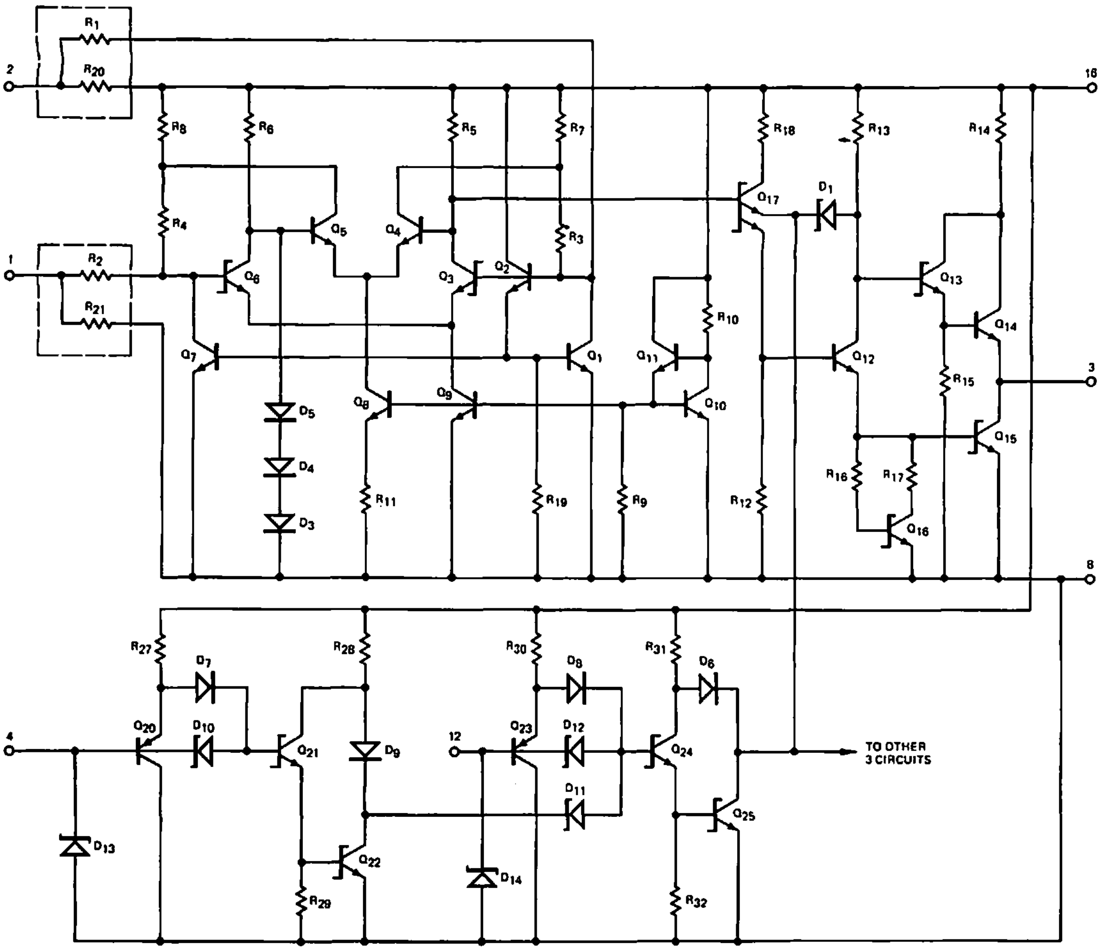


LIC-363

Notes:

1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 15ns; t_f ≤ 6.0ns.

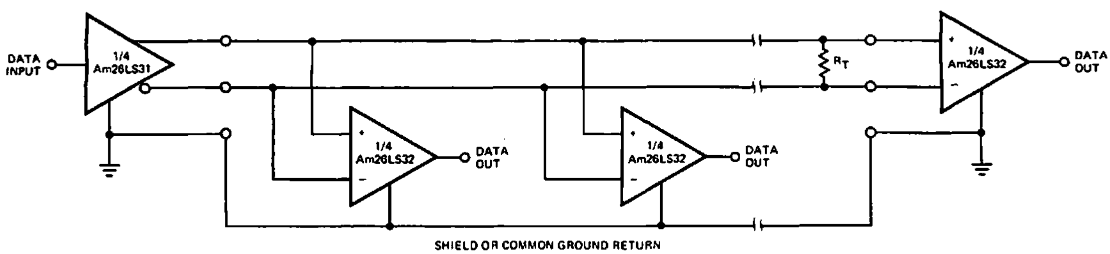
EQUIVALENT CIRCUIT (1/4 Am26LS32 OR Am26LS33)



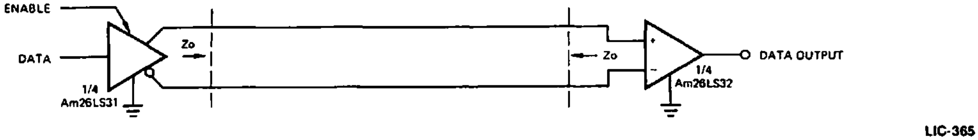
Note: R_3 and R_4 value for Am26LS32 is 2 times Am26LS33 value.

BLI-025

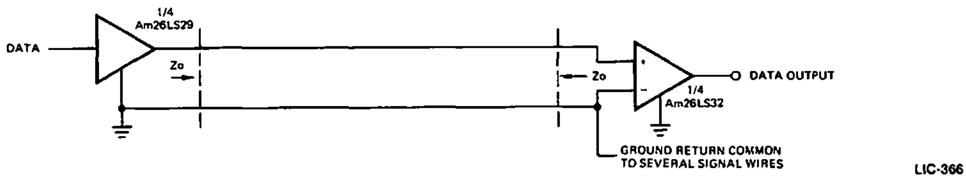
TYPICAL APPLICATION



LIC-364



Two Wire Balanced System.



Single Wire With Common Ground Unbalanced System.

LINE TERMINATION

It is important in a digital communication system to have the minimum amount of noise generated by undesired reflections at the driver and receiver. There are numerous ways of matching to the line. The line can be matched at the driver, at the receiver or both, each method has advantages and disadvantages. Generally for any but the longest lines it is sufficient to match at one place, and only when there are discontinuities in the line, party line operation, or lack of a reasonable match at the opposite end of the line is the extra hardware of matching at both ends justified. The majority of transmission lines have fairly low characteristic impedances (in the range of 50 to 200 ohms) and the currents involved for a reasonable voltage swing are quite large. It is more difficult to couple noise into this low impedance, but it is also more difficult to drive, and line drivers must have the ability to supply large currents.

Various matching techniques that can be employed are shown in Figure 1. These impedance charts are useful in showing what happens to wave fronts traveling down a line, when the line delay is longer than the wave front transition. The DC input characteristic of the receiver, including any external components, is plotted on the V-I graph together with the output characteristic of the driver, including any external components used at the driving end. There are always quiescent points – points where the driver and receiver characteristics cross. These points represent the DC voltage/current conditions, which must eventually be satisfied. To determine the effect of switching from one quiescent point to the other, a line with a slope equal to the characteristic impedance of the transmission line is plotted, starting at the initial quiescent point and ending at the applicable output impedance characteristic. The point of intersection gives the voltage and current at the output of the driver (and the input of the transmission line immediately after the driver switched states). From this point a line having an equal but opposite slope is drawn to the input characteristic and, at the intersection shows the voltage/current conditions of the wave front at the input of the receiver. This procedure is repeated to the output characteristic and so on at each intersection of the characteristic, the voltage/current relationship for a particular reflection is given. The resulting time/voltage relationships for the traveling wavefront at the two ends of the transmission line are shown alongside.

From the graphs several important features can be seen. If the line is not matched at either end considerable transient voltage swings can occur. In fact if the input and output characteristics are at right angles to one another, the reflections continue for an infinite time if the line is assumed to have zero loss. Most lines have extremely low losses, and, therefore, a very undesirable situation exists if the line is not matched at either end.

If the line is matched at the receiver, a voltage wave of constant amplitude travels down the line and is absorbed at the termination. Note whether the line is terminated to ground or to the power supply the system consumes DC power, either in the HIGH logic level or in the LOW logic level. In order to reduce the power dissipation, a blocking capacitor can be used in series with the receiver termination. The capacitor can be chosen to look like a short circuit to the voltage wavefront but stop DC (current) flow. Since the capacitor must be charged and discharged through the line, the data rate is reduced, when this technique is employed.

If the line is matched with a series resistor at the driver, then the line input initially rises to one half the final voltage. This wave front travels down the line and is reflected at the receiver. When the reflection reaches the driver the voltage at the driver rises to its final amplitude. The receiver, however, sees one transition from the initial to the final amplitude. When the driver switches from HIGH to LOW a similar situation occurs, in which the input of the line sees at first a step to one half the final value and, two line delays later, the final LOW condition. This back matching mode of operation consumes no DC power if the input impedance of the receiver is infinite. The advantage of the method is that if the input impedance of the receiver is high, very little power is dissipated and current only flows during the transition time, which is twice the line delay time. If back matching is used in a balanced system the terminating series resistance must be divided into two equal resistances with resistors inserted in series with each wire in order to maintain a balanced system.

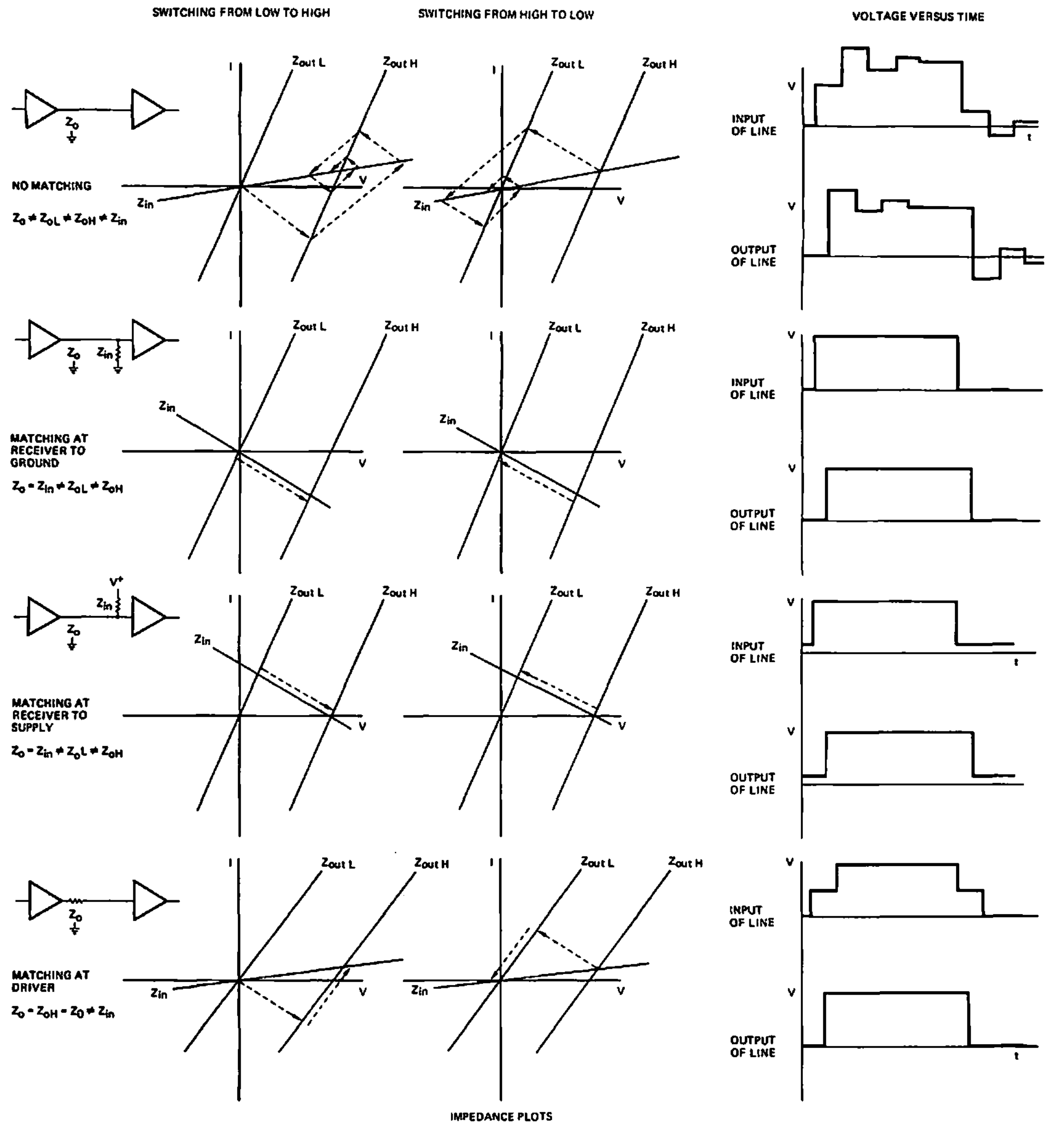
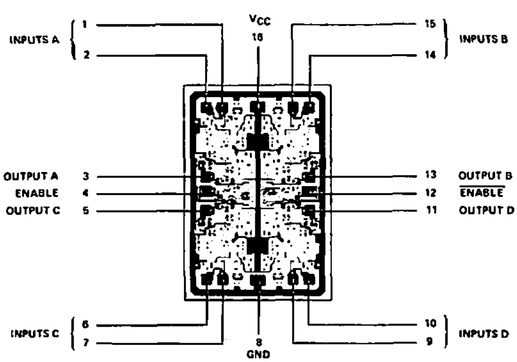


Figure 1. Line Matching Methods

LIC-367

Metallization and Pad Layout



DIE SIZE
0.087" X 0.059"

USE OF THE Am26LS29, 30, 31 and 32 QUAD DRIVER/RECEIVER FAMILY IN EIA RS-422 AND 423 APPLICATIONS

By David A. Laws and Roy J. Levy

INTRODUCTION

Today's high-performance data processing systems demand significantly faster data communications rates than are possible with the EIA RS-232 specifications in use for the past ten years.

Two new standards prepared by the Electronic Industries Association address this need. EIA RS-423 is an unbalanced, bipolar voltage specification designed to interface with RS-232C, while greatly enhancing its operation. It permits the communication of digital information over distances of up to 2000 feet and at data rates of up to 300 Kilobaud. EIA RS-422 is a balanced voltage digital interface for communicaton of digital data over distances of 4000 feet or data rates of up to 10 megabaud.

Advanced Micro Devices has developed a family of monolithic Low-power Schottky quad line drivers and receivers to meet the requirements of these specifications.

The Am26LS29 and 30 line drivers and the Am26LS32 receiver meet all requirements of RS-423 while the Am26LS31 differential line driver and the Am26LS32 receiver meet the requirements of RS-422.

A second receiver element, the Am26LS33 is available for use in high common mode noise environments, exceeding the common mode voltage requirements of RS-422 and RS-423.

This application note reviews the use of these devices in implementing the new standards. Emphasis is given to the EIA RS-422 balanced interface.

EIA STANDARD SPECIFICATIONS

Two basic forms of operation are available for transmission of digital data over interconnecting lines. These are the single ended and differential techniques.

The single-ended form uses a single conductor to carry the signal with the voltage referenced to a single return conductor. This may also be the common return for other signal conductors. Figure 1a.

The single-ended form is the simplest way to send data as it requires only one signal line per circuit. This simplicity, however, is often offset by the inability of this form to allow discrimination between a valid signal produced by the driver, and the sum of the driver signal plus externally induced noise signals.

A solution to some of the problems inherent in the single-ended form of operation is offered by the differential form of operation. Figure 1b. This consists of a differential driver (essentially two single-ended drivers with one driver always producing the complementary output signal level to the other driver), a twisted pair transmission line and a differential line receiver. The driver signal appears as a differential voltage to the line receiver, while the noise signals appear as a common mode signal. The two signals, therefore, can be discriminated by a line receiver with a sufficient common mode voltage operating range.

The Electronic Industries Association, EIA, has defined a number of specifications standardizing the interface between data terminal equipment and data circuit terminating equipment based on both single-ended and differential operation.

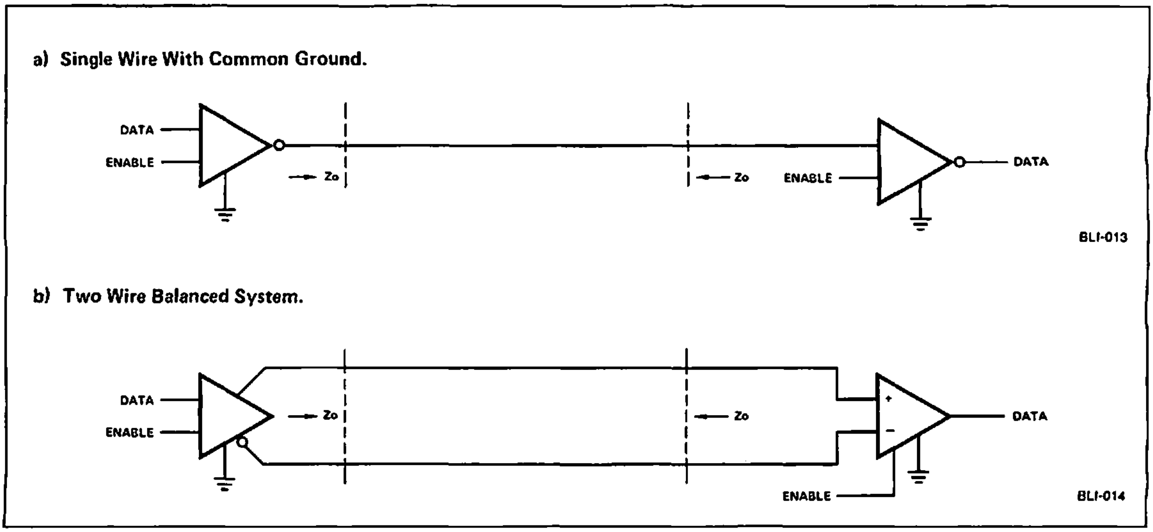


Figure 1. Data Communication Techniques.

The most widely used standard for interfacing between data terminal equipment and data communications equipment today, is EIA RS-232C, issued in August 1969. The RS-232C electrical interface is a single-ended, bipolar-voltage, unterminated circuit. This specification is for serial binary data interchange over short distances (up to 50 feet) at low rates (up to 20 Kilobaud). It is a protocol standard as well as an electrical standard, specifying hand shaking signals and functions between terminal and the communications equipment. As already noted, single-ended circuits are susceptible to all forms of electromagnetic interference. Noise and cross talk susceptibility are proportional to length and bandwidth. RS-232C places restrictions on both. It limits slew rate of the drivers (30V/μs) to control radiated emission on neighboring circuits and allows bandwidth limiting on the receivers to reduce susceptibility to cross talk. The length and slew rate limits can adequately control reflections on unterminated lines, and the length and bandwidth limits are more than adequate to reduce susceptibility to noise.

Like EIA RS-232C, the new EIA RS-423 is also a single-ended, bipolar-voltage unterminated circuit. It extends the distance and data rate capabilities of this technique to distances of up to 4000 feet at data rates of 3000 baud, or at higher rates of up to 300 Kilobaud over a maximum distance of 40 feet.

EIA RS-422 is a differential, balanced voltage interface capable of significantly higher data rates over longer distances. It can accommodate rates of 100 Kilobaud over a distance of 4000 feet or rates of up to 10 megabaud. These performance improvements stem from the advantages of a balanced configuration which is isolated from ground noise currents. It is also immune to fluctuating voltage potentials between system ground references and to common mode electromagnetic interference. Figure 2 compares the driver output waveforms for the three EIA standard configurations, while Table I compares the key characteristics required by drivers and receivers intended for these applications. Since RS-232C has been in use for many years, RS-422 and 423 parameter values have been selected to facilitate an orderly transition from existing designs to new equipment.

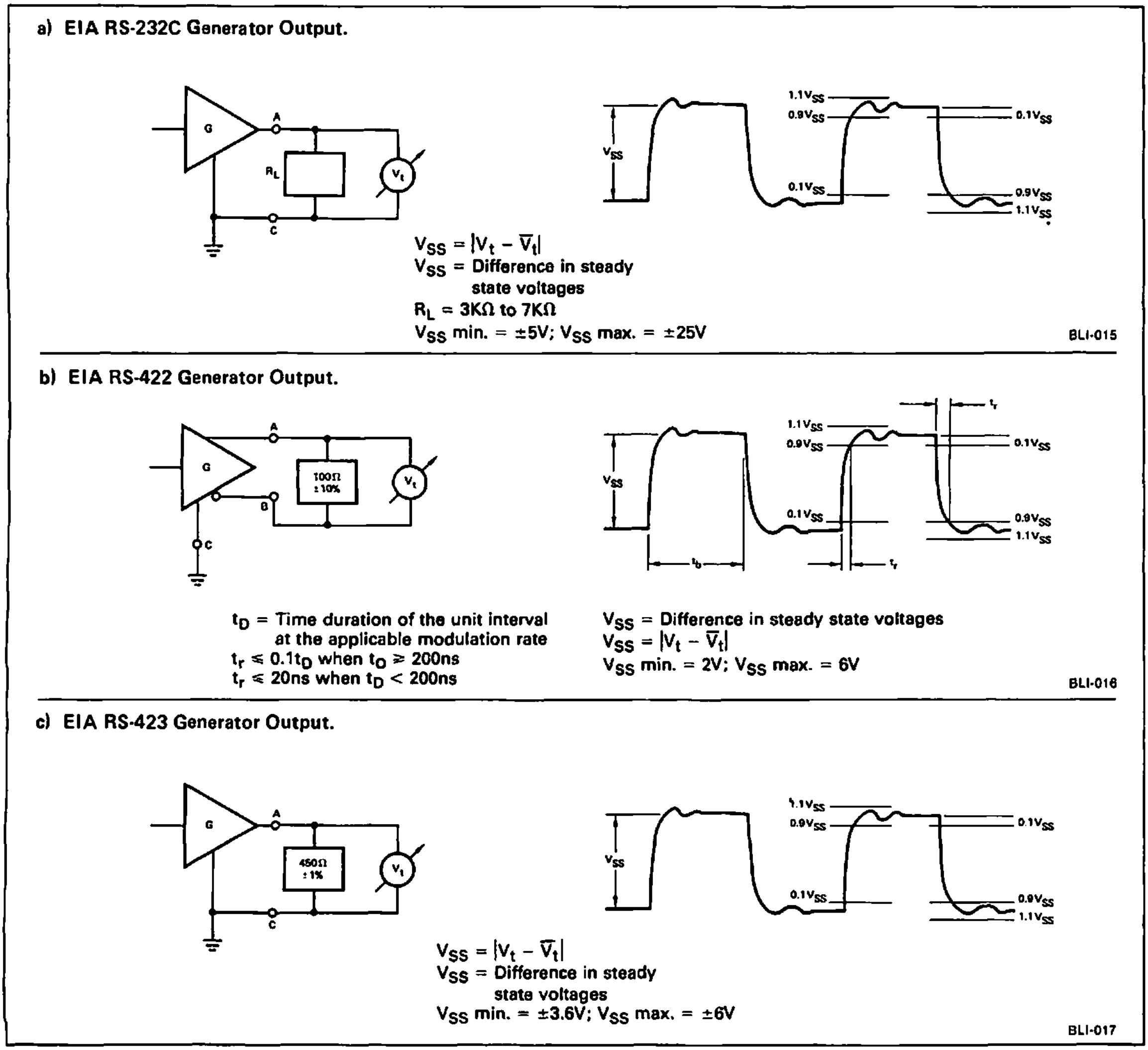


Figure 2. Driver Output Waveforms.

TABLE I
KEY PARAMETERS OF EIA SPECIFICATIONS

Characteristics	EIA RS-232C	EIA RS-423	EIA RS-422	Units
Form of Operation	Single Ended	Single Ended	Differential	
Max. cable length	50	2000	4000	Feet
Max. data rate	20K	300K	10M	Baud
Driver output voltage, open circuit*	±25	±6	6 volts between outputs	Volts (Max.)
Driver output voltage, Loaded output*	±5 to ±15	±3.6	2 volts between outputs	Volts (Min.)
Driver output resistance power off	Ro = 300Ω	100μA between −6 to +6V	100μA between +6 and −.25V	Min.
Driver output short circuit current I_{SC}	±500	±150	±150	mA (Max.)
Driver output slew rate	30 V/μsec Max.	Slew rate must be controlled based upon cable length and modulation rate	No control necessary	
Receiver input resistance R_{in}	3K to 7K	≥4K	≥4K	Ω
Receiver input thresholds	−3 to +3	−0.2 to +0.2	−0.2 to +0.2	Volts (Max.)
Receiver input voltage	−25 to +25	−12 to +12	−12 to +12	Volts (Max.)

*± indicates polarity switched output.

INTEGRATED CIRCUIT CHARACTERISTICS

Most semiconductor manufacturers offer integrated circuits designed to satisfy the old RS-232C standard. A number of them have designs in progress to meet the new EIA specifications. Products available from Advanced Micro Devices to meet these needs are shown in Table II.

The Am26LS29, 30, 31 and 32 are a family of quad drivers and receivers designed specifically to meet the new EIA standards. These products utilize Low-Power Schottky technology to incorporate four drivers or four receivers, together with control logic, in the standard 16-pin package outlines.

The Am26LS29/30 and the Am26LS32 are driver and receiver pairs designed to implement the single-ended EIA RS-423 standard. The Am26LS31 is a differential line driver designed for use with the Am26LS32 receiver in a differential mode to meet EIA RS-422.

Am26LS29 AND Am26LS30 QUAD RS-423 LINE DRIVERS

The Am26LS29 and 30 consist of four single-ended line drivers designed to meet or exceed the requirements of RS-423. The buffered driver outputs are provided with sufficient source and sink current capability to drive 50 ohm to a virtual ground transmission line and high capacitive loads. The Am26LS29 has a three-state output control while the Am26LS30 has a Mode Control input that allows it to operate as a dual RS-422 driver (with suitable power supply changes), Figure 3.

Each of the four driver inputs, as well as the $\overline{\text{Enable}}$/Mode *Control* input is a PNP Low-Power Schottky input for reduced input loading, one-half the normal fan-in. Since there are two inverters from each input to output, the driver is non-inverting. When operating in the RS-423 mode, the Am26LS29 and 30 require both +5V and −5V nominal value power supplies. This allows the outputs to swing symmetrically about ground – producing a true bipolar output. The Mode Control (Pin 4) of the Am26LS30 should be HI or tied to

TABLE II
ADVANCED MICRO DEVICES'
EIA COMPATIBLE DEVICES

EIA Standard	Drivers	Receivers
RS-232C	Am1488 Quad Driver	Am1489, 1489A Quad Receivers with response control pin
	Am9616 Triple Driver with logic control	Am9617 Triple Receiver with optional hysteresis
	Am2616 Quad Driver also specified for CCITT V.24 and MIL-188C	Am2617 Quad Receiver specified over MIL range
RS-422	Am26LS31 Quad Differential with three-state control gating	Am26LS32 Quad Differential Driver single-ended Receiver
RS-423	Am26LS29 Quad Driver with three-state output	Am26LS32 Quad single-ended/ Differential Receiver
	Am26LS30 Quad Driver with slew rate control	

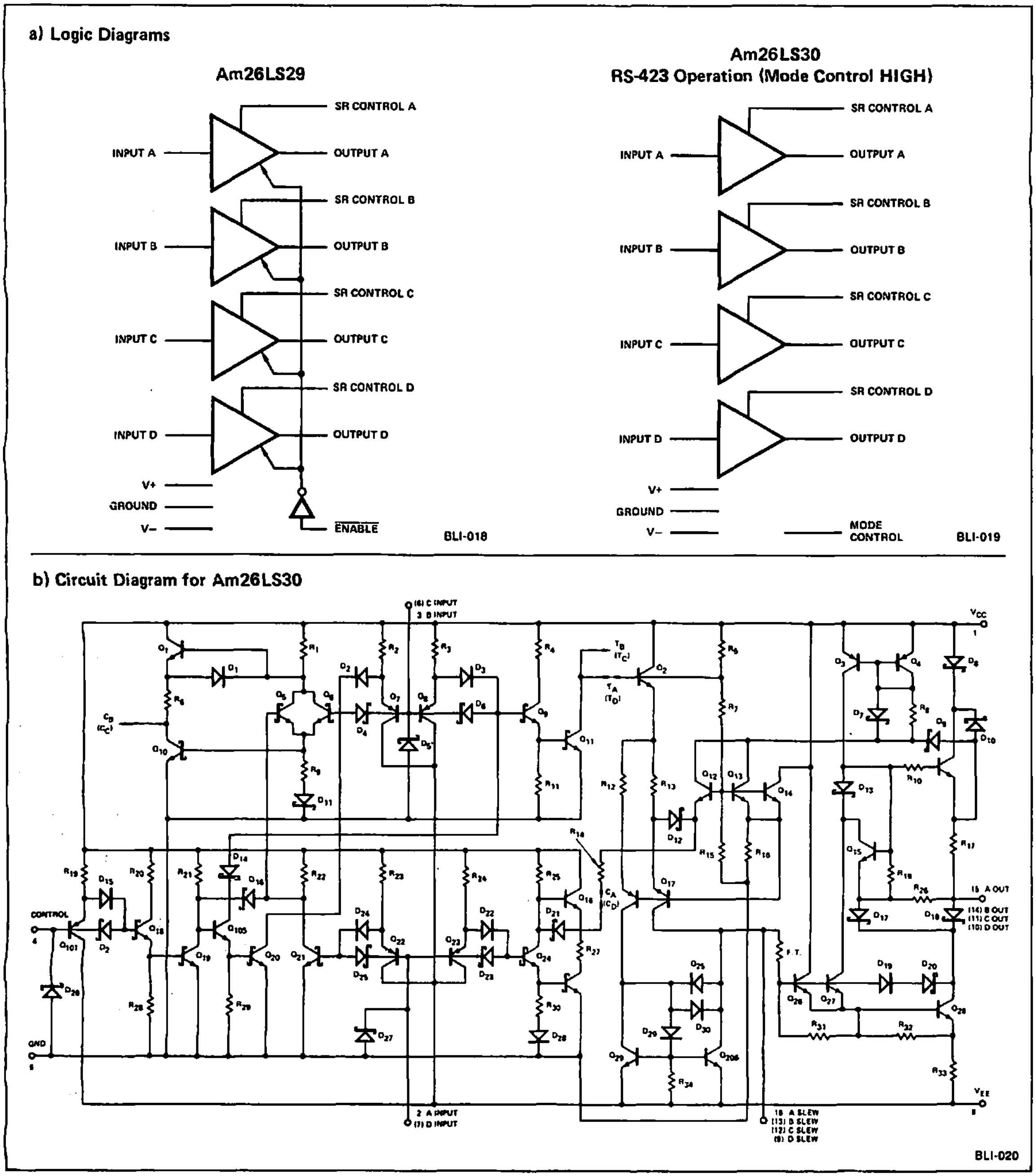


Figure 3. Am26LS29 and Am26LS30 Drivers.

V_{CC}. Each output is designed to drive the RS-423 load of 50 ohms with an output voltage equal or greater than +3.6 volts in the HI state and −3.6 volts in the LO state. Each output is current limited to 150mA max. in either logic state. A Slew Rate control pin is brought out separately for each output to allow output ramp rate (rise and fall time) control. This provides suppression of near end cross talk to other receivers in the cable. Connecting a capacitor from this node to that driver's respective output will produce a ramp (10% to 90%) of 50ns typical for each picofarad of capacitance in that capacitor. RS-423 establishes recommended ramp rates versus length of line driven and modulation rate, Figure 4.

The Am26LS30 can be used at low data rates as a dual EIA RS-422 driver with three-state outputs by connecting the V_{EE} supply and the mode control input to ground.

Am26LS31 QUAD RS-422 DRIVER

The Am26LS31 is a quad differential line driver designed to meet the RS-422 specification while operating with a single +5 volt supply. A common enable and disable function controls all four drivers, Figure 5. The driver features high speed, de-skewed differential outputs with typical propagation delays of 12ns and residual skew of 2ns. Both differential line outputs are designed for three-state operation to allow two-way half duplex and multiplex, data bus applications.

Table III is a summary of the essential requirements of the RS-422 standard. Section A describes the key characteristics satisfied by the Am26LS31 driver.

The balanced differential line driver consists of two halves, each of which is similar to a Low-power Schottky TTL gate with equal source and sink current capability. The two halves are emitter coupled in a differential input configuration. One side of the input circuit is tied to a fixed TTL bias threshold and the other side is tied to a sink diode in normal DTL/TTL fashion. This configuration offers complementary outputs with very low skew, dependent only upon component matching, a necessity to meet RS-422.

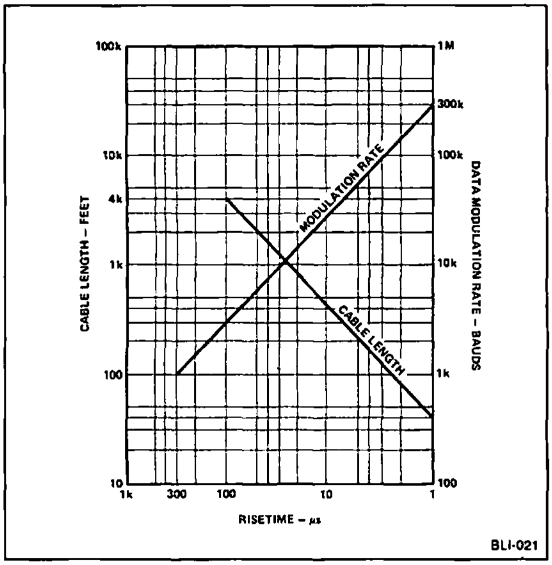


Figure 4. Data Modulation Rate or Cable Length Versus Risetime for EIA RS-423.

The circuit diagram of the driver is shown in Figure 6. The emitter-coupled input circuit is formed by Q2 and Q3, which are biased by a current source. This source is a current mirror, formed by Q1 which supplies the current, and D6 which is diode connected transistor matched to Q1. The fixed bias for Q3, formed by D5 and D6, is $2V_{BE}$. A $2V_{BE}$ bias, less the D2 Schottky diode drop, provides the normal Low-power Schottky TTL threshold, $V_{IL} \doteq 0.7V$. R19 provides a boost to 0.8V for a full 400mV TTL noise margin. The differential outputs of the emitter coupled stage, A and $\bar{A}$, drive emitter followers Q14 and Q15, which provide the required speed and matching characteristics. The emitter followers, drive phase splitters Q4 and Q5, which in turn drive totem-pole outputs. The outputs at the line interface are of standard Low-power Schottky TTL configuration, except that circuit values are modified to provide high sourcing capability. The outputs are designed to source or sink 20mA each, so that they can generate a voltage of at least 2.0V across a 100 ohm load, as required by RS-422. Additional circuitry has been included to make the line outputs three-state for two-way bus applications. The Am26LS31 meets the RS-422 requirement that the driver not load the line in the powered down condition ($I_X \leq 100\mu A$) or if the power supply to that device should fail.

Am26LS32 QUAD RS-422 AND 423 RECEIVER

The Am26LS32 is a quad line receiver which, operating from a single 5 volt supply, can be used in either differential or single-ended modes to satisfy RS-422 and 423 applications respectively. A complementary enable and disable feature, similar to that on the driver, controls all four receivers, Figure 7. The device's three-state outputs, which can sink 8mA, incorporate a fail-safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 meets the receiver input specification of Table III, a 200mV threshold sensitivity with common mode rejection exceeding the supply line potentials, (greater than 7 volts). The same design feature of the input circuit which provides the common mode rejection also insures excellent power supply ripple rejection, which is important when switching the high currents involved in a system's interfaces. Furthermore, unlike operational amplifiers, where the DC common mode and power supply rejection ratios roll off with open loop gain, the full rejection capability of this line receiver is maintained at high frequencies. The receiver hysteresis of typically 30mV, provides differential noise immunity. Signals received on long lines can have slow transition times, and without hysteresis, a small amount of noise around the switching threshold can cause errors in the receiver output.

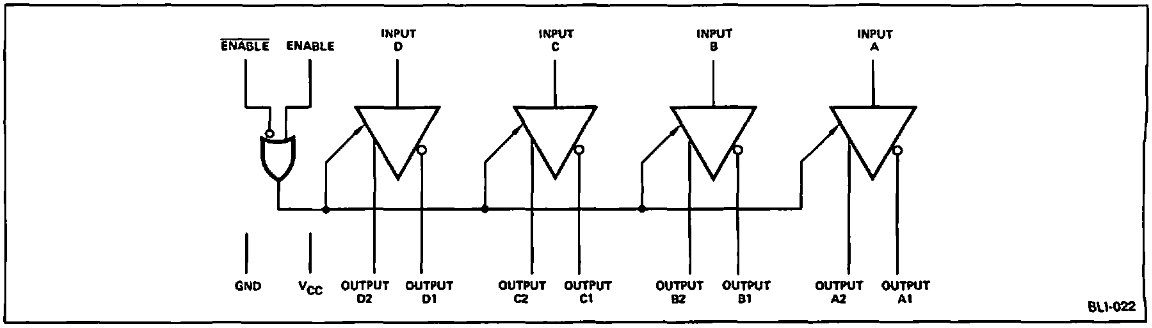


Figure 5. Am26LS31 Logic Diagram.

TABLE III
SUMMARY OF EIA RS-422 STANDARD FOR A BALANCED DIFFERENTIAL INTERFACE

A. Line Driver

Open Circuit Voltage (either logic state)	
Differential	$\lvert V_{do} \rvert \leq 6.0V$
Common Mode	$\lvert V_{cmo} \rvert \leq 3.0V$
Differential Output Voltage (across 100 ohm load)	
Either logic state	$\lvert V_d \rvert \geq \max(0.5V_{do}, 2.0V)$
Output Impedance	
Either logic state	$R_G \leq 100$ ohms
Mark-Space Level Symmetry (across 100 ohm load)	
Differential	$\lvert V_{dS} \rvert - \lvert V_{dM} \rvert \leq 0.4V$
Common Mode	$\lvert V_{cmS} \rvert - \lvert V_{cmM} \rvert \leq 0.4V$
Output Short Circuit Current (to ground)	
Either Output	$\lvert I_{SC} \rvert \leq 150mA$
Output Leakage Current (power off)	
Voltage Range	$-0.25V \leq V_x \leq +6.0V$
Either Output at V_x	$\lvert I_X \rvert \leq 100\mu A$
Rise and Fall Times (across 100 ohm load)	
T = Baud Interval	$(t_r, t_f) \leq \max(0.1T, 20ns)$
Ringing (across 100 ohm load)	
Definitions	
$V_{dSS} = V_d$ (steady state)	
$V_{SS} = V_{dS} - V_{dM}$ (steady state)	
Limits (either logic state)	
Percentage	$\lvert V_d - V_{dSS} \rvert \leq 0.1V_{SS}$
Absolute	$2.0V \leq \lvert V_d \rvert \leq 6.0V$

B. Line Receiver

Signal Voltage Range	
Differential	$\lvert V_d \rvert \leq 6.0V$
Common Mode	$\lvert V_{cM} \rvert \leq 7.0V$
Single-Ended Input Current (power ON or OFF)	
Either Input at V_x	$\lvert V_x \rvert = 10V$
Other Input Grounded	$\lvert I_V \rvert \leq 3.25mA$
Single-Ended Input Bias Voltage (other input grounded)	
Either Input Open Circuit	$\lvert V_B \rvert \leq 3.0V$
Single-Ended Input Impedance (other input grounded)	
Either Input	$R_L \geq 4000$ ohms
Differential Threshold Sensitivity	
Common Mode Voltage Range	$\lvert V_{cm} \rvert \leq 7.0V$
Either Logic State	$\lvert V_T \rvert \leq 200mV$
Absolute Maximum Input Voltage	
Differential	$\lvert V_d \rvert \leq 12V$
Single-Ended	$\lvert V_x \rvert \leq 10V$
Input Balance (threshold shift)	
Common Mode Voltage Range	$\lvert V_{cm} \rvert \leq 7.0V$
Differential Threshold (500 ohms in series with each input)	
Either Logic State	$\lvert V_t \rvert \leq 400mV$
Termination (optional)	
Total Load Resistance (differential)	$R_T > 90$ ohms

Multiple Receivers (bus applications)

Up to 10 receivers allowed. Differential threshold sensitivity of 200mV must be maintained.

Hysteresis (optional)

As required for applications with slow rise/fall time at receiver, to control oscillations.

Fail Safe (optional)

As required by application to provide a steady MARK or SPACE condition under open connector or driver power OFF condition.

C. Interconnecting Cable

Type	
Twisted Pair Wire or Flat Cable Conductor Pair	
Conductor Size	
Copper Wire (solid or stranded)	24 AWG or larger
Other (per conductor)	$R \leq 30$ ohms/1000 ft.
Capacitance	
Mutual Pair	$C \leq 20pF/ft.$
Stray	$C \leq 40pF/ft.$
Pair-to-Pair Cross Talk (balanced)	
Attenuation at 150KHz	$A \geq 40dB$

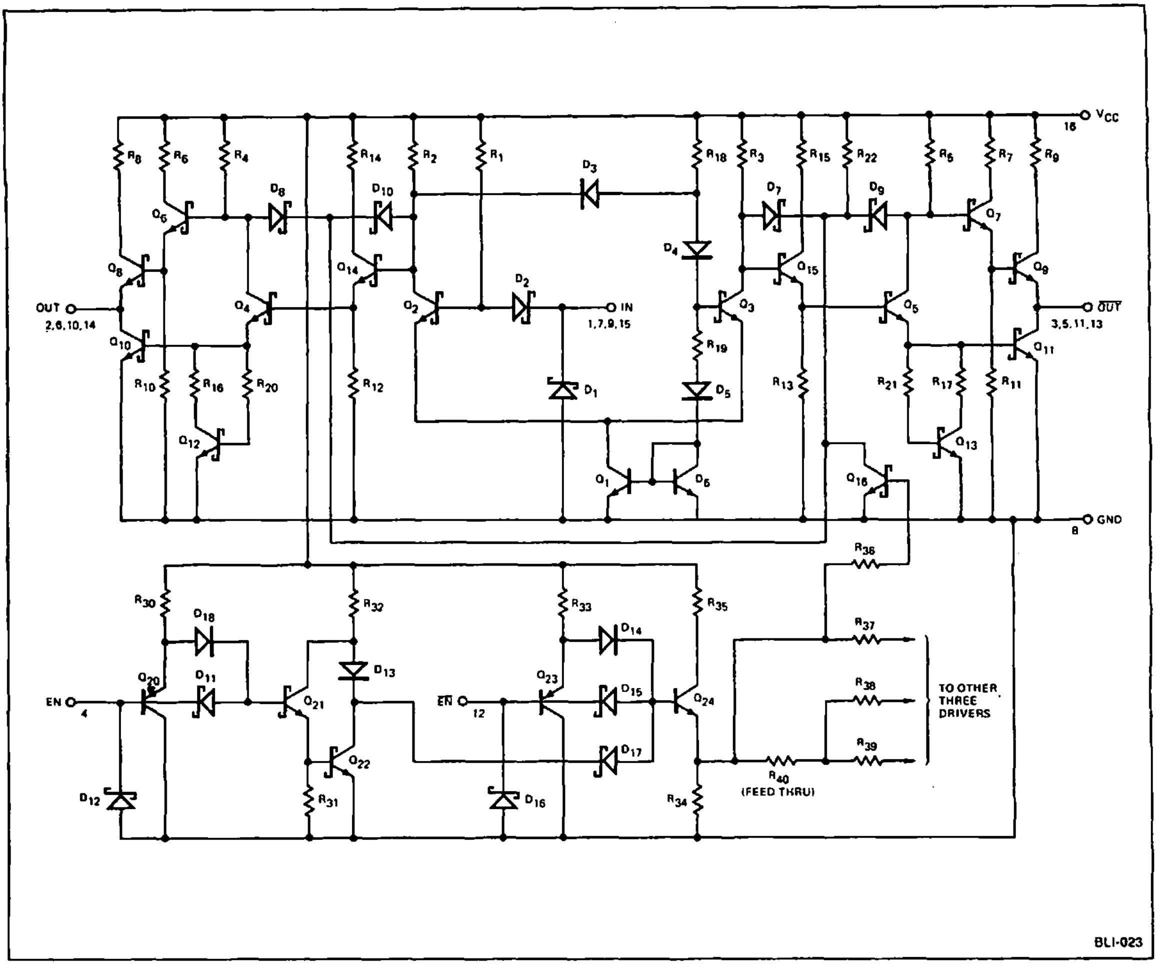


Figure 6. Am26LS31 Circuit Diagram (Only one driver shown).

The balanced differential line receiver is a three-stage circuit. The input stage consists of a low-impedance differential current amplifier with series resistor inputs to convert line signal voltage to current and provide a moderate input impedance. The input resistors provide an impedance greater than 6K on each input, power on or power off, which exceeds the requirements of RS-422 and RS-423. This is one advantage of the current amplifier input circuit. Another advantage is that is can operate with immunity to common mode voltages above V_{CC} and below ground. The differential threshold sensitivity of this circuit is 200mV, as required by RS-422. The second stage is a differential voltage amplifier, which interfaces to the single-ended output stage through an emitter follower. The output stage is a standard Low-power Schottky TTL totem-pole output with three-state capability.

The full circuit is shown in Figure 8. Resistors R_{20} and R_{21}, which connect the non-inverting input to V_{CC} and the inverting input to ground, provide the fail-safe feature, which guarantees a HIGH logic state for the receiver output when there is no signal on the line. The differential voltage amplifier in the second stage is formed by Q6 and Q3 which are biased by current source Q9. The hysteresis in the receiver switching characteristic is provided by Q4 and Q5, a differential pair biased by current source Q6, whose collectors are connected in positive feedback to the input pull-up circuits. A small amount of current is switched by Q4 and Q5, which must be overcome by the different voltage signal, resulting in the hysteresis. The output stage is driven from one side of the differential second stage by emitter follower Q17, which is a multiple emitter transistor. the second emitter is the control point for the three-state output.Q17 drives the phase splitter Q12, which in turn drives the three-state totempole output. The remainder of the circuit is the output enable control logic. This three-state capability on the receiver TTL side of the interface is a useful feature for modularizing two-way bus design.

A mask option of the input resistors (R_1, R_2, R_{20} and R_{21}) modifies the receiver characteristics to improve operation in high common mode noise environments. This device, known as the Am26LS33, has these resistors at twice the value of the Am26LS32. An input differential or common mode voltage range of ±15 volts is achieved at the expense of a minor decrease of input threshold sensitivity, to ±500mV from ±200mV.

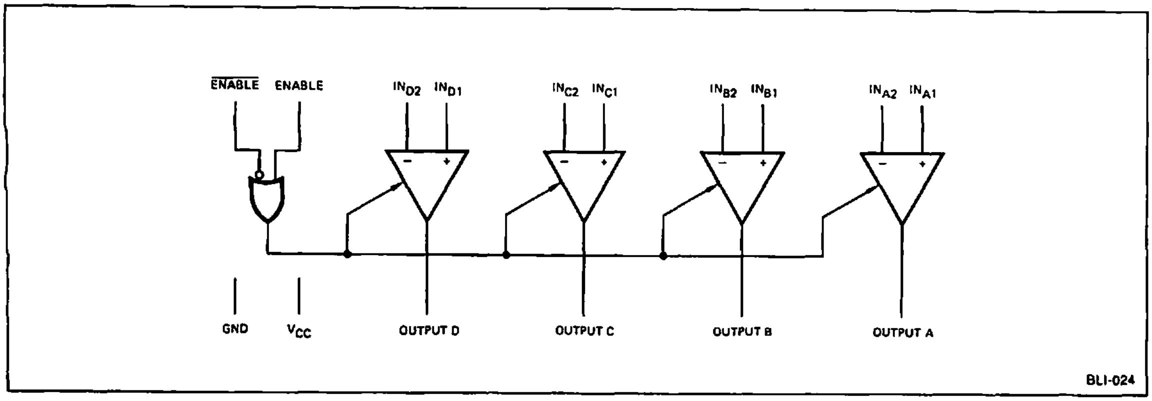
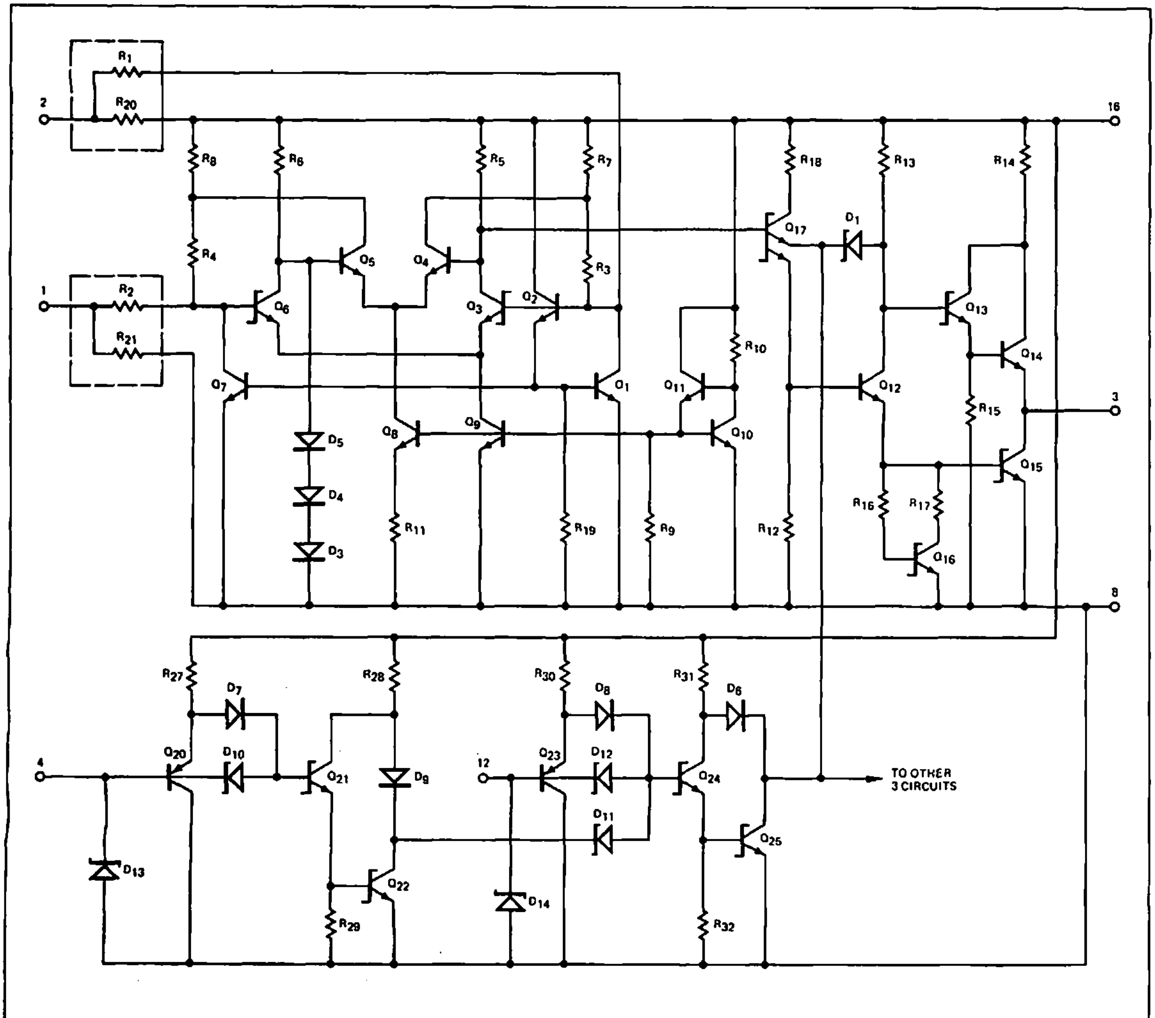


Figure 7. Am26LS32 Logic Diagram.



Note: R_3 and R_4 values for Am26LS32 are half the Am26LS33 values.

Figure 8. Am26LS32 and Am26LS33 Circuit Diagram (Only one receiver shown).

APPLICATIONS IN MIXED RS-232 AND 422/3 SYSTEMS

A system implemented with the RS-422 differential output cannot be used to drive an RS-232C system directly. An RS-423 single-ended driver, such as the Am26LS29 or Am26LS30, may be used provided certain precautions are observed.

1. Although the RS-423 driver output specification of between 4 to 5V does not meet the RS-232C specification of 6V, operation is usually satisfactory with RS-232C receivers. This is achieved because the short cable lengths permitted by RS-232C cause very little signal degredation and because of the low source impedance of the RS-423 driver.
2. RS-232C specifies that the rise time for the signal to pass through the ±3.0V transition region shall not exceed 4% of the signal element duration. RS-423 requires much slower rise times, specified from 10% to 90% of the total signal amplitude, to reduce cross talk for operation over longer distances. Therefore, the RS-423 driver in the equipment must be waveshaped. This is achieved by selection of a capacitor value for the Am26LS30 to simultaneously meet the requirements of both RS-423 and RS-232C for data rates covered by RS-232C.
3. RS-423 specifies one common return ground for each direction of transmission, RS-232C requires only one for both directions of transmission. Care must be taken to insure that a return ground path has been created when interfacing between the two systems.
4. RS-232C does not require termination, while it may be necessary for RS-422 and 423. Detailed consideration of termination is covered in the next section.

Note that RS-422 and RS-423 specifies that receivers should not be damaged by voltages up to 12V, while RS-232C allows drivers to produce output voltages up to 25V. The Am26LS32 receiver has been designed to avoid this hazard and can withstand input voltages of ±25 volts.

RS-422 TRANSMISSION LINE FEATURES

Any time a receiver and transmitter are connected with more than a few inches of a wire, problems due to reflections can arise if care is not exercised to terminate the line correctly. RS-422 describes the cable as a twisted pair of approximately 120Ω impedance terminated in a resistor R_T. R_T is not specified because there are two extreme values which may be chosen for the two following general classes of usage: (1) single direction transmission; and (2) multi-direction and multiple source transmission (party line). Considering the cable impedance only, the termination should equal the cable impedance of 120Ω. However this reduces the terminated cable resistance as seen by the driver to only 60Ω, with resulting loading of the output signal. This loading causes a reduction of S/N ratio at the received terminal due to the decrease in signal voltage swing. The solution lies in a compromise between an R_T of 120Ω which provides maximum power transfer at a reduced S/N ratio or R_T of 240Ω which causes a mis-match of 2-to-1 but no S/N reduction. The choice is left to the user as it is system dependent. Both schemes will work for an average line length and should only approach the margins at maximum line length and maximum bit rates.

Electronic Industries Association, when preparing EIA Standard RS-422 conducted their tests with 24 gauge twisted pair wire. The resulting length *vs.* data rate, is published as a guideline in RS-422 (Figure 9). This shows two important results: (1) Unmodulated baseband (NRZ) signalling is not recommended at distances greater than 4000 feet; (2) At data

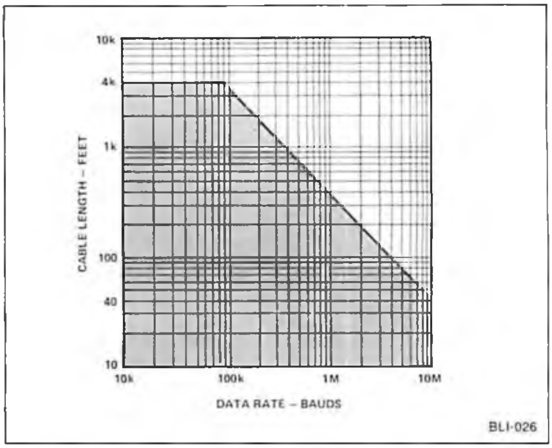


Figure 9. Data Rate Versus Cable Length for Balanced, Twisted Pair Cable (From EIA RS-422).

rates above about 100KHz, the maximum cable length for acceptable signal quality is inversely proportional to data rate.

Result (1) above is due to the DC resistance of the cable. For a 4000 foot cable with a DC resistance of 30 ohms/1000 feet, the DC series loop resistance is 240Ω. The minimum allowable terminated differential load impedance is 90Ω. The DC voltage attentuation is 90/(90 – 240) = 1/4(6db), which is arbitrarily chosen as the maximum allowable limit.

Result (2) is due to line losses. Laboratory tests using the 26LS31 Line Driver connected to the 26LS32 Line Receiver by 800 feet of ordinary 20 AWG twisted pair (Beldon #8205 plastic-jacketed wire), terminated in its characteristic impedance of 100Ω were evaluated. The input waveform was a 500KHz square wave with (10% to 90%) rise and fall times of less than 10ns. The output waveform produced rise and fall times which together accounted for approximately one-half the period ($t_r + t_f = 500ns$). This was due to line loss and constant capacity. The energy per cycle of the output waveform is approximately 25% lower than that of the input. The input rise and fall times are not a function of line length, assuming matching termination. The output rise and fall times are dependent upon length in a complex manner. Furthermore, it can be shown by observation that they build up along the line.

Many good reference sources are available on the subject of transmission lines (References 1, 2, 3 and 4). These will provide background information to the following discussion.

Seshadri in Reference (1) has analyzed a line with series resistance losses and has shown that rise time varies with the square of the length. This shows series resistance to be a function of the square root of frequency. However when one tries to use this result in combination with the previous result, it becomes apparent just how difficult the problem is. In Reference (2), the authors point out that skin depth implies a frequency dependent series inductance as well as resistance, and that one cannot be considered without the other.

They go on to show how this leads to the same result; namely that rise and fall times vary with the square of distance.

No attempt will be made to explain here why Figure 5 shows maximum length varying inversely with frequency rather than with the square of frequency. Certainly many complex factors are involved. Our laboratory observations showed a dependence somewhere in between linear and square law.

The Am26LS31 Quad Line Driver and the Am26LS32 Quad Line Receiver are capable of good, clean operation to the distance limits and data rate limits of RS-422.

SYSTEM APPLICATIONS

The Am26LS30, 31, 32 and 33 can be combined in various signaling networks. Using Am26LS29, Am26LS30 and Am26LS32, Figure 10, a unidirectional RS-423 communication can be constructed. Allowing for the voltage variation described earlier, RS-232C requirements can be satisfied. It should be noted that the Am26LS29 or Am26LS30 is used above to meet the bipolar requirements. If a single-ended line, Figure 11, is required without a bipolar requirement, the Am26LS31 can be used by biasing the reference terminal of the receiver to approximately 1.5 volts. Note that additional resistors will enhance fail safe operation.

Figure 12 shows the use of the Am26LS31 and Am26LS32 to meet a balanced line, single direction RS-422 application. If bidirectionality is required, an additional termination should be added as shown in Figure 13.

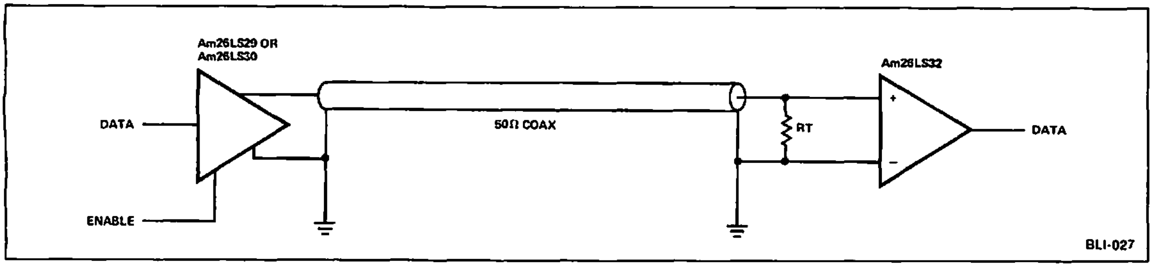


Figure 10. Unidirectional RS-423 (partial RS-232C).

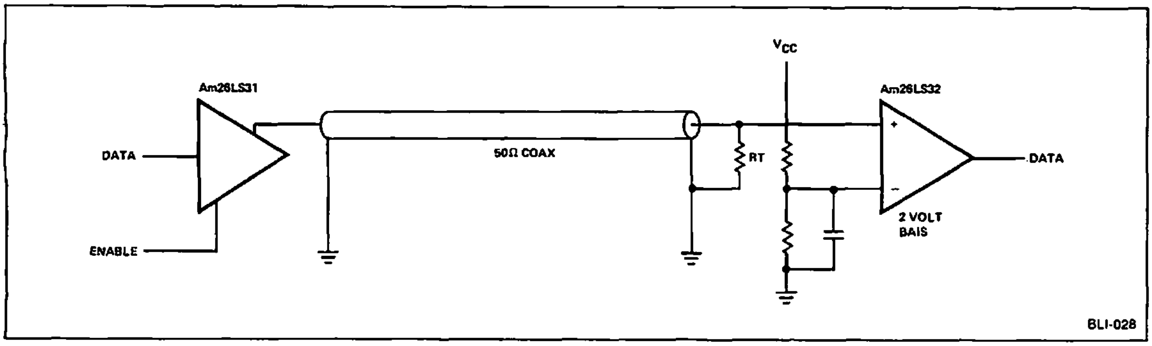


Figure 11. Single-Ended Line Without Bipolar Requirement.

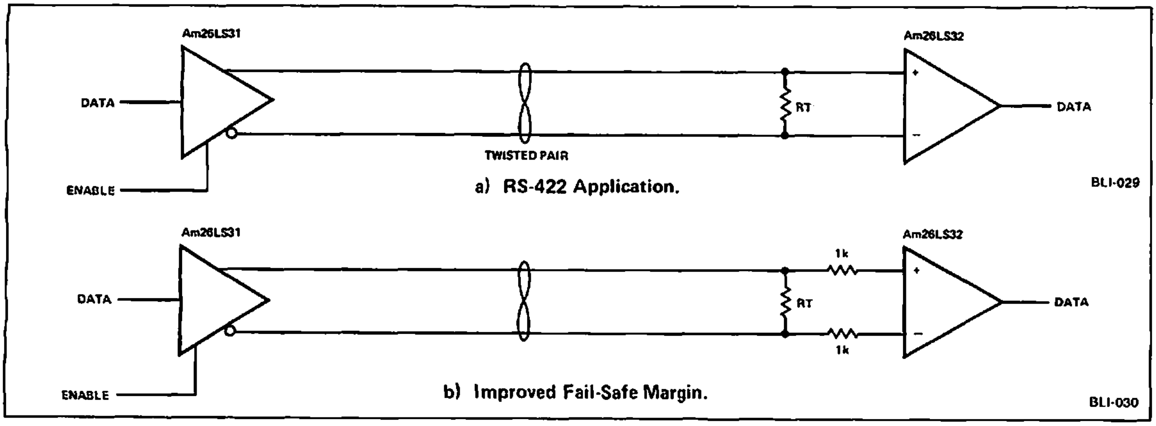


Figure 12.

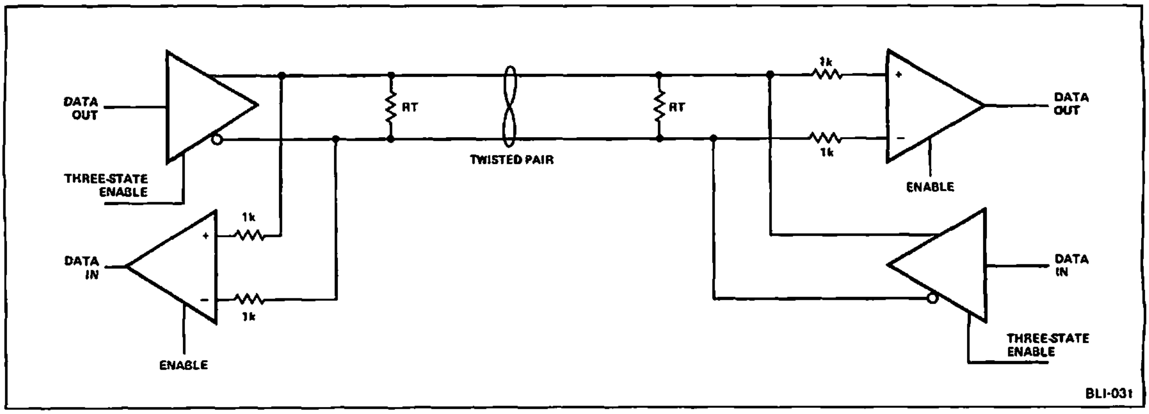


Figure 13. Bidirectional RS-422.

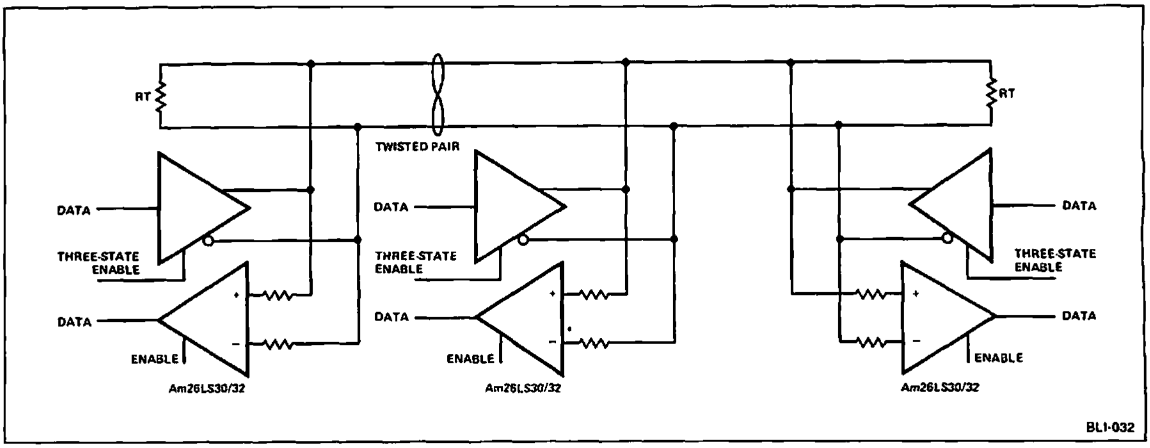


Figure 14. Party Line Configuration.

a) Full Duplex Four-Wire Data Communication RS-422 Interface (with Data Modem).

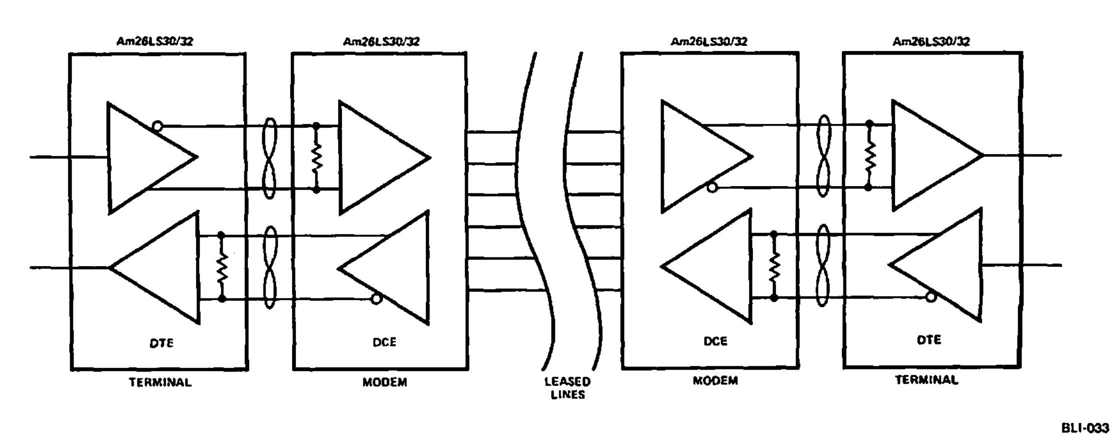


Figure 15.

b) Full Duplex Four-Wire Data Communication RS-422 Interface (without Data Modem).

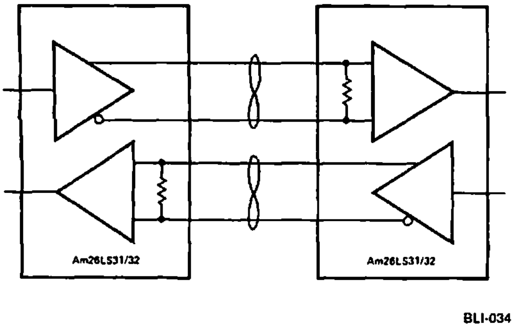


Figure 15. (Cont.)

The high speed capability of RS-422 has attracted the interest of many computer designers for use in the party line mode (Figure 14). The most common usage is that of a four wire full duplex exchange system (Figure 15). This mode of operation involves two pairs of wires each handling a single direction of traffic. The outgoing direction consists of one driver (Am26LS30 or Am26LS31) and n receivers (Am26LS32 or Am26LS33). The incoming direction consists of one receiver (Am26LS32 or Am26LS33) and n drivers (Am26LS30 or Am26LS31). This seems extremely simple to organize. However, problems arise when system ground is considered. If the network of receiver and driver span a moderate to long physical distance, ground loop noise or differences are developed changing the voltage that appears at the terminals of all receivers and drivers except for the one driver that is active. It remains the system reference as long as it is active. This induced or system developed voltage is referred to as Common Mode voltage (CMV) and as such must be considered as a device parameter. All manufacturers specify CMV capability of their receiver in compliance with RS-422 (approx. 7 volts plus signal) but there is no specification for drivers. If the dimensions of the system are short compared to 1/4 wave length of the maximum date rise and fall times, the CMV can be assumed to be minimal and drivers with single voltage supply and limited negative CMV can be used, i.e., Am26LS31. If the system dimensions are large, the CMV will cause problems in that the driver will clamp to the ground the moment the collective or apparent voltage swings below minus 0.5 volts relative to the driver ground, causing a short in the line and increasing level shift and noise. The clamping is caused in part by conduction of the I/C substrate diode. The problem can be avoided by using a driver with an output common mode range (Am26LS30). The Am26LS30 guarantees an output CMV range of ±10 volts about the driver ground reference. New international standards are under consideration to specify this mode of operation. In conclusion, a good system of 4 wire full duplex for data communication would use as an outgoing pair an Am26LS30 line driver and up to 12 – Am26LS32 line receivers, with a termination at the near and far ends of the cable. The same system would use as an incoming pair an Am26LS32 line receiver and up to 32 – Am26LS30 line drivers with only one enabled at a time and all others in three-state mode with cable termination at both near and far ends of the cable.

Many other applications are possible using this family of devices. Although the designs are based on the requirements of the EIA data communications specifications, they are not limited to these situations. Aircraft buses and internal equipment interconnections will benefit from the features offered by these products.

REFERENCES

1. Seshadri, S. R., Fundamental of Transmission Lines and Electromagnetic Fields, (U. of Wisconsin), Addison-Wesley, Reading, Mass., 1971.
2. Adler, R. B., L. J. Chu, and R. M. Fano, Electromagnetic Energy Transmission and Radiation, (MIT), John Wiley & Sons, New York, 1963.
3. Matick, R. E., Transmission Lines for Digital and Communication Networks, (IBM), McGraw-Hill, New York, 1969.
4. Reference Data for Radio Engineers, (ITT), Fifth Edition, Howard W. Sams & Company, Indianapolis, 1974.
5. Electronic Industries Association, 2001 Eye Street, N.W. Washington, D.C., RS Standard Proposal, RS-232C, August, 1969.
6. Electronic Industries Association, 2001 Eye Street, N.W. Washington, D.C., RS Standard Proposal 1220, Rev. RS-422, September 21, 1976.
7. Electronic Industries Association, 2001 Eye Street, N.W. Washington, D.C., RS Standard Proposal 1221, Rev. RS-423, September 21, 1976.

Am26S10 • Am26S11

Quad Bus Transceivers

Distinctive Characteristics

- Input to bus is inverting on Am26S10
- Input to bus is non-inverting on Am26S11
- Quad high-speed open collector bus transceivers
- Driver outputs can sink 100mA at 0.8V maximum
- Bus compatible with Am2905, Am2906, Am2907
- Advanced Schottky processing
- PNP inputs to reduce input loading
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

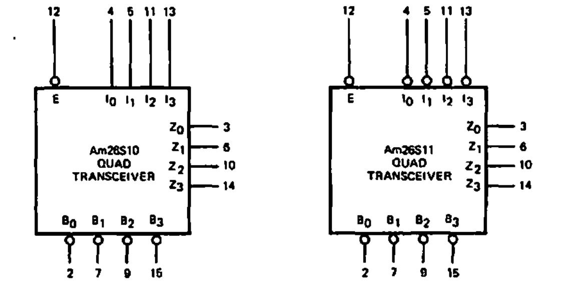
The Am26S10 and Am26S11 are quad Bus Transceivers consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.8 volts and four high-speed bus receivers. Each driver output is connected internally to the high-speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving ten Schottky TTL unit loads.

An active LOW enable gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable input can be conveniently driven by active LOW decoders such as the Am25LS139.

The bus output high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2.0 volts.

The Am26S10 and Am26S11 feature advanced Schottky processing to minimize propagation delay. The device package also has two ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND_1 and GND_2 should be tied to the ground bus external to the device package.

LOGIC SYMBOLS



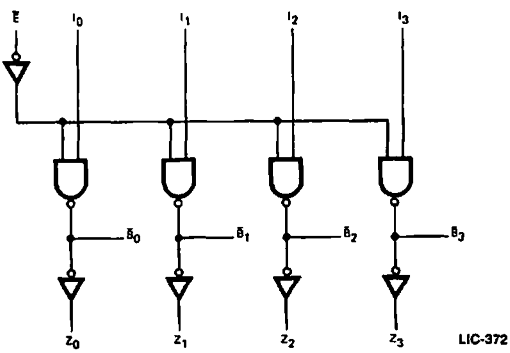
V_{CC} = Pin 16
GND_1 = Pin 1
GND_2 = Pin 8

ORDERING INFORMATION

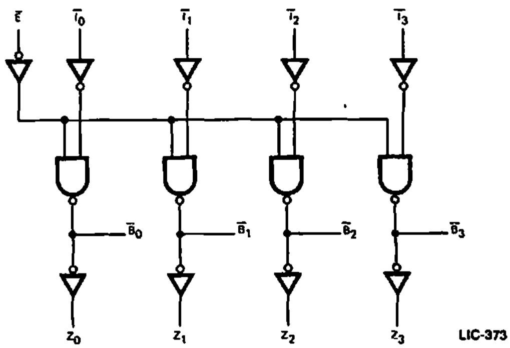
Package Type	Temperature Range	Am26S10 Order Number	Am26S11 Order Number
Molded DIP	0°C to +70°C	AM26S10PC	AM26S11PC
Hermetic DIP	0°C to +70°C	AM26S10DC	AM26S11DC
Dice	0°C to +70°C	AM26S10XC	AM26S11XC
Hermetic DIP	–55°C to +125°C	AM26S10DM	AM26S11DM
Hermetic Flat Pack	–55°C to +125°C	AM26S10FM	AM26S11FM
Dice	–55°C to +125°C	AM26S10XM	AM26S11XM

LOGIC DIAGRAMS

Am26S10

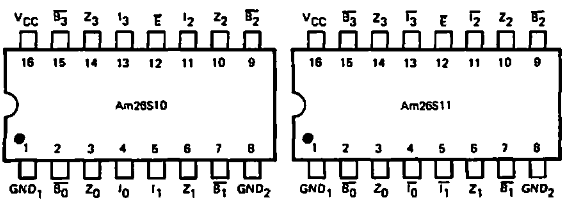


Am26S11



CONNECTION DIAGRAMS

Top Views



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to $+150^\circ$C
Temperature (Ambient) Under Bias	-55°C to $+125^\circ$C
Supply Voltage to Ground Potential	-0.5V to $+7$V
DC Voltage Applied to Outputs for High Output State	-0.5V to $+V_{CC}$ max.
DC Input Voltage	-0.5V to $+5.5$V
Output Current, Into Bus	200 mA
Output Current, Into Outputs (Except Bus)	30 mA
DC Input Current	-30mA to $+5.0$mA

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Am26S10XC, Am26S11XC	$T_A = 0^\circ$C to $+70^\circ$C	$V_{CC} = 5.0$V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am26S10XM, Am26S11XM	$T_A = -55^\circ$C to $+125^\circ$C	$V_{CC} = 5.0$V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Receiver Outputs)	V_{CC} = MIN., $I_{OH} = -1.0$mA $V_{IN} = V_{IL}$ or V_{IH}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Receiver Outputs)	V_{CC} = MIN., I_{OL} = 20mA $V_{IN} = V_{IL}$ or V_{IH}				0.5	Volts
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs				0.8	Volts
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				-1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4V	Enable			-0.36	mA
			Data			-0.54	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7V	Enable			20	μA
			Data			30	
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 5.5V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX. (Note 3)	MIL	-20		-55	mA
			COM'L	-18		-60	
I_{CCL}	Power Supply Current (All Bus Outputs LOW)	V_{CC} = MAX. Enable = GND	Am26S10		45	70	mA
			Am26S11			80	

Bus Input/Output Characteristics

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Output LOW Voltage	V_{CC} = MIN.	MIL	I_{OL} = 40mA		0.33	0.5	Volts
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
			COM'L	I_{OL} = 40mA		0.33	0.5	
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.		V_O = 0.8V			-50	μA
			MIL	V_O = 4.5V			200	
			COM'L	V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V V_{CC} = MAX		MIL	2.4	2.0		Volts
				COM'L	2.25	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V V_{CC} = MIN		MIL		2.0	1.6	Volts
				COM'L		2.0	1.75	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Data Input to Bus	Am26S10	R_B = 50Ω, C_B = 50pF (Note 1)		10	15	ns
t_{PHL}					10	15	
t_{PLH}		Am26S11			12	19	
t_{PHL}					12	19	
t_{PLH}	Enable Input to Bus	Am26S10			14	18	ns
t_{PHL}					13	18	
t_{PLH}		Am26S11			15	20	
t_{PHL}					14	20	
t_{PLH}	Bus to Receiver Out		R_B = 50Ω, R_L = 280Ω, C_B = 50pF (Note 1), C_L = 15pF		10	15	ns
t_{PHL}					10	15	
t_r	Bus		R_B = 50Ω, C_B = 50pF (Note 1)	4.0	10		ns
t_f	Bus			2.0	4.0		ns

Note 1. Includes probe and jig capacitance.

TRUTH TABLES

Am26S10

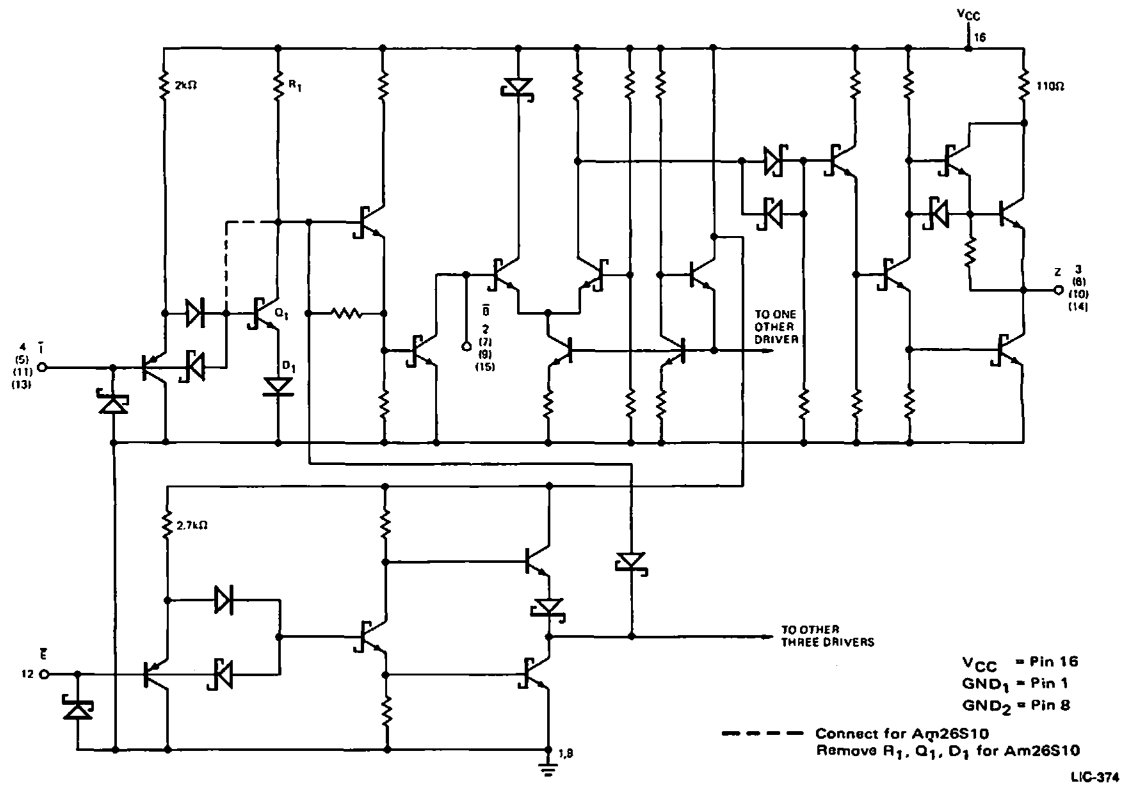
Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

Am26S11

Inputs		Outputs	
$\overline{E}$	$\overline{I}$	$\overline{B}$	Z
L	L	L	H
L	H	H	L
H	X	Y	$\overline{Y}$

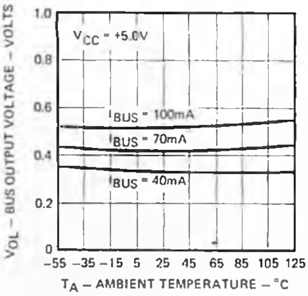
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus (Assumes Control by Another Bus Transceiver)

Am26S10/Am26S11 SCHEMATIC DIAGRAM



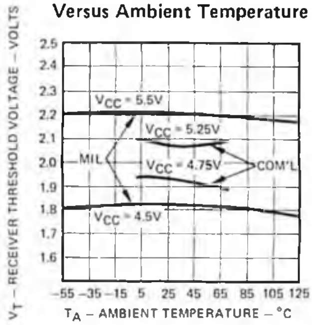
TYPICAL PERFORMANCE CURVES

Typical Bus Output Low Voltage Versus Ambient Temperature



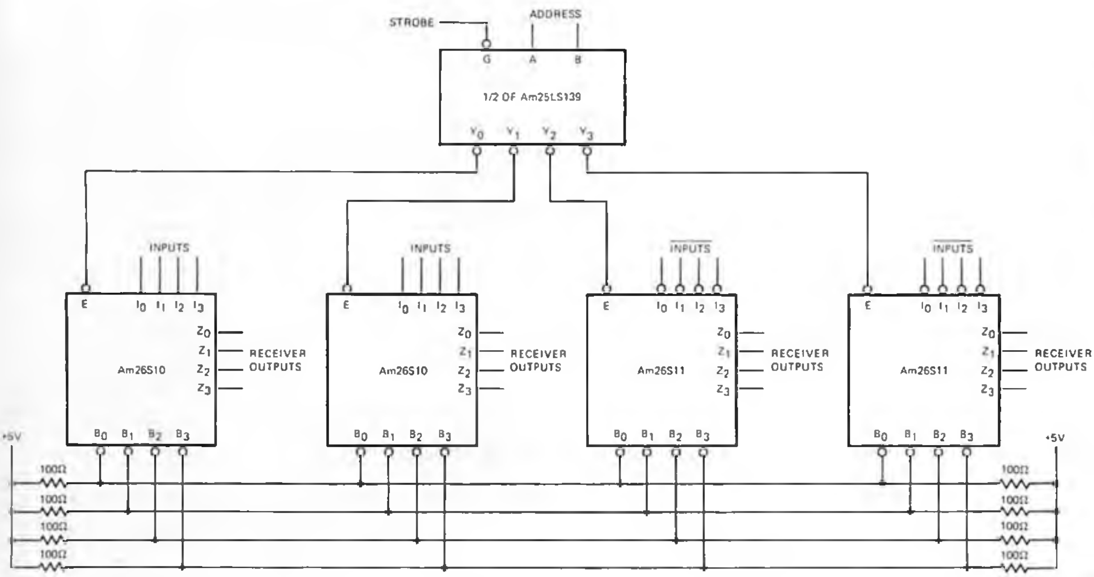
LIC-375

Receiver Threshold Variation Versus Ambient Temperature



LIC-376

TYPICAL APPLICATION

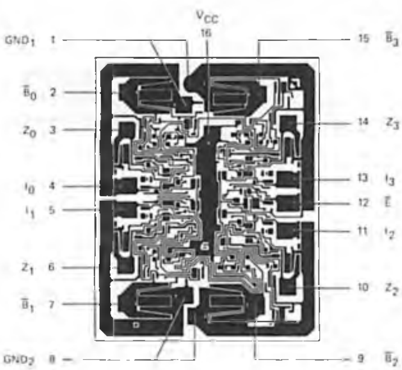


100Ω PARTY LINE OPERATION.

LIC-377

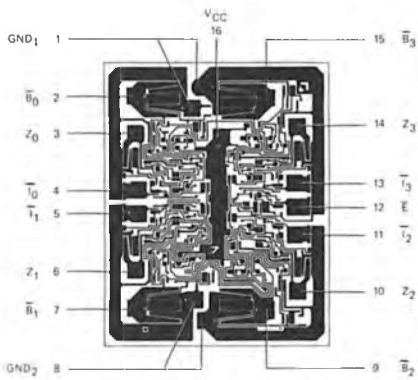
Metallization and Pad Layout

Am26S10



DIE SIZE 0.059" X 0.075"

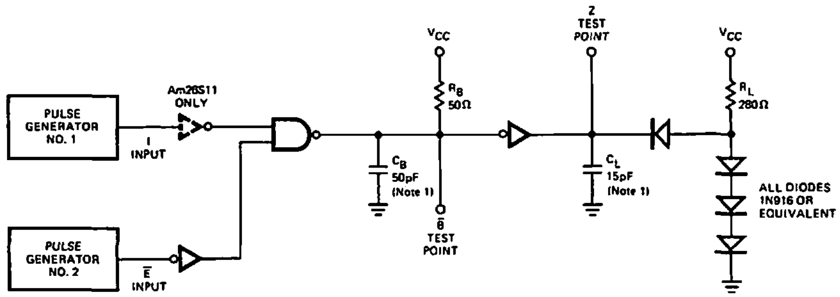
Am26S11



DIE SIZE 0.059" X 0.075"

SWITCHING CHARACTERISTICS

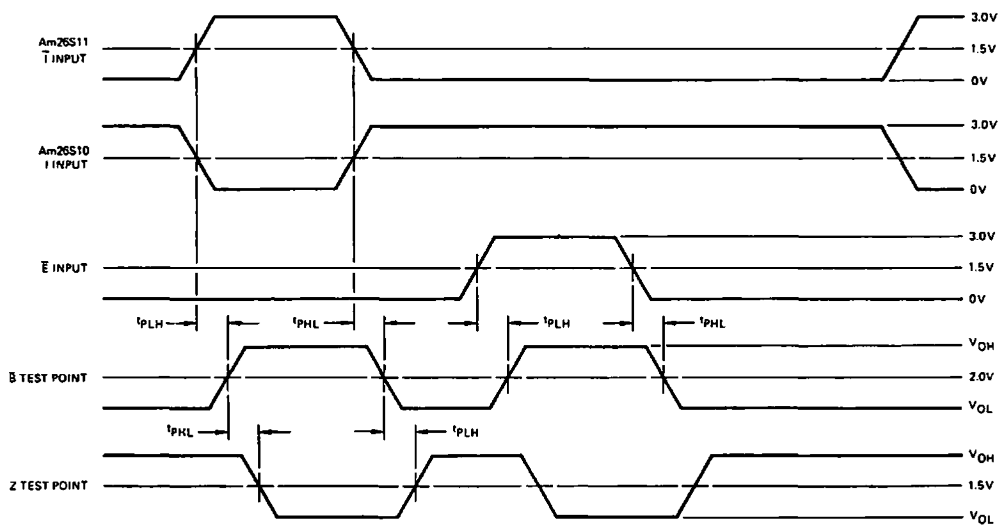
TEST CIRCUIT



LIC-378

Note 1. Includes Probe and Jig Capacitance.

WAVEFORMS



LIC-379

Am26S12•Am26S12A

Quad Bus Transceiver

Distinctive Characteristics

- Quad high-speed bus transceivers
- Driver outputs can sink 100mA at 0.7V typically
- 100% reliability assurance testing in compliance with MIL-STD-883
- Choice of receiver hysteresis characteristics

FUNCTIONAL DESCRIPTION

The Am26S12 • Am26S12A are high-speed quad Bus Transceivers consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.7 volts and four high-speed bus receivers. Each driver output is brought out and also connected internally to the high-speed bus receiver. The receiver has an input hysteresis characteristic and a TTL output capable of driving ten TTL Loads.

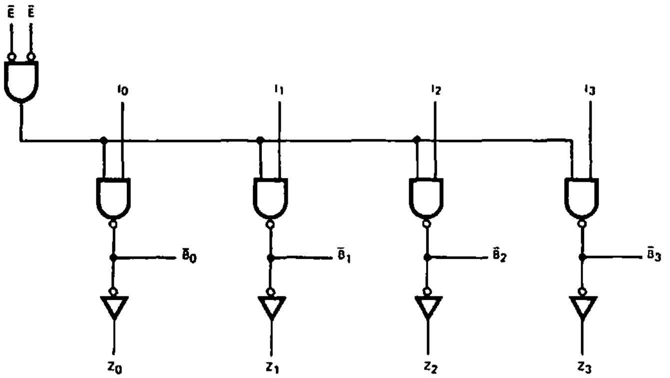
An active LOW, two-input AND gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable inputs can be conveniently driven by active LOW decoders such as the Am54S/74S139.

The high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The hysteresis characteristic of the Am26S12 receiver is chosen so that the receiver output switches to a HIGH logic level when the receiver input is at a HIGH logic level and moves to 1.4 volts typically, and switches to a LOW logic level when the receiver input is at a LOW logic level and moves to 2.0 volts typically. This hysteresis characteristic makes the receiver very insensitive to noise on the bus.

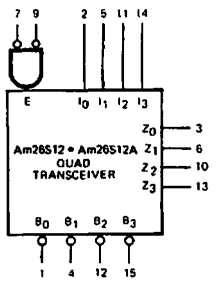
The Am26S12A is functionally identical to the Am26S12 but has a different hysteresis characteristic so that the output switches with the input being typically at 1.2 volts or 2.25 volts. In both devices the threshold margin, the difference between the switching points, is greater than 0.4 volts.

4

LOGIC DIAGRAM/SYMBOL



LIC-380



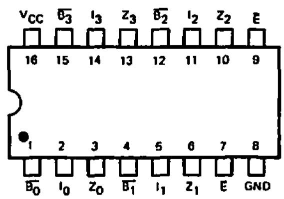
VCC = PIN 16
GND = Pin 8

LIC-381

ORDERING INFORMATION

Package Type	Temperature Range	Am26S12 Order Number	Am26S12A Order Number
Molded DIP	0°C to +75°C	AM26S12PC	AM26S12APC
Hermetic DIP	0°C to +75°C	AM26S12DC	AM26S12ADC
Dice	0°C to +75°C	AM26S12XC	AM26S12AXC
Hermetic DIP	–55°C to +125°C	AM26S12DM	AM26S12ADM
Flat Pak	–55°C to +125°C	AM26S12FM	AM26S12AFM
Dice	–55°C to +125°C	AM26S12XM	AM26S12AXM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-382

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to $+V_{CC}$ max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs (BUS)	200mA
Output Current, Into Outputs (Receiver)	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am26S12XC-Am26S12AXC $T_A = 0°C$ to $+75°C$ $V_{CC} = 5.0V \pm 5\%$ (COM Range)
Am26S12XM-Am26S12AXM $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIL Range) Note 1

Parameters	Description	Test Conditions	Min.	Typ. (Note 2)	Max.	Units
I_{CC}	Power Supply Current	V_{CC} = MAX.		46	70	mA
I_{BUS}	Bus Leakage Current	V_{CC} = MAX. or 0V; V_{BUS} = 4.0V; Driver in OFF State			100	μA

Driver Characteristics

Parameters	Description	Test Conditions			Min.	Typ.	Max.	Units
V_{OL} (Note 1)	Output LOW Voltage	V_{CC} = MIN. $V_{IN} = V_{IH}$ or V_{IL}	COM'L	I_{OL} = 100mA		0.7	0.8	Volts
			MIL	I_{OL} = 60mA		0.55	0.7	Volts
				I_{OL} = 100mA		0.7	0.85	
V_{IH}	Input HIGH Voltage				2.0			Volts
V_{IL}	Input LOW Voltage						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX., V_I = 5.5V					1.0	mA
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX., V_I = 2.4V				1.0	40	μA
I_{IL}	Unit Load Input LOW Current	V_{CC} = MAX., V_I = 0.4V				−0.4	−1.6	mA

Receiver Characteristics

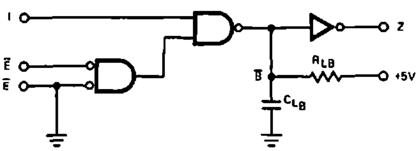
Parameters	Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −800μA $V_{IN} = V_{IL}$ (Receiver)		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA $V_{IN} = V_{IL}$ (Receiver)			0.4	0.5	Volts
V_{IH}	Input HIGH Level Threshold	$\overline{E}$ = H	Am26S12	1.8	2.0	2.2	Volts
			Am26S12A	2.05	2.25	2.45	
V_{IL}	Input LOW Level Threshold	$\overline{E}$ = H	Am26S12	1.2	1.4	1.6	Volts
			Am26S12A	1.0	1.2	1.4	
V_{TM}	Input Threshold Margin	$\overline{E}$ = H		0.4			Volts
I_{OS}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−20		−55	mA

Notes: 1. For the Am26S12FM, Am26S12AFM the output current must be limited at 60mA or the maximum case temperature limited to 125°C for correct operation.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

Switching Characteristics (T_A = 25°C, V_{CC} = 5.0V)

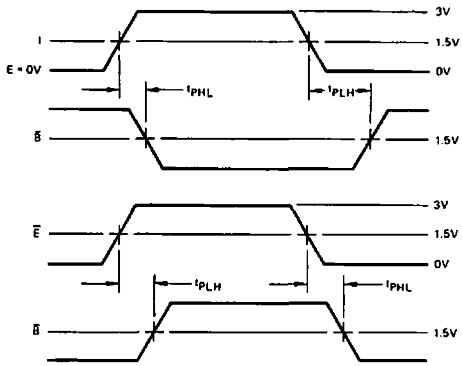
Parameters	Description	Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Turn Off Delay Input to Bus	C_{LB} = 15pF, R_{LB} = 100Ω		7	11	ns
t_{PHL}	Turn On Delay Input to Bus	C_{LB} = 300pF, R_{LB} = 50Ω		14	21	ns
t_{PLH}	Turn Off Delay Enable to Bus	C_{LB} = 15pF, R_{LB} = 50Ω		10	15	ns
t_{PHL}	Turn On Delay Enable to Bus	C_{LB} = 15pF, R_{LB} = 50Ω		10	15	ns
t_{PLH}	Turn Off Delay Bus to Output	C_L = 15pF		18	26	ns
t_{PHL}	Turn On Delay Bus to Output	C_L = 15pF		18	26	ns

SWITCHING CIRCUITS AND WAVEFORMS



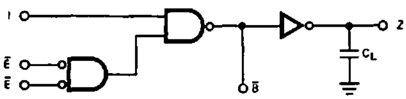
LIC-383

Frequency 5MHz
$t_r = t_f$ = 2ns Measured Between
1V to 2V Levels.

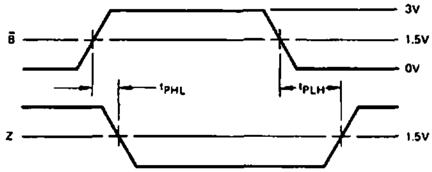


LIC-384

Figure 1. Bus Propagation Delays



LIC-385



LIC-386

Figure 2. Receiver Propagation Delays

TRUTH TABLE
Am26S12/26S12A

Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus

Table I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	Equivalent Input Unit Load LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table II

PERFORMANCE CURVES

Am26S12 Typical Receiver Input Characteristic

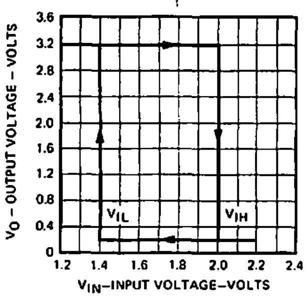


Figure 3

Am26S12A Typical Receiver Input Characteristic

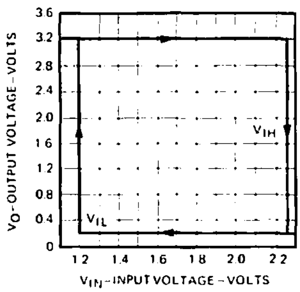


Figure 4

LIC-387 LIC-388

INPUT/OUTPUT CIRCUITRY

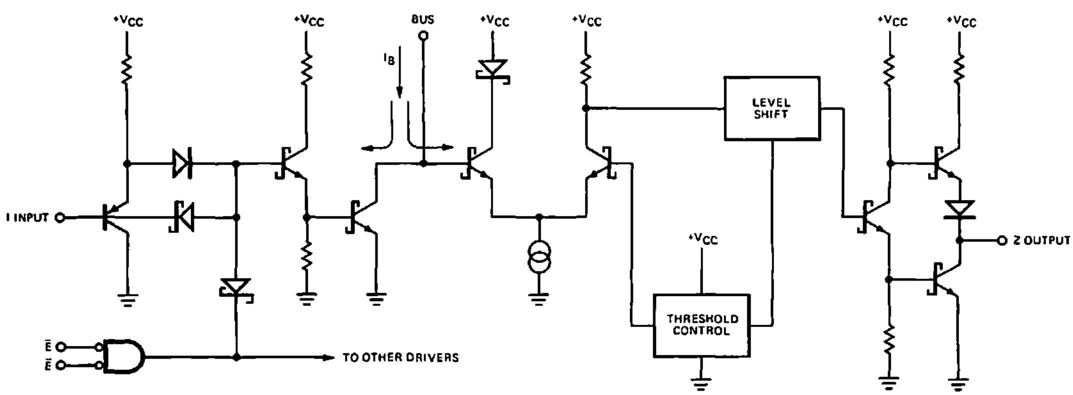


Figure 5

LIC-389

Am26S12/26S12A APPLICATION

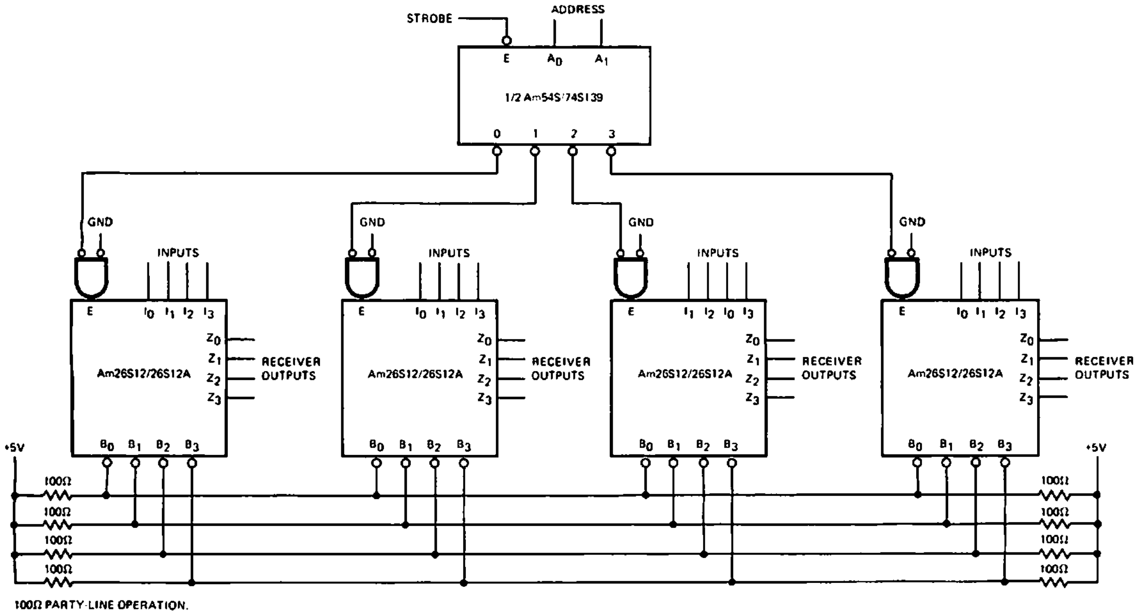
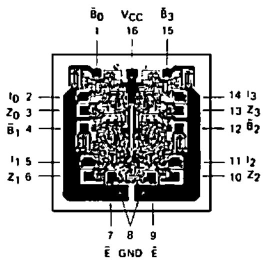


Figure 6

Metallization and Pad Layout



DIE SIZE: 0.071" x 0.072"

4

Am2614

Quad Single-Ended Line Driver

Distinctive Characteristics

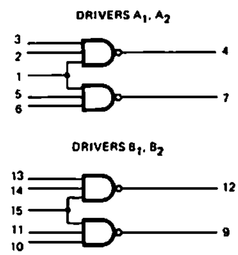
- Quad single-ended driver for multi-channel common ground operation
- Single 5V power supply
- DTL, TTL compatible
- Short-circuit protected outputs
- Capable of driving 50Ω terminated transmission lines
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2614 is a DTL, TTL compatible line driver operating off a single 5V supply. The Am2614 is a quad inverting driver with two separate inputs and one common-strobe input for each pair of drivers. The device has active pull-up outputs for high-speed and HIGH capacitance drive. The Am2614 is ideal for single-ended transmission line driving, or as a high-speed, high-fan-out driver for semiconductor memory decoding, buffering, clock driving and general logic use.

The Am2614 has short circuit protected active pull-ups, and incorporates input clamp diodes to reduce the effect of line transients, and also is capable of driving 50Ω terminated transmission lines.

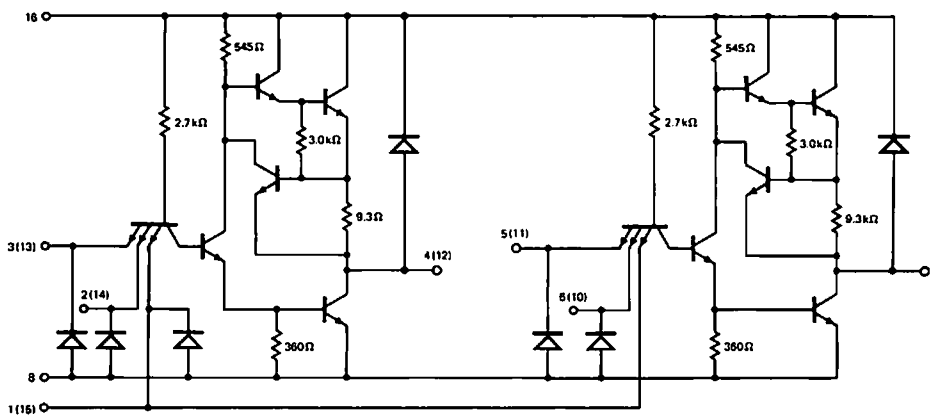
LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

LIC-391

CIRCUIT DIAGRAM



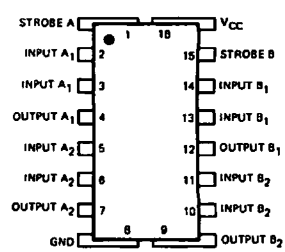
LIC-392

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	AM2614DM
Flat Pak	−55°C to +125°C	AM2614FM
Dice	−55°C to +125°C	AM2614XM
Hermetic DIP	0°C to +70°C	AM2614DC
Molded DIP	0°C to +70°C	AM2614PC
Dice	0°C to +70°C	AM2614XC

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

LIC-393

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to $+V_{CC}$ max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	mA
DC Input Current	Note 1

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2614XM (MIL)	T_A = −55°C to +125°C	V_{CC}MIN. = 4.50V	V_{CC}MAX. = 5.50V
Am2614XC (COM'L)	T_A = 0°C to +70°C	V_{CC}MIN. = 4.75V	V_{CC}MAX. = 5.25V

DC Characteristics (Note 2)

Parameters	Description	Test Conditions		T_A MIN. Min.	T_A MIN. Max.	LIMITS +25°C Min.	LIMITS +25°C Typ.	LIMITS +25°C Max.	T_AMAX. Min.	T_AMAX. Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −10mA		2.4		2.4	3.2		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 40mA	MIL		0.4		0.2	0.4		0.4	Volts
			COM'L		0.45		0.2	0.45		0.45	
V_{IH}	Input HIGH Voltage	V_{CC} = MIN.	MIL	2.0		1.7	1.5		1.4		Volts
			COM'L	1.9		1.8	1.5		1.6		
V_{IL}	Input LOW Voltage	V_{CC} = MAX.	MIL		0.8		1.3	0.9		0.8	Volts
			COM'L		0.85		1.3	0.85		0.85	
I_F	Input Load Current	V_{CC} = MAX.	V_F = 0.4V, MIL V_F = 0.45V, COM'L		−2.4		−1.65	−2.4		−2.4	mA
I_R	Reverse Input Current	V_{CC} = MAX. V_R = 4.5V			90			90		90	µA
I_{SC}	Short Circuit Current	V_{CC} = MAX., V_O = 0V				−40	−90	−120			mA
I_{PD}	Power Supply Current	V_{CC} = MAX., Inputs = 0V			48.7		33	48.7		48.7	
		V_{CC} = 7.0V, Inputs = 0V	COM'L				46	70			
			MIL				46	65.7			
I_{CEX}	Reverse Output Current	V_{CC} = MAX.	V_{CEX} = 5.5V, MIL		100		10	100		200	µA
			V_{CEX} = 5.25V, COM'L		100		10	100		200	
V_{OLC}	Output Low Clamp Voltage	V_{CC} = MAX., I_{OLC} = −40mA					−0.8	−1.5			Volts
V_{IC}	Input Clamp Voltage	V_{CC} = MIN., I_{IC} = −12mA					−1.0	−1.5			Volts

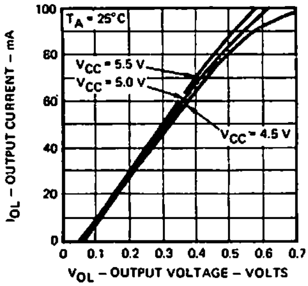
Switching Characteristics (T_A = 25°C unless otherwise specified)

Parameters	Description	Test Conditions	Am2614XM Min.	Am2614XM Typ.	Am2614XM Max.	Am2614XC Min.	Am2614XC Typ.	Am2614XC Max.	Units
t_{pd+}	Turn Off Delay	V_{CC} = 5.0V, C_L = 30pF, V_M = 1.5V, Refer to Fig. 92		8	12		8	15	ns
t_{pd-}	Turn On Delay			7	10		7	12	ns

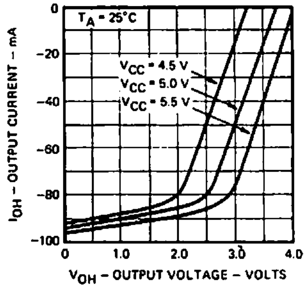
Notes: 1. Maximum current defined by DC Input voltage.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type or grade.

TYPICAL ELECTRICAL CHARACTERISTICS

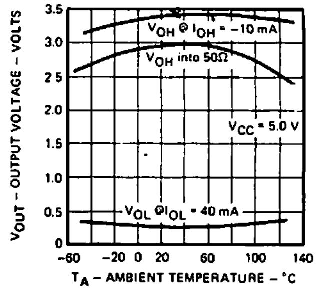
Output Low Current Versus Output Low Voltage



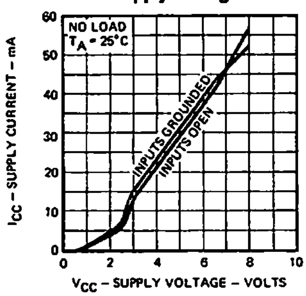
Output High Current Versus Output High Voltage



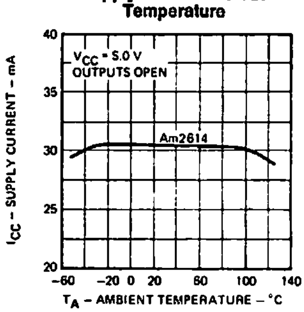
Logic Levels Versus Ambient Temperature



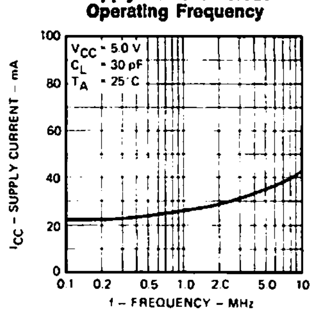
Supply Current Versus Supply Voltage



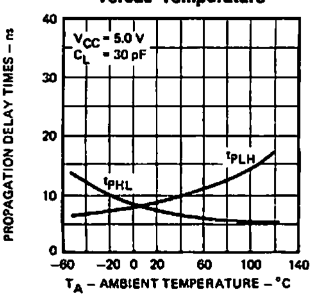
Supply Current Versus Temperature



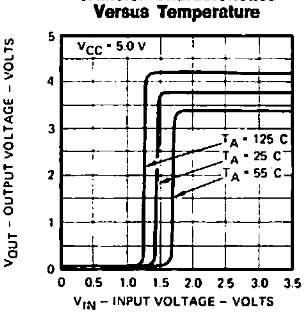
Supply Current Versus Operating Frequency



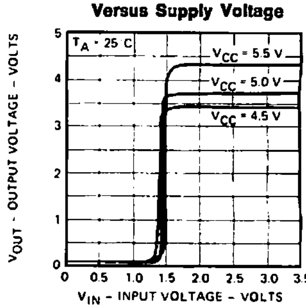
Propagation Delay Time Versus Temperature



Transfer Characteristics Versus Temperature



Transfer Characteristics Versus Supply Voltage



LIC-394

USER NOTES

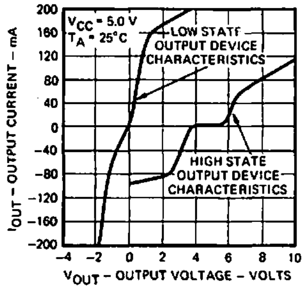
SINGLE ENDED LINES. The Am2614 quad line driver and the Am2615 dual differential amplifier allow data to be transmitted with only a single data wire per channel and a common ground for typically 8 data wires. This single-ended mode of interconnection offers considerable savings in integrated circuit packages required and effectively halves the number of interconnections as compared to a balanced differential system. The method still gives ±15V common mode rejection and DC noise margin of interconnected TTL logic. The common ground wire should be twisted in with the data wires so that any injected noise is common to all wires. If a multiwire cable with screen is used one of the wires is used as the common ground line, and the screen is tied to ground at the driving end only.

MATCHING. Transmission lines can be matched in a number of ways. The most widely used method is to terminate the line at the receiving end in its characteristic impedance. This impedance is connected across the input terminals of the receiver. A 130Ω resistor is included at the + input of each receiver for matching twisted pairs and this resistor, or if the characteristic impedance is not 130Ω, a discrete resistor is connected between the two receiver inputs. This method of matching causes a DC component in the signal. Power is dissipated in the resistor and the signal is attenuated. The DC component can be effectively removed by connecting a large capacitor in series with the terminating resistor.

The transmission line can also be terminated through the receiver power supply by placing equal value resistors from the + input of the receiver to V_{CC} and from the – input to ground. This method again has the disadvantage that a DC signal component exists, attenuation occurs, and power is dissipated in the terminating resistors but it does allow multiplexed operation in the balanced differential mode.

An alternate method of matching at the receiver is to back match at the driver. A resistor is placed in series with the line so that the signal from the driver which is reflected at the high input impedance of the receiver is absorbed at the driver. This method does not have a DC component and therefore no attenuation occurs and power is not dissipated in the resistor. For balanced differential driving a resistor is required in series with each line. The table below shows the value of each matching resistor required for lines of different characteristic impedance.

TYPICAL DC CHARACTERISTICS
FOR MATCHING TO TRANSMISSION LINE



LIC-395

BACK MATCHING TABLE

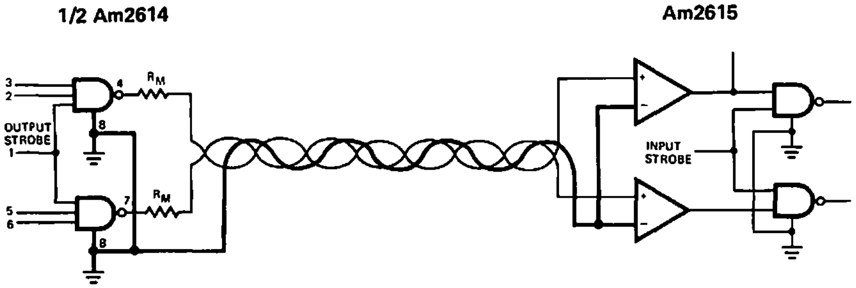
Z_O	R_M (ohms) SINGLE ENDED
50	24
75	51
92	68
100	75
130	110
300	280
600	580

LOADING RULES

Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
Strobe A	1	3	—	—
Input A_1	2	1.5	—	—
Input A_1	3	1.5	—	—
Output A_1	4	—	166	25
Input A_2	5	1.5	—	—
Input A_2	6	1.5	—	—
Output A_2	7	—	166	25
GND	8	—	—	—
Output B_2	9	—	166	25
Input B_2	10	1.5	—	—
Input B_2	11	1.5	—	—
Output B_2	12	—	166	25
Input B_1	13	1.5	—	—
Input B_1	14	1.5	—	—
Strobe B	15	3	—	—
V_{CC}	16	—	—	—

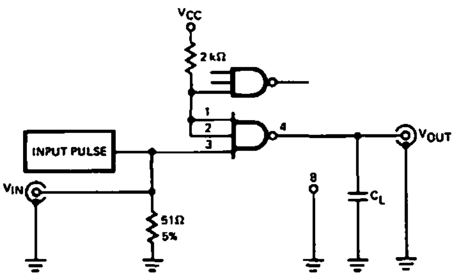
APPLICATIONS

Single-Ended Back-Matched Operation With Common Ground

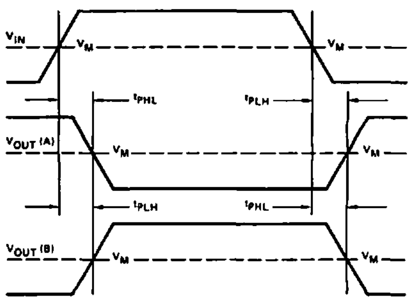


LIC-396

SWITCHING CIRCUITS AND WAVEFORMS



LIC-397



LIC-398

INPUT PULSE
Frequency = 500 kHz
Amplitude = 3.0 ±0.1 V
Pulse Width = 110 ±10 ns
$t_r = t_f \leq 5.0$ ns

Figure 1.

Am2615/9615

Dual Differential Line Receivers

Distinctive Characteristics:

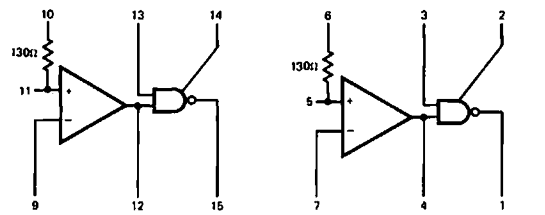
- Dual differential receiver (Am9615) pin-for-pin equivalent to the Fairchild 9615
- Dual differential receiver for single-ended data (Am2615)
- Single 5-volt supply
- High common-mode voltage range (±15 volts)
- Frequency response control, strobe, and internal terminating resistor
- Am2615 has fail safe capability
- Choice of uncommitted collector or active pull-up outputs
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2615 and Am9615 are dual differential line receivers designed to receive digital data from transmission lines and operate over the military and industrial temperature ranges using a single 5 volt supply. The Am2615 can receive 3 volt single ended and the Am9615 ±500 mV differential data in the presence of high level (±15 V) common mode voltages and deliver undisturbed logic levels to the following DTL or TTL circuitry. The response time of each receiver and thereby immunity to AC noise can be controlled by an external capacitor. A strobe is provided for each receiver together with a 130Ω input terminating resistor. Each output has an uncommitted collector with an active pull-up network available on an adjacent pin.

The Am2615 is identical to the Am9615 except for the input offset (threshold) voltage. The Am2615 has an input threshold of ~1.5 V compatible with DTL & TTL logic. The Am9615 has an input threshold of ~0 V. The Am2615 can directly replace the Am9615 and give fail safe protection in differential systems where the input difference is >2.0 V.

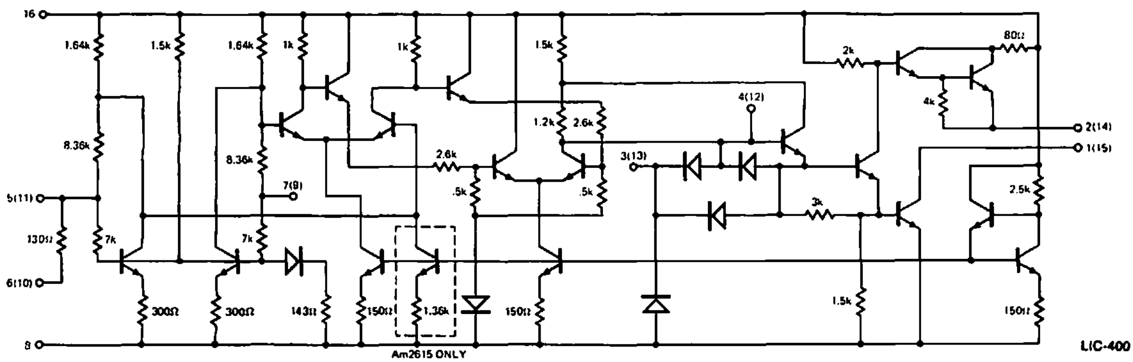
LOGIC DIAGRAM



LIC-399

V_{CC} = PIN 16
GND = PIN 8

CIRCUIT DIAGRAM

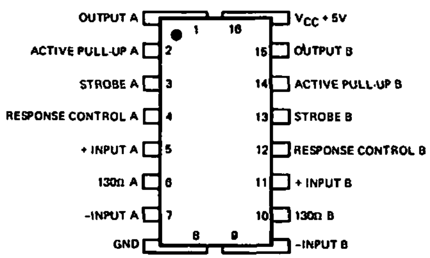


LIC-400

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am2615	Hermetic DIP	−55°C to +125°C	AM2615DM
	Flat Pak	−55°C to +125°C	AM2615FM
	Dice	−55°C to +125°C	AM2615XM
	Hermetic DIP	0°C to +75°C	AM2615DC
	Molded DIP	0°C to +75°C	AM2615PC
	Dice	0°C to +75°C	AM2615XC
Am9615	Hermetic DIP	−55°C to +125°C	9615DM
	Flat Pak	−55°C to +125°C	9615FM
	Dice	−55°C to +125°C	AM9615XM
	Hermetic DIP	0°C to +75°C	9615DC
	Molded DIP	0°C to +75°C	9615PC
	Dice	0°C to +75°C	AM9615XC

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

LIC-401

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +13.2 V
DC Strobe Input Voltage	−0.5 V to +5.5 V
DC Data Input Voltage	−20 V to + 20 V
Output Current, Into Outputs	30 mA
DC Input Current	maximum current is defined by DC Input Voltage

Am2615 ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Am2615XM	V_{CC} = 4.5V to 5.5V	T_A = −55°C to +125°C	(MIL grade)
Am2615XC	V_{CC} = 4.75V to 5.25V	T_A = 0°C to +75°C	(COM'L grade)

Parameters	Description	Test Conditions		LIMITS T_A = Min Min	Max	T_A = 25°C Min	Typ	Max	T_A = Max Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −5.0 mA, V_{IN+} = +0.8 V, V_{IN-} = 0 V		2.4		2.4	3.2		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MAX, I_{OH} = 15.0 mA, V_{IN+} = +2.0 V, V_{IN-} = 0 V	MIL grade		0.40		.18	0.40		0.40	Volts
			COM'L grade		0.45		.25	0.45		0.45	
I_{CEX}	Output Leakage Current	V_{CC} = MIN, V_{IN+} = 0 V, V_{IN-} = 4.5 V; V_{CEX} = 12 V	MIL grade		100			100		200	µA
		V_{CEX} = 5.25 V	COM'L grade								
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0 V, V_{IN+} = +0.8 V, V_{IN-} = 0 V	MIL grade	−15	−80	−15	−39	−80	−15	−80	mA
			COM'L grade	−14	−100	−14	−39	−100	−14	−100	
I_{IL}	Input Load Current	V_{CC} = MAX, V_{IN} = $V_{OL\ MAX}$, other input = V_{CC}			−0.9		−0.49	−0.7		−0.7	mA
$I_{IL(ST)}$	Strobe Input Low Current	V_{CC} = MAX V_{IN+} = +2.0V, V_{ST} = V_{OL} MAX V_{IN-} = 0 V			−2.4		−1.15	−2.4		−2.4	mA
$I_{IL(RC)}$	Response Control Input Load Current	V_{CC} = MAX V_{IN+} = +2.0V, V_{RC} = V_{OL} MAX V_{IN-} = 0 V				−1.2	−3.4				mA
V_{CM}	Common Mode Voltage	V_{CC} = 5.0 V V_{IN+} - V_{IN-} = 0.4 or 2.4 V		−15	+15	−15	±17.5	+15	−15	+15	V
$I_{IH(ST)}$	Strobe Input HIGH Current	V_{CC} = MIN, V_{ST} = 4.5 V, V_{IN+} = +0.8 V, V_{IN-} = 0 V	MIL grade					2.0		5.0	µA
			COM'L grade					5.0		10.0	
R_{IN}	Input Resistor	V_{CC} = 5.0 V, V_{IN+} = 0 V, V_{RES} = 1.0 V	MIL grade			77	130	167			Ω
			COM'L grade			74	130	179			
V_{TH}	Differential Input Threshold Voltage	V_{CM} = 0 V		+0.8	+2.0	+0.8	+1.5	+2.0	+0.8	+2.0	V
I_{CC}	Power Supply Current	V_{CC} = MAX, V_{IN+} = +2.0 V, V_{IN-} = 0 V	MIL grade		50		28.7	50		50	mA
			COM'L grade		50		28.7	50		50	

Switching Characteristics (T_A = 25°C)

Parameters			Test Conditions	Am2615XM Min	Typ	Max	Am2615XC Min	Typ	Max	Units
t_{pd+}	Turn Off Delay	R_L = 3.9 kΩ	V_{CC} = 5.0 V, C_L = 30 pF Refer to figure 4		30	50		30	75	ns
t_{pd-}	Turn On Delay	R_L = 390 Ω			30	50		30	75	
t_{pd+}	Turn Off Delay	Strobe to Output	R_L = 3.9 kΩ, C_L = 30 pF		7	12		7	15	ns
t_{pd-}	Turn On Delay	Strobe to Output	R_L = 390 Ω		10	15		10	20	

Am9615 ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Am9615XM	V_{CC} = 4.5V to 5.5V	T_A = −55°C to +125°C	(MIL grade)
Am9615XC	V_{CC} = 4.75V to 5.25V	T_A = 0°C to +75°C	(COM'L grade)

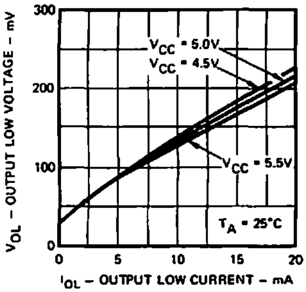
Parameters	Description	Test Conditions		T_A = Min Min	T_A = Min Max	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	T_A = Max Min	T_A = Max Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −5.0 mA V_{IN+} = −0.5 V, V_{IN-} = 0 V		2.4		2.4	3.2		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MAX I_{OH} = 15.0 mA V_{IN+} = +0.5 V, V_{IN-} = 0	MIL grade		0.40		.18	0.40		0.40	Volts
			COM'L grade		0.45		.25	0.45		0.45	
I_{CEX}	Output Leakage Current	V_{CC} = MIN V_{IN+} = 0 V V_{IN-} = V_{CC} — V_{CEX} = 12 V	MIL grade		100			100		200	µA
		V_{CEX} = 5.25 V	COM'L grade								
I_{SC}	Output Short Circuit Current	V_{CC} = MAX V_{OUT} = 0 V V_{IN+} = −0.5 V V_{IN-} = 0 V	MIL grade	−15	−80	−15	−39	−80	−15	−80	mA
			COM'L grade	−14	−100	−14	−39	−100	−14	−100	
I_{IL}	Input Load Current	V_{CC} = MAX V_{IN} = $V_{OL\ MAX}$, other input = V_{CC}			−0.9		−0.49	−0.7		−0.7	mA
$I_{IL(ST)}$	Strobe Input Low Current	V_{CC} = MAX V_{IN+} = +0.5 V V_{ST} = $V_{OL\ MAX}$ V_{IN-} = 0 V			−2.4		−1.15	−2.4		−2.4	mA
$I_{IL(RC)}$	Response Control Input Load Current	V_{CC} = MAX V_{IN+} = +0.5 V V_{RC} = $V_{OL\ MAX}$ V_{IN-} = 0 V					−1.2	−3.4			mA
V_{CM}	Common Mode Voltage	V_{CC} = 5.0 V V_{IN+} - V_{IN-} = ±2.0 V		−15	+15	−15	±17.5	+15	−15	+15	V
$I_{IH(ST)}$	Strobe Input HIGH Current	V_{CC} = MIN V_{ST} = 4.5 V V_{IN+} = −0.5 V V_{IN-} = 0 V	MIL grade					2.0		5.0	µA
			COM'L grade					5.0		10.0	
R_{IN}	Input Resistor	V_{CC} = 5.0 V V_{IN+} = 0 V V_{RES} = 1.0 V	MIL grade			77	130	167			Ω
			COM'L grade			74	130	179			
V_{TH}	Differential Input Threshold Voltage	V_{CM} = 0 V		−0.5	+0.5	−0.5	±0.02	+0.5	−0.5	+0.5	V
I_{CC}	Power Supply Current	V_{CC} = MAX V_{IN+} = +0.5 V V_{IN-} = 0 V	MIL grade		50		28.7	50		50	mA
			COM'L grade		50		28.7	50		50	

Switching Characteristics (T_A = 25°C)

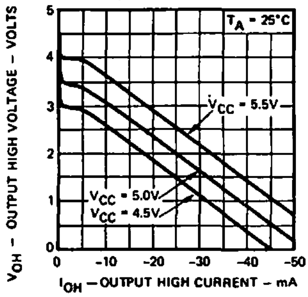
Parameters			Test Conditions	Am9615XM Min	Am9615XM Typ	Am9615XM Max	Am9615XC Min	Am9615XC Typ	Am9615XC Max	Units
t_{pd+}	Turn Off Delay	R_L = 3.9 kΩ	V_{CC} = 5.0 V, C_L = 30 pF Refer to figure 4		30	50		30	75	ns
t_{pd-}	Turn On Delay	R_L = 390 Ω			30	50		30	75	
t_{pd+}	Turn Off Delay	Strobe to Output	R_L = 3.9 kΩ, C_L = 30 pF		7	12		7	15	ns
t_{pd-}	Turn On Delay	Strobe to Output	R_L = 390 Ω		10	15		10	20	

D. C. CHARACTERISTICS

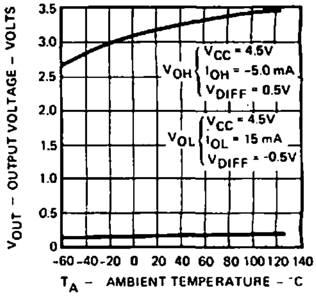
Output Low Voltage Versus Output Low Current



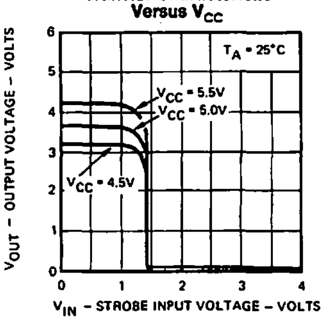
Output High Voltage Versus Output High Current



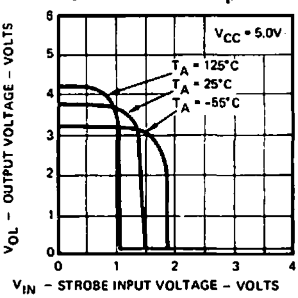
Output Voltage Versus Ambient Temperature



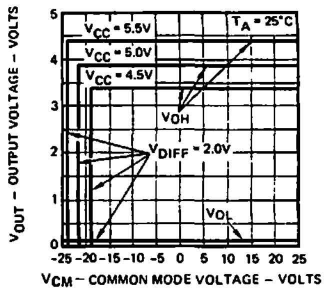
Strobe Input-Output Transfer Characteristic Versus V_{CC}



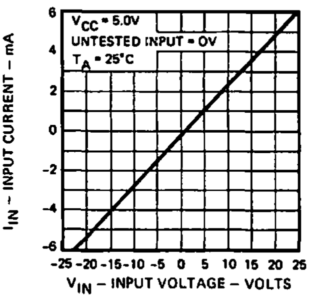
Strobe Input-Output Transfer Characteristic Versus Ambient Temperature



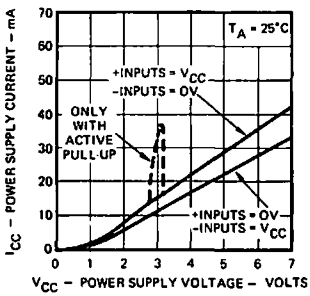
Output Voltage Versus Common Mode Voltage (Am9615)



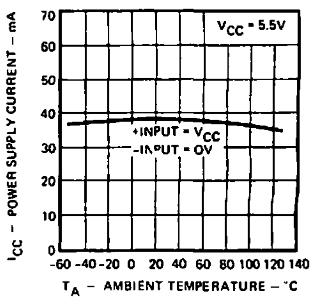
Input Current Versus Input Voltage



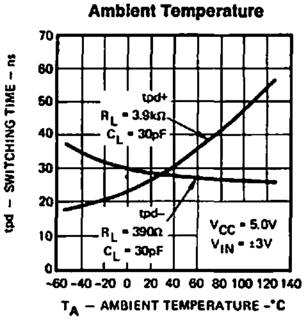
Power Supply Current Versus Power Supply Voltage



Power Supply Current Versus Ambient Temperature



Switching Time Versus Ambient Temperature

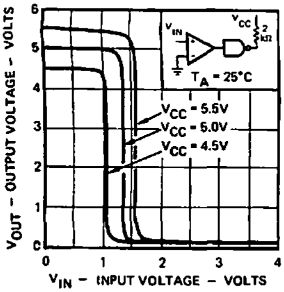


LIC-402

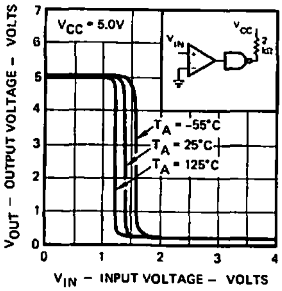
THRESHOLD CHARACTERISTICS

Am2615

Input-Output Transfer Characteristic Versus V_{CC}

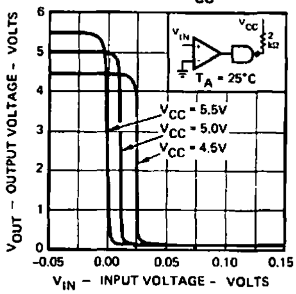


Input-Output Transfer Characteristic Versus Temperature

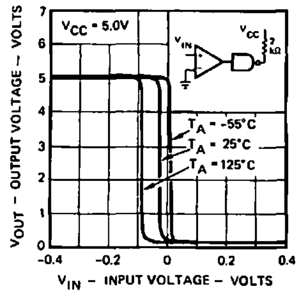


Am9615

Input-Output Transfer Characteristic Versus V_{CC}

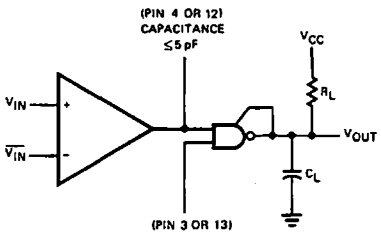


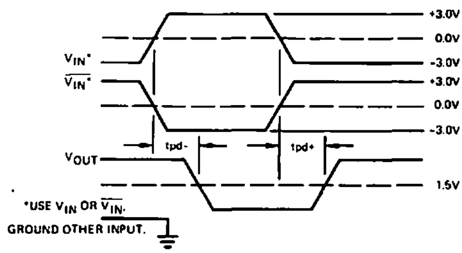
Input-Output Transfer Characteristic Versus Temperature



LIC-403

SWITCHING TIME TEST CIRCUIT & WAVEFORMS



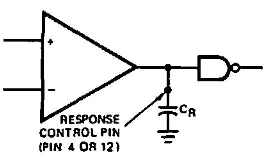


LIC-404

Figure 4

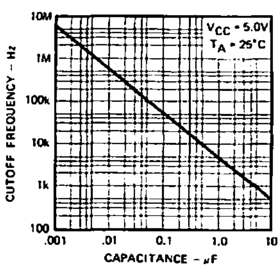
LIC-405

FREQUENCY RESPONSE CONTROL



LIC-406

Frequency Response Versus Capacitance



LIC-407

Am2615/9615 LOADING RULES

	Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
Receiver A	Out	1	—	o/c	10
	Active Pull-Up	2	—	83	—
	Response Control	3	—	—	—
	Strobe	4	1.5	—	—
	+ In	5	0.5	—	—
	130 Ω	6	—	—	—
	– In	7	0.5	—	—
	GND	8	—	—	—
Receiver B	– In	9	0.5	—	—
	130 Ω	10	—	—	—
	+ In	11	0.5	—	—
	Response Control	12	—	—	—
	Strobe	13	1.5	—	—
	Active Pull-Up	14	—	83	—
	Out	15	—	o/c	10
	V_{CC}	16	—	—	—

Am2615 STANDARD USAGE

**Single-Ended-Back Matched Operation
With Common Ground**

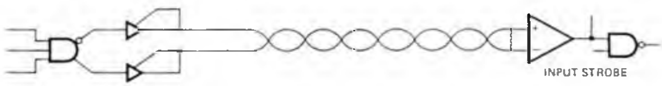
½ Am2614 | Am2615

LIC-408

Am9615 STANDARD USAGE

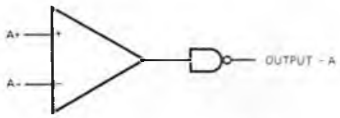
Differential Operation

½ Am9614 | ½ Am9615



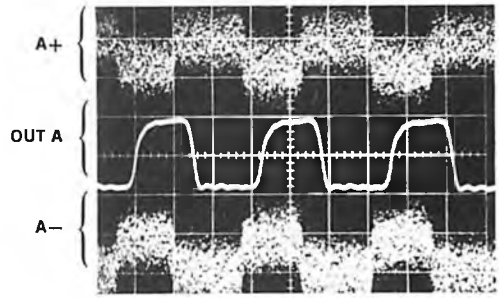
LIC-409

Photograph of an Am9615 switching differential data in the presence of high common mode noise.

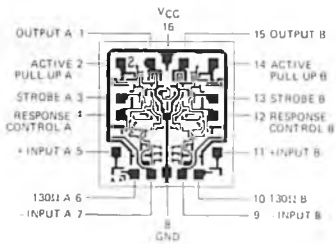


LIC-410

Vertical = 2.0 V/Div. Horizontal = 50 ns/Div.



Metallization and Pad Layout



53 X 58 Mils

Am2616

Quad MIL-188C and RS-232C Line Driver

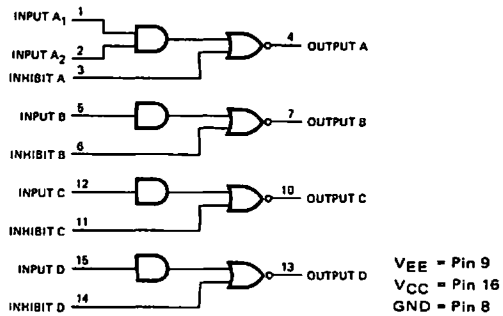
Distinctive Characteristics

- Conforms to EIA RS-232C, CCITT V.24 and MIL-188C specifications
- Short circuit protected output
- Internal slew rate limiting
- Supply independent output swing
- 100% reliability assurance testing in compliance with MIL-STD-883
- TTL/DTL compatible input

FUNCTIONAL DESCRIPTION

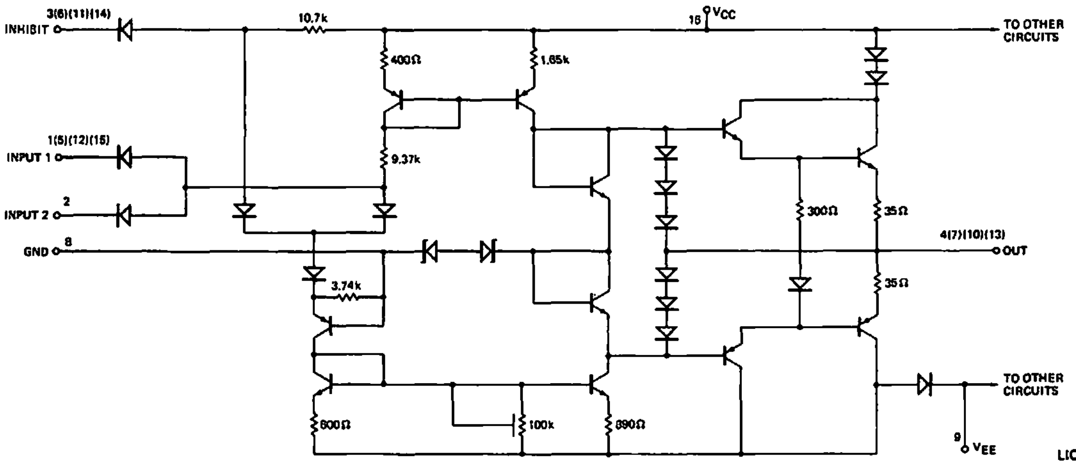
The Am2616 is a quad line driver specifically designed to meet the EIA RS-232C, CCITT V.24 and MIL-188C interface requirements. Each driver accepts DTL/TTL logic levels and converts them to the requisite levels for data transmission between equipment. The output slew rate of each driver is internally limited, but can be lowered by an external capacitor. All outputs are short circuit protected, and protected against fault conditions specified in RS-232C. A HIGH logic level on the inhibit input forces the driver output to V_{OL} or mark state. For 188C interface the output impedance is guaranteed to be less than 100 ohms and the positive and negative output voltage amplitudes are guaranteed to be within 10 percent of each other.

LOGIC SYMBOL



LIC-411

CIRCUIT DIAGRAM
(One Driver Shown)

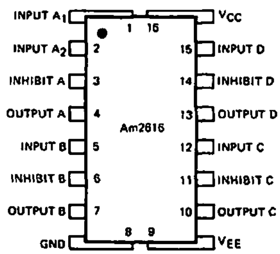


LIC-412

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +75°C	AM2616DC
Molded DIP	0°C to +75°C	AM2616PC
Dice	0°C to +75°C	AM2616XC
Hermetic DIP	–55°C to +125°C	AM2616DM
Flat Pack	–55°C to +125°C	AM2616FM
Dice	–55°C to +125°C	AM2616XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-413

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential	
V_{CC}	+15 V
V_{EE}	–15 V
DC Voltage Applied to Outputs	±15 V
DC Input Voltage	–1.5 V to +6 V
Lead Temperature (Soldering, 30 sec.)	300°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

(COM'L) T_A = 0°C to +75°C
(MIL) T_A = –55°C to +125°C
V_{CC} = +12 V ± 10%, V_{EE} = –12 V ± 10%, R_L = 3 kΩ unless otherwise noted

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage (Note 2)	$V_{IN_1} = V_{IN_2} = V_{INHIBIT}$ = 0.8 V	+5.0	+6.0	+7.0	Volts
V_{OL}	Output LOW Voltage (Note 2)	$V_{IN_1} = V_{IN_2} = V_{INHIBIT}$ = 2.0 V	–7.0	–6.0	–5.0	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage			0.8	Volts
I_{IL}	Input LOW Current	$V_{IN_1} = V_{IN_2}$ = 0.4 V or $V_{INHIBIT}$ = 0.4 V		–1.2	–1.6	mA
I_{IH}	Input HIGH Current	$V_{IN_1} = V_{IN_2}$ = 2.4 V or $V_{INHIBIT}$ = 2.4 V			40	μA
I_{SC}	Output Short Circuit Current (Positive) (Note 3)	R_L = 0 Ω V_{IN_1} or $V_{IN_2} = V_{INHIBIT}$ = 0.8 V	–10	–17	–30	mA
I_{SE}	Output Short Circuit Current (Negative) (Note 3)	R_L = 0 Ω V_{IN_1} or $V_{IN_2} = V_{INHIBIT}$ = 2.0 V	+10	+17	+30	mA
I_{CC}	Total Positive Supply Current	$V_{IN_1} = V_{IN_2} = V_{INHIBIT}$ = 0.8 V		19	28	mA
		$V_{IN_1} = V_{IN_2} = V_{INHIBIT}$ = 2.0 V		9.5	17	
I_{EE}	Total Negative Supply Current	$V_{IN_1} = V_{IN_2} = V_{INHIBIT}$ = 0.8 V		0	–2	mA
		$V_{IN_1} = V_{IN_2} = V_{INHIBIT}$ = 2.0 V		–20	–30	

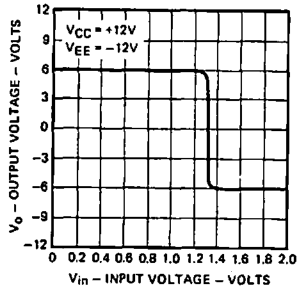
Notes: 1. Typical values are at V_{CC} = 12 V, V_{EE} = –12 V, T_A = 25°C.
2. V_{OH} and V_{OL} are guaranteed to be equal within ±10 percent of each other for MIL-188C operation.(i.e., V_{OH} = 6.0V then V_{OL} = –6.0V ±0.6V).
3. The I_{SC} and I_{SE} minimum limits guarantee the output impedance to be less than 100 ohms.

Switching Characteristics (T_A = 25°C, V_{CC} = +12.0V, V_{EE} = –12.0 V)

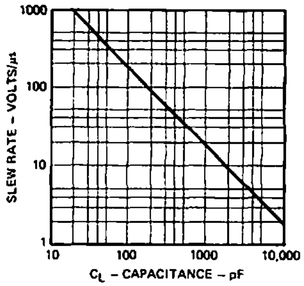
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Delay from Input LOW to Output HIGH	C_L = 15 pF, R_L = ∞		320	650	ns
t_{PHL}	Delay from Input HIGH to Output LOW			320	650	ns
dV/dt (+)	Positive Slew Rate	0 pF < C_L < 2500 pF, R_L > 3 kΩ	4.0	15	30	V/μs
dV/dt(–)	Negative Slew Rate		–30	–15	–4.0	V/μs

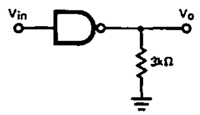
TYPICAL CHARACTERISTICS

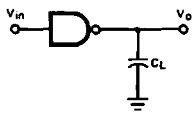
Transfer Characteristics



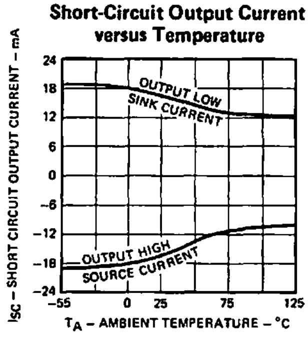
Output Slew Rate versus Load Capacitance



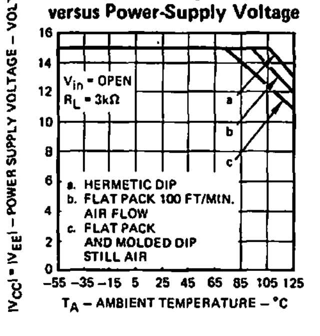




Short-Circuit Output Current versus Temperature



Maximum Operating Temperature versus Power-Supply Voltage



LIC-414

DEFINITION OF TERMS

FUNCTIONAL TERMS

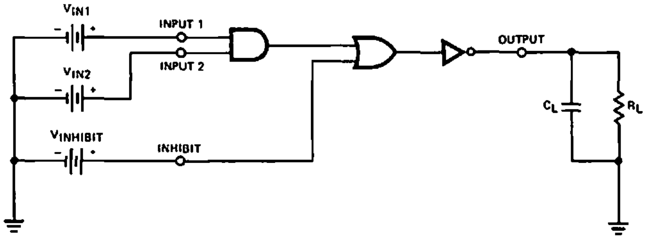
RS-232C A specification of the Electronic Industries Association that defines the electrical characteristics of data signals transmitted between two pieces of digital equipment.

R_L Load resistance. The DC resistance between the driver output and ground.

MIL-188C A Military specification that defines the electrical interface and characteristics of data signals transmitted between two pieces of digital equipment.

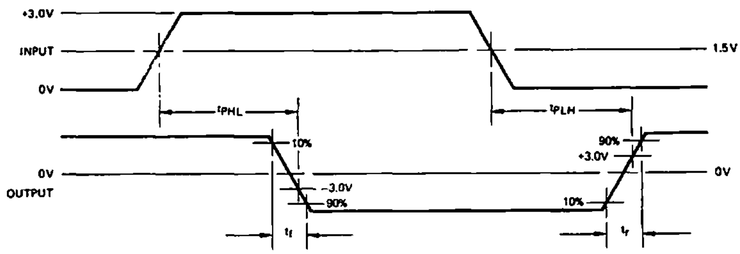
CCITT V.24 A European specification similar to the MIL-188C and RS-232 specifications.

SWITCHING TEST CIRCUIT & VOLTAGE WAVEFORMS



LIC-415

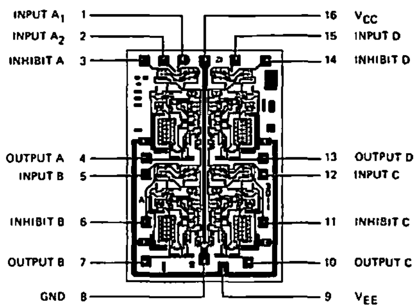
Note: Omit V_{IN2} for channels B, C and D.



LIC-416

Pulse Generator Rise Time = 10 ± 5ns.

Metallization and Pad Layout



DIE SIZE
0.069" X 0.103"

Am2617

Quad RS-232C Line Receiver

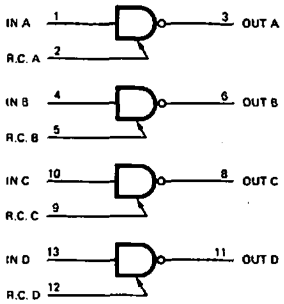
Distinctive Characteristics

- Full military temperature range
- Compatible with EIA specification RS-232C
- Input signal range ± 30 volts
- Guaranteed input thresholds over full military temperature range
- 100% reliability assurance testing in compliance with MIL-STD-883
- Includes response control input and built-in hysterisis

FUNCTIONAL DESCRIPTION

The Am2617 is a quad line receiver whose electrical characteristics conform to EIA specification RS-232C. Each receiver has a single data input that can accept signal swings of up to ±30V. The output of each receiver is TTL/DTL compatible, and includes a 2kΩ resistor pull-up to V_{CC}. An internal feedback resistor causes the input to exhibit hysterisis so that AC noise immunity is maintained at a high level even near the switching thresholds. For example, at 25°C when a receiver is in a LOW state on the output, the input may drop as LOW as 1.25 volts without affecting the output. The device is guaranteed to switch to the HIGH state when the input voltage is below 0.75V. Once the output has switched to the HIGH state, the input may rise to 1.75V without causing a change in the output. The Am2617 is guaranteed to switch to a LOW output when its input reaches 2.25V. Because of this hysterisis in switching thresholds, the device can receive signals with superimposed noise or with slow rise and fall times without generating oscillations on the output. The threshold levels may be offset by a constant voltage by applying a DC bias to the response control input. A capacitor added to the response control input will reduce the frequency response of the receiver for applications in the presence of high frequency noise spikes. The companion line driver is the Am2616.

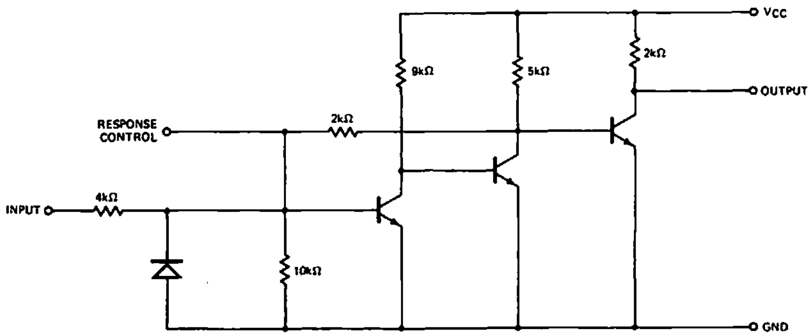
LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LIC-417

CIRCUIT DIAGRAM
(One Receiver)

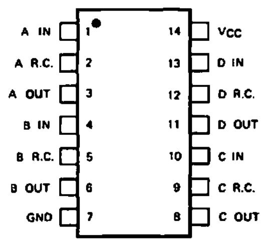


LIC-418

ORDERING INFORMATION

	Temperature Range	Order Number
Molded DIP	0°C to +75°C	AM2617PC
Hermetic DIP	0°C to +75°C	AM2617DC
Dice	0°C to +75°C	AM2617XC
Hermetic DIP	–55°C to +125°C	AM2617DM
Hermetic Flat Pack	–55°C to +125°C	AM2617FM
Dice	–55°C to +125°C	AM2617XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-419

4

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +175°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous	−0.5 V to +10 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to $+V_{CC}$ max.
Input Signal Range	−30 V to +30 V
Output Current, Into Outputs	30 mA
DC Input Current	Defined by Input Voltage Limits

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

T_A = 0°C to +75°C V_{CC} = 5.0 V ± 5%
T_A = −55°C to +125°C V_{CC} = 5.0 V ± 10%
} Response control pin open.

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −0.5 mA, V_{IN} = 0.4 V or open	2.4	4.0		Volts
V_{OL}	Output LOW Voltage	I_{OL} = 10 mA, V_{IN} = 3.0 V		0.2	0.45	Volts
I_{IL}	Input LOW Current	V_{IN} = −3.0 V	−0.43			mA
		V_{IN} = −25 V	−3.6		−8.3	
I_{IH}	Input HIGH Current	V_{IN} = +3.0 V	0.43			mA
		V_{IN} = +25 V	3.6		8.3	
I_{SC}	Output Short Circuit Current	V_{IN} = 0.0 V, V_{OUT} = 0.0 V	1.9	2.5	3.8	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		20	26	mA

Note 1. Typical Limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.

Threshold Characteristics (Note 2)

Parameters	Description	Test Conditions	T_A	Min.	Typ. (Note 1)	Max.	Units
V_{T+}	Positive-Going Threshold Voltage	V_{OL} = 0.45V, V_{CC} = 5.0V	−55°C	2.3		3.1	Volts
			0°C	1.9		2.5	
			25°C	1.75	2.0	2.25	
			75°C	1.45		1.90	
			125°C	1.20		1.65	
V_{T-}	Negative-Going Threshold Voltage	V_{OH} = 2.5V, V_{CC} = 5.0V	−55°C	0.85		1.65	Volts
			0°C	0.75		1.40	
			25°C	0.75	0.95	1.25	
			75°C	0.60		1.10	
			125°C	0.50		0.95	

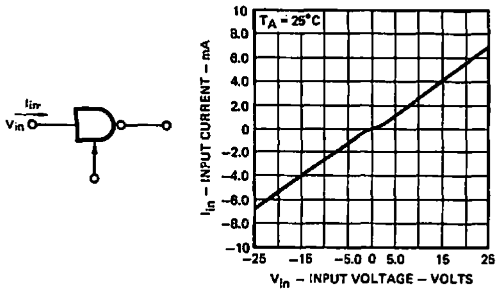
Notes: 1. Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. The input threshold margin for the device is greater than the voltage computed as the $V_{T+}-V_{T-}$ value. For the minimum value see the input threshold margin versus temperature graph.

Switching Characteristics (T_A = 25°C, response control pin open, C_L = 15 pF)

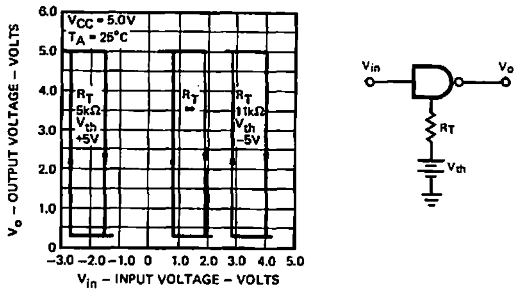
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Delay from Input LOW to Output HIGH	R_L = 3.9 kΩ		25	85	ns
t_{PHL}	Delay from Input HIGH to Output LOW	R_L = 390 Ω		25	50	ns
t_r	Output Rise Time (10% to 90%)	R_L = 3.9 kΩ		120	175	ns
t_f	Output Fall Time (90% to 10%)	R_L = 390 Ω		10	20	ns

TYPICAL CHARACTERISTICS

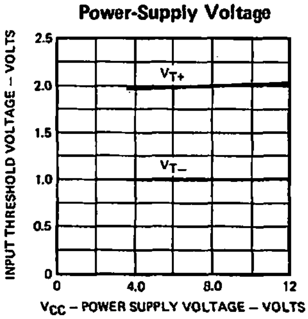
Input Current



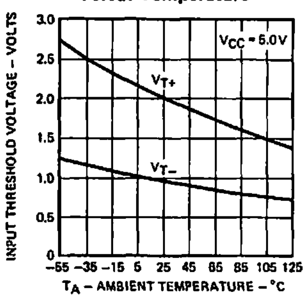
Input Threshold Voltage Adjustment



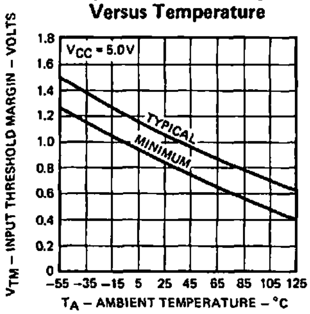
Input Threshold Versus Power-Supply Voltage



Input Threshold Voltage Versus Temperature



Input Threshold Margin Versus Temperature



LIC-420

DEFINITION OF TERMS

FUNCTIONAL TERMS

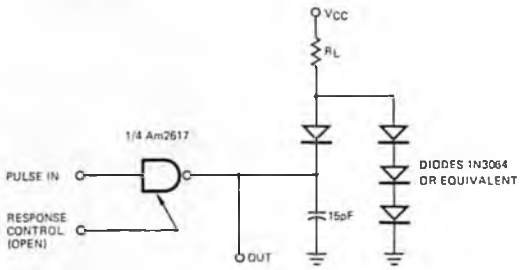
Response Control Pin A pin available on each receiver that allows the user to set the switching thresholds and frequency response of the receiver.

Threshold Voltage The voltage level on the input that will cause the output to change state. Because the device exhibits hysterisis, the LOW level input threshold is different from the HIGH level input threshold. Both thresholds can be moved by applying a bias to the response control pin.

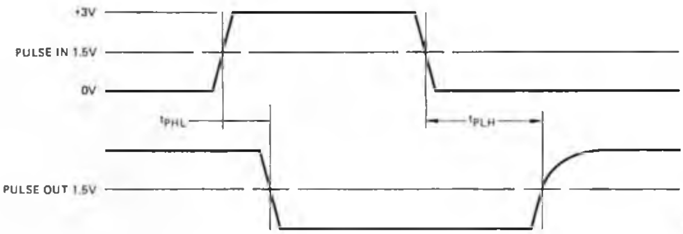
RS-232C A specification of the Electronic Industries Association that defines the electrical characteristics of data signals transmitted between two pieces of digital equipment.

Input Signal Range The permitted range of DC voltages that can be applied to the receiver input without damage to the device.

SWITCHING TIME TEST CIRCUIT & WAVEFORMS

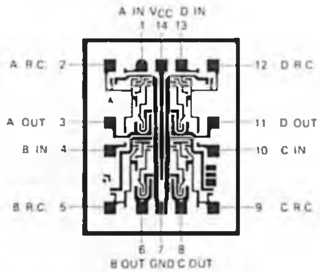


LIC-421



LIC-422

Metallization and Pad Layout



DIE SIZE 0.047" X 0.059"

Am2905

Quad Two-Input OC Bus Transceiver With Three-State Receiver

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 100 mA at 0.8V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

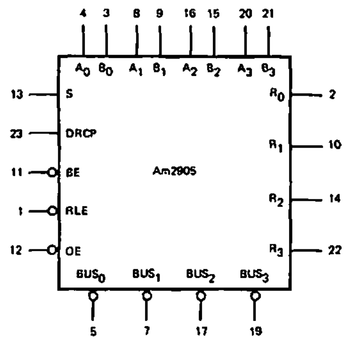
The Am2905 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

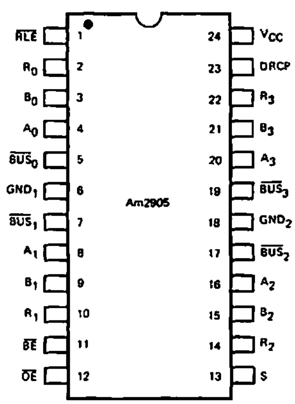
LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

MPR-063

CONNECTION DIAGRAM
Top View

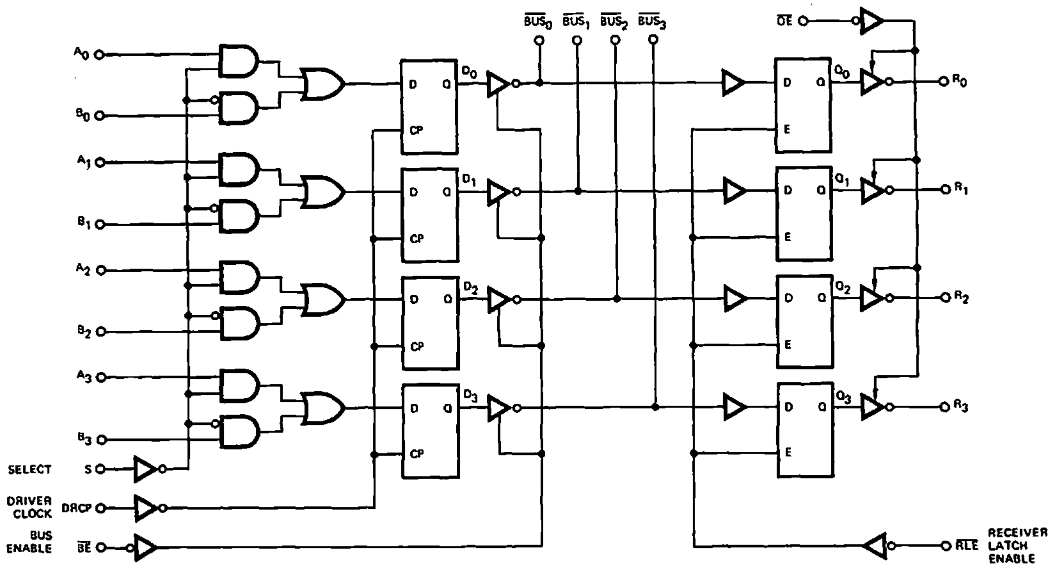


Note: Pin 1 is marked for orientation.

MPR-064

4

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential	–0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	–0.5V to $+V_{CC}$ max.
DC Input Voltage	–0.5V to +7V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	200mA
DC Input Current	–30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V
Am2905XM (MIL) T_A = –55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				–50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2905XM MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

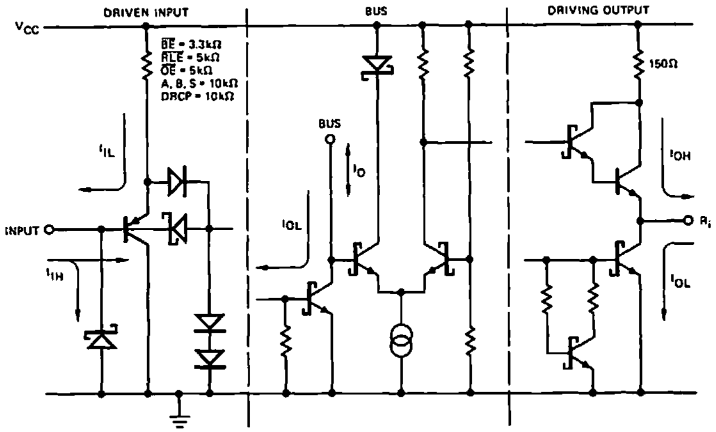
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	$V_{CC} = V_{IN}$, $V_{IN} = V_{IL}$ or V_{IH}	MIL, $I_{OH} = -1.0mA$	2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$	2.4	3.4		
V_{OL}	Receiver Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4mA$		0.27	0.4	Volts
			$I_{OL} = 8mA$		0.32	0.45	
			$I_{OL} = 12mA$		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5V$				100	μA
I_O	Receiver Off-State Output Current	V_{CC} = MAX.	$V_O = 2.4V$			20	μA
			$V_O = 0.4V$			−20	
I_{SC}	Receiver Output Short Circuit Current	V_{CC} = MAX.		−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND			69	105	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2905XM			Am2905XC			Units
			Min.	Typ. (Note 2)	Max.	Min.	Typ. (Note 2)	Max.	
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs (A or B)	C_L = 15pF, R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_s	Select Input (S)		33			30			ns
t_h			8.0			7.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{ZH}	Output Control to Receiver Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Receiver Output			14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

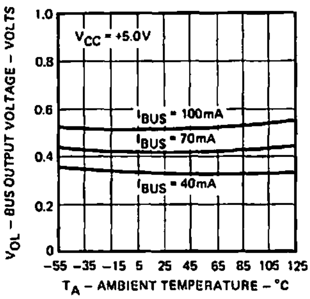


Note: Actual current flow direction shown.

MPR-066

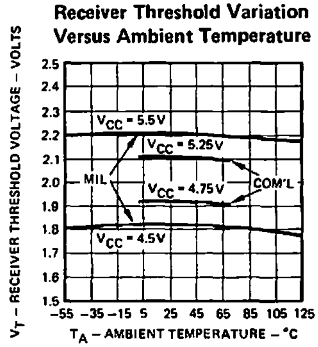
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



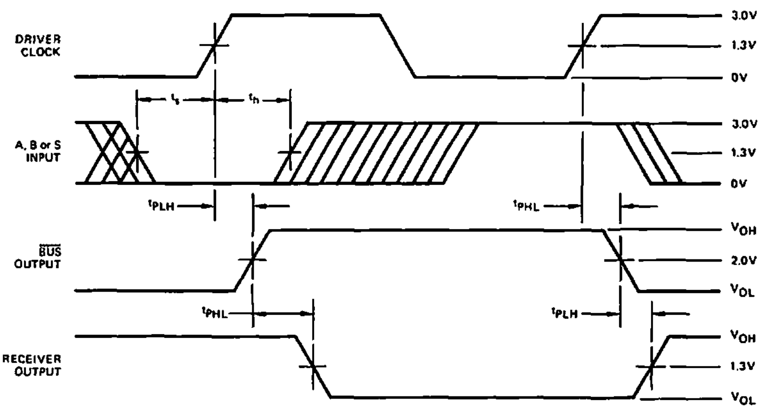
MPR-067

Receiver Threshold Variation Versus Ambient Temperature



MPR-068

SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

MPR-069

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2905PC	P-24	C	C-1
AM2905DC	D-24	C	C-1
AM2905DC-B	D-24	C	B-1
AM2905DM	D-24	M	C-3
AM2905DM-B	D-24	M	B-3
AM2905FM	F-24	M	C-3
AM2905FM-B	F-24	M	B-3
AM2905XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2905XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

4

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

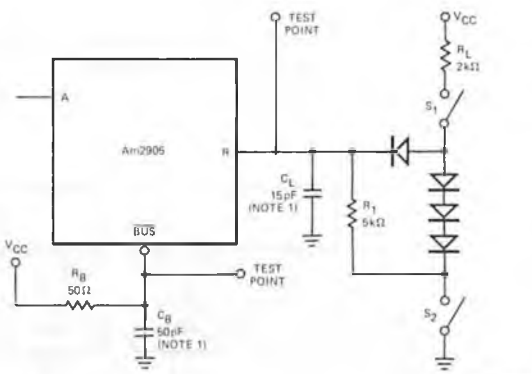
$\overline{BUS}_0, \overline{BUS}_1, \overline{BUS}_2, \overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

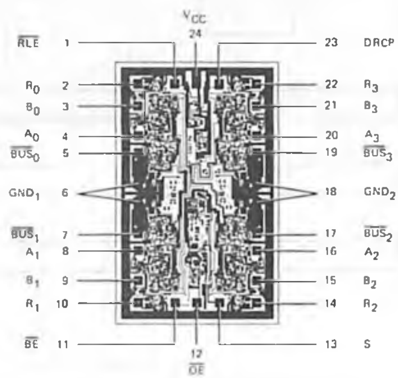
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

LOAD TEST CIRCUIT



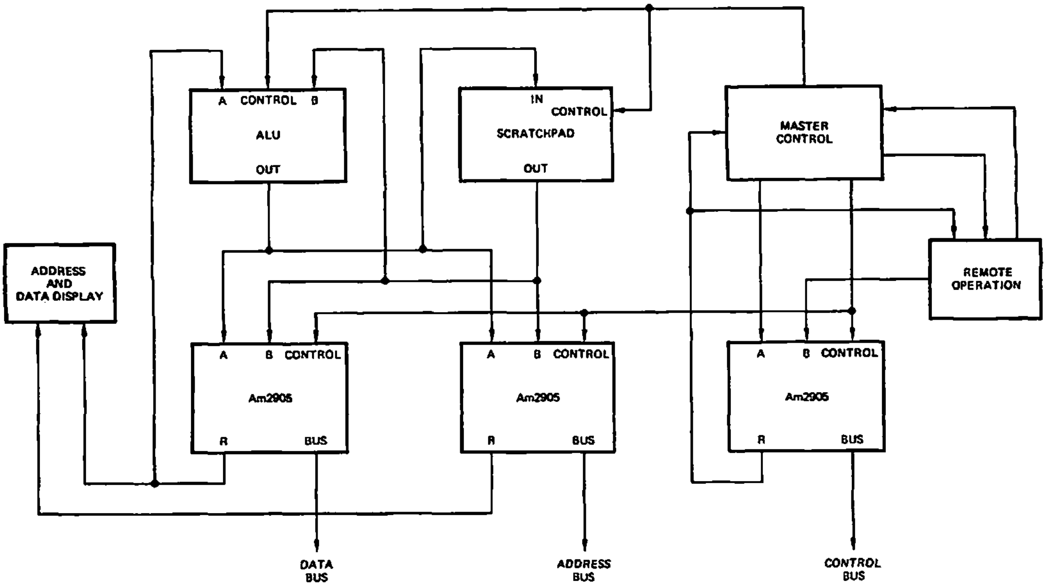
MPR-070

Metallization and Pad Layout



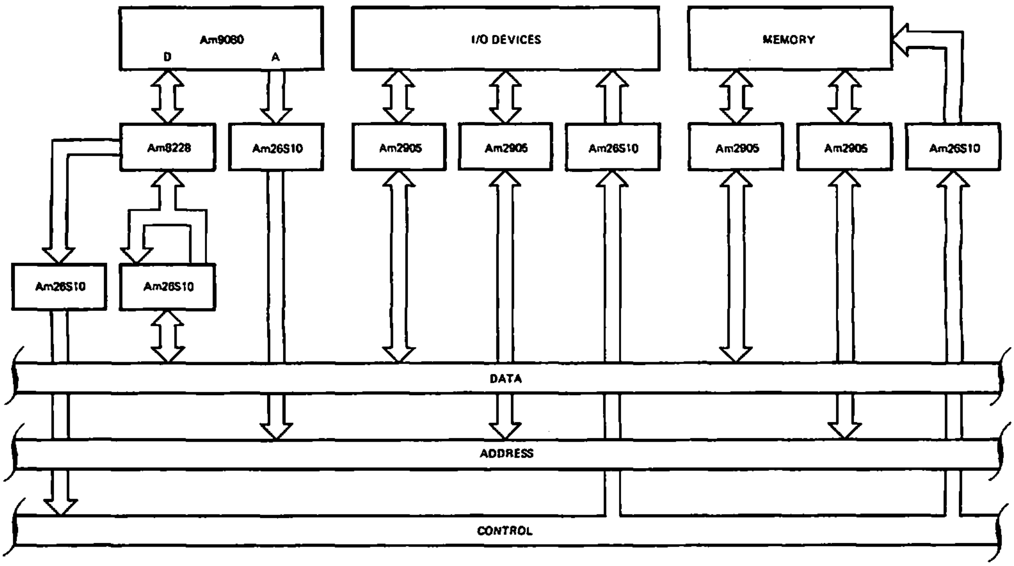
DIE SIZE 0.080" X 0.130"

APPLICATIONS



The Am2905 is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.

MPR-071



Using the Am2905 and Am26S10 in a terminated Bus system for the Am9080 MOS Microprocessor.

MPR-072

Am2906

Quad Two-Input OC Bus Transceiver With Parity

Distinctive Characteristics

- Quad high-speed LSI bus transceiver.
- Open-collector bus driver.
- Two-port input to D-type register on driver.
- Bus driver output can sink 100 mA at 0.8V max.
- Internal odd 4-bit parity checker/generator.
- Receiver has output latch for pipeline operation.
- Receiver outputs sink 12 mA.
- Advanced low-power Schottky processing.
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am2906 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

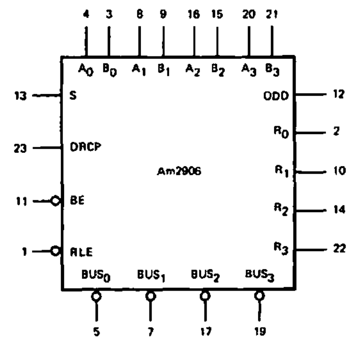
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2906 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

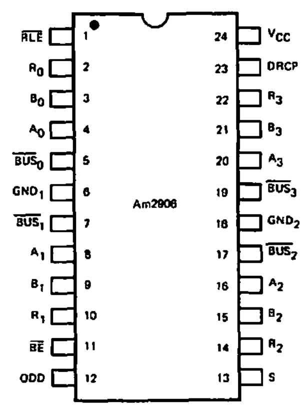
LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

MPR-073

CONNECTION DIAGRAM
Top View

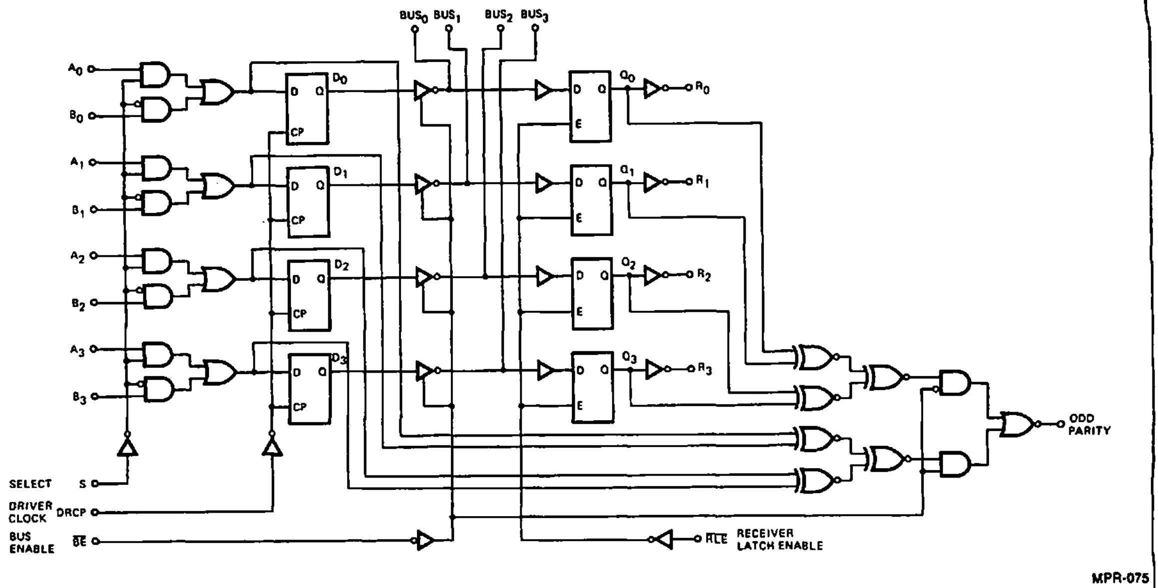


Note: Pin 1 is marked for orientation.

MPR-074

4

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential	–0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	–0.5V to $+V_{CC}$ max.
DC Input Voltage	–0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	200mA
DC Input Current	–30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2906XC (COM'L)	T_A = 0°C to +70°C	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2906XM (MIL)	T_A = –55°C to +125°C	V_{CC} MIN. = 4.50V	V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage		I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				–50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2906XC (COM'L)	T_A = 0°C to +70°C	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2906XM (MIL)	T_A = −55°C to +125°C	V_{CC} MIN. 4.5V	V_{CC} MAX. = 5.5V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

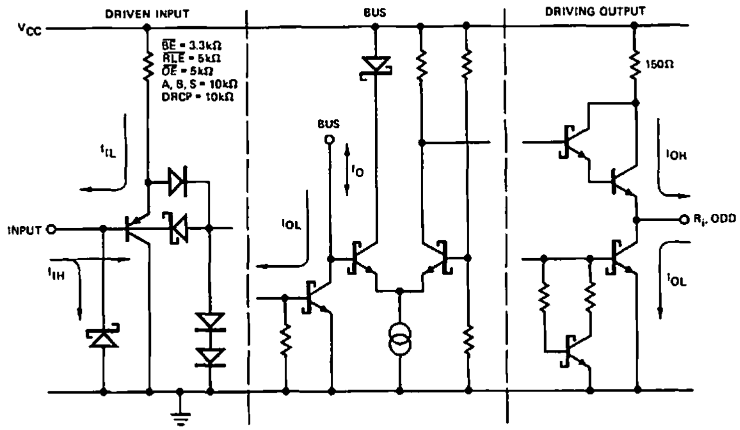
Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IL} or V_{IH}	MIL	I_{OH} = −1mA	2.4	3.4		Volts
			COM'L	I_{OH} = −2.6mA	2.4	3.4		
	Parity Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −660μA V_{IN} = V_{IH} or V_{IL}		MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN. V_{IN} = V_{IL} or V_{IH}	I_{OL} = 4mA			0.27	0.4	Volts
			I_{OL} = 8mA			0.32	0.45	
			I_{OL} = 12mA			0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4V					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7V					20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 5.5V					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND				72	105	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2906XM Min.	Am2906XM Typ. (Note 2)	Am2906XM Max.	Am2906XC Min.	Am2906XC Typ. (Note 2)	Am2906XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs (A or B)	C_L = 15pF R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_s	Select Inputs (S)		33			30			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

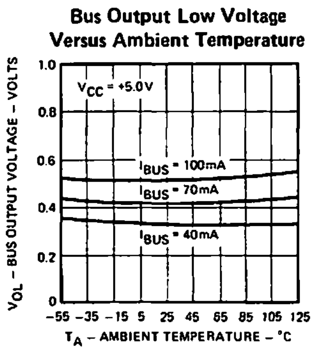
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



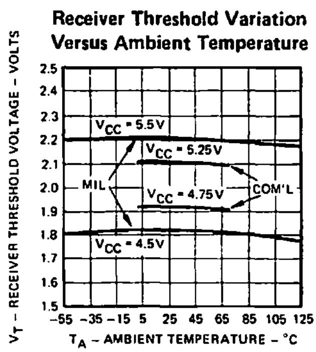
Note: Actual current flow direction shown.

MPR-076

TYPICAL PERFORMANCE CURVES

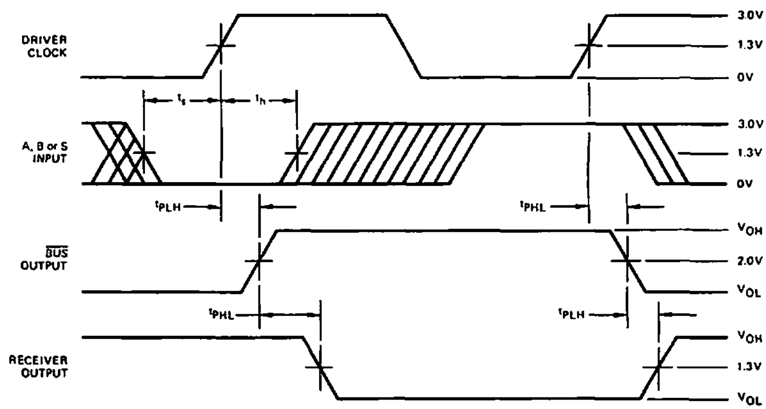


MPR-077



MPR-078

SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

MPR-079

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS_i}$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2906PC	P-24	C	C-1
AM2906DC	D-24	C	C-1
AM2906DC-B	D-24	C	B-1
AM2906DM	D-24	M	C-3
AM2906DM-B	D-24	M	B-3
AM2906FM	F-24	M	C-3
AM2906FM-B	F-24	M	B-3
AM2906XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2906XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

4

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

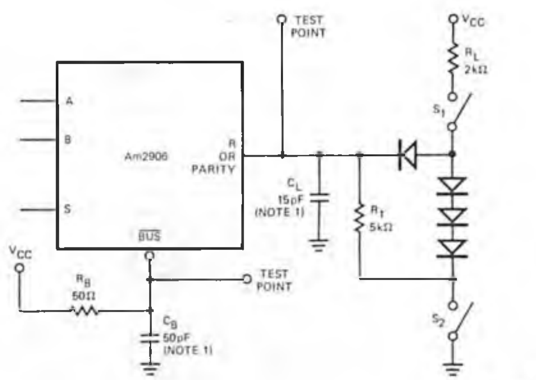
$\overline{BUS_0}, \overline{BUS_1}, \overline{BUS_2}, \overline{BUS_3}$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

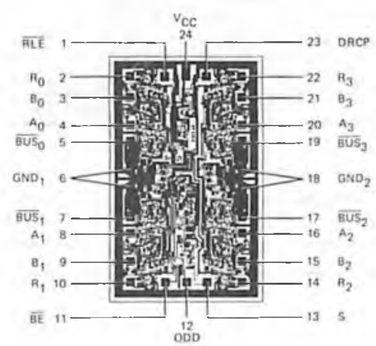
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

LOAD TEST CIRCUIT



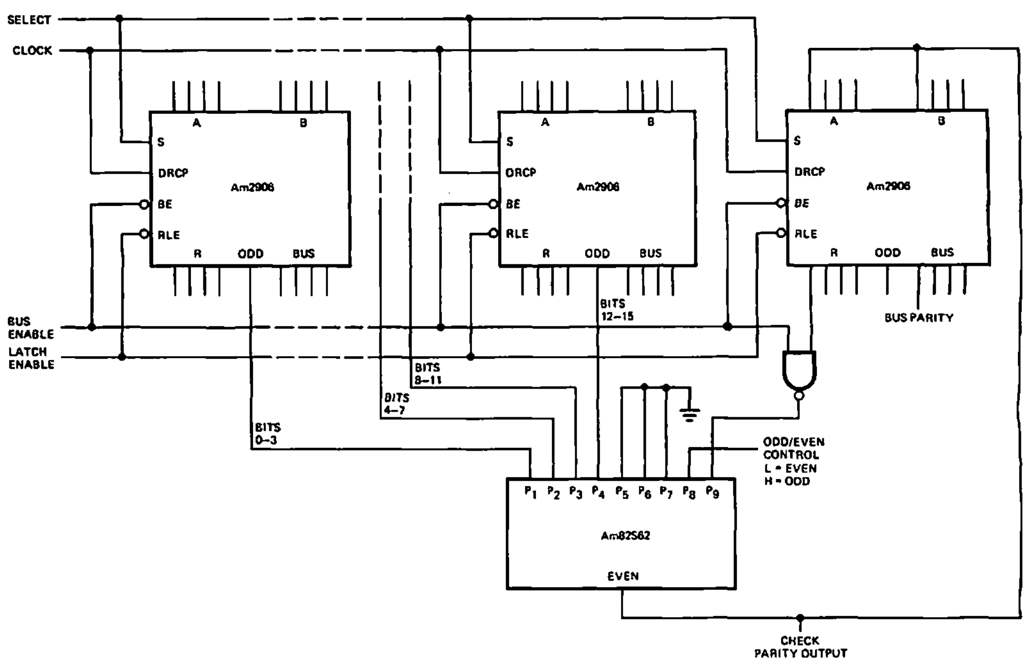
MPR-080

Metallization and Pad Layout



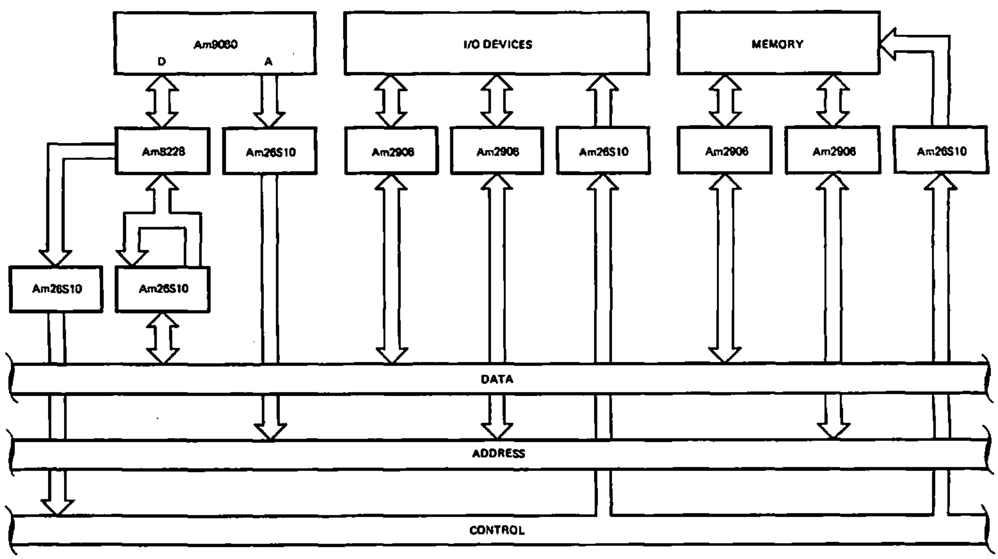
DIE SIZE 0.080" X 0.130"

APPLICATIONS



Generating or checking parity for 16 data bits.

MPR-081



Using the Am2906 and Am26S10 in a terminated Bus system for the Am9080 MOS Microprocessor.

MPR-082

Am2907 • Am2908

Quad Bus Transceivers with Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- D-type register on driver
- Bus driver output can sink 100mA at 0.8V max.
- Internal odd 4-bit parity checker/generator
- Am2907 has 2.0V input receiver threshold; Am2908 is "DEC Q or LSI-II bus compatible" with 1.5V receiver threshold
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced Low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2907 and Am2908 are high-performance bus transceivers intended for bipolar or MOS microprocessor system applications. The Am2908 is Digital Equipment Corporation "Q or LSI-II bus compatible" while the Am2907 features a 2.0V receiver threshold. These devices consist of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches, that feature three-state outputs. The devices also contain a four-bit odd parity checker/generator.

These LSI bus transceivers are fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

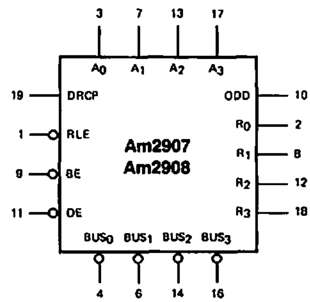
The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted form driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2907 and Am2908 feature a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

The Am2907 has receiver threshold typically of 2.0V while the Am2908 threshold is typically 1.5V.

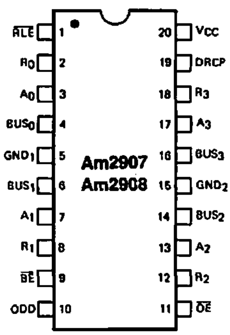
LOGIC SYMBOL



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

MPR-083

CONNECTION DIAGRAM
Top View



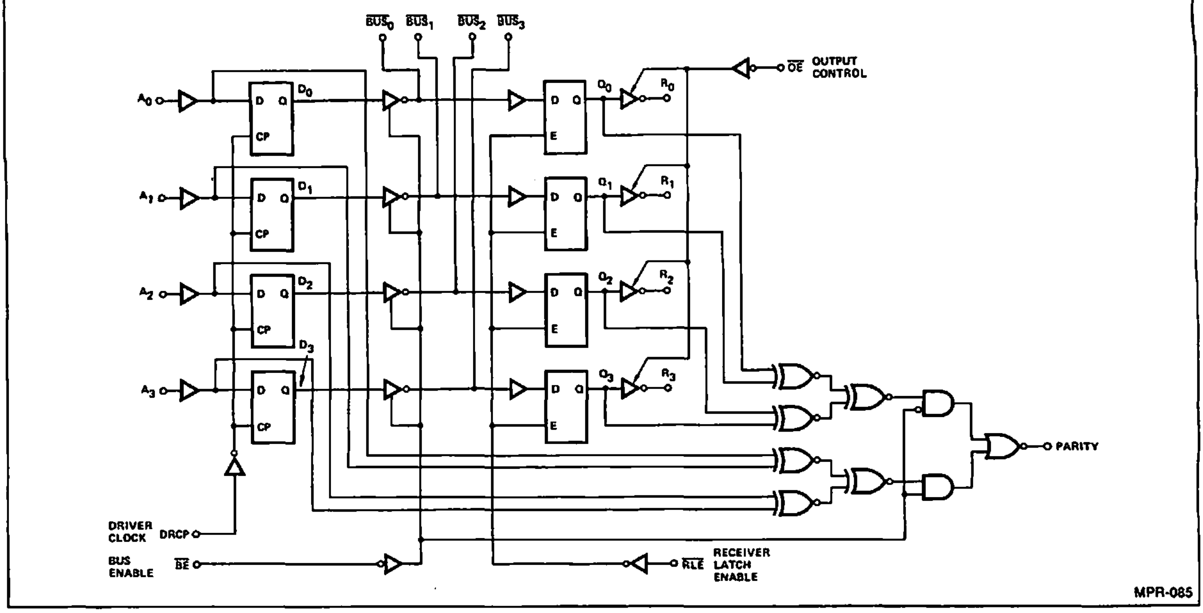
Note: Pin 1 is marked for orientation.

MPR-084

ORDERING INFORMATION

Package Type	Temperature Range	Am2907 Order Number	Am2908 Order Number
Molded DIP	0°C to +70°C	AM2907PC	AM2908PC
Hermetic DIP	0°C to +70°C	AM2907DC	AM2908DC
Dice	0°C to +70°C	AM2907XC	AM2908XC
Hermetic DIP	−55°C to +125°C	AM2907DM	AM2908DM
Hermetic Flat Pak	−55°C to +125°C	AM2907FM	
Dice	−55°C to +125°C	AM2907XM	

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential	–0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	–0.5 V to +V_{CC} max.
DC Input Voltage	–0.5 V to +5.5 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	200 mA
DC Input Current	–30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC, Am2908XC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2907XM, Am2908XM (MIL) T_A = –55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O 4 0.4V				–50	µA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	µA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V	Am2907	MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
			Am2908	MIL	1.9	1.5		
				COM'L	1.7	1.5		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V	Am2907	MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	
			Am2908	MIL		1.5	1.1	
				COM'L		1.5	1.3	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = –18mA					–1.2	Volts

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC, Am2908XC (COM'L)	T_A = 0°C to +70°C	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2907XM, Am2908XM (MIL)	T_A = −55°C to +125°C	V_{CC} MIN. = 4.50V	V_{CC} MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IL} or V_{IH}	MIL: I_{OH} = −1mA	2.4	3.4		Volts
			COM'L: I_{OH} = −2.6mA	2.4	3.4		
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −660μA V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN. V_{IN} = V_{IL} or V_{IH}	I_{OL} = 4mA		0.27	0.4	Volts
			I_{OL} = 8mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4 V				−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 5.5 V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND			75	110	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4 V			20	μA
			V_O = 0.4 V			−20	

Am2907 SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2907XM Min.	Am2907XM Typ. (Note 2)	Am2907XM Max.	Am2907XC Min.	Am2907XC Typ. (Note 2)	Am2907XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs	C_L = 15pF, R_L = 2.0kΩ	18			15			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	Data to Odd Parity Out (Driver Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{ZH}	Output Control to Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Output	C_L = 5.0pF, R_L = 2.0kΩ		14	28		14	25	ns
t_{LZ}				14	28		14	25	

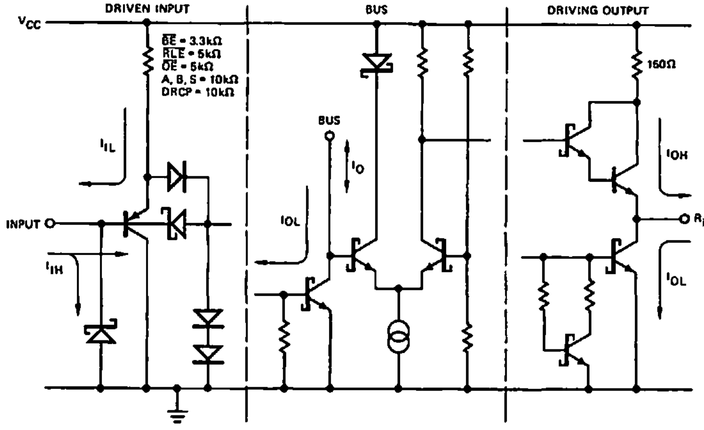
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Am2908 SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2908XM Min.	Am2908XM Typ. (Note 2)	Am2908XM Max.	Am2908XC Min.	Am2908XC Typ. (Note 2)	Am2908XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L(BUS) = 50pF R_L(BUS): 91Ω to V_{CC} 200Ω to GND		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_r	Bus Output Rise Time		5	10		7	10		ns
t_f	Bus Output Fall Time		3	6		4	6		
t_s	Data Inputs		18			15			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)	C_L = 50pF R_L = 2.0kΩ		18	38		18	35	ns
t_{PHL}				18	38		18	35	
t_{PLH}	Latch Enable to Receiver Output			21	38		21	35	ns
t_{PHL}				21	38		21	35	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	Data to Odd Parity Out (Driver Enabled)	C_L = 15pF R_L = 2.0kΩ		21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{ZH}	Output Control to Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Output	C_L = 5.0pF R_L = 2.0kΩ		14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics fo the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

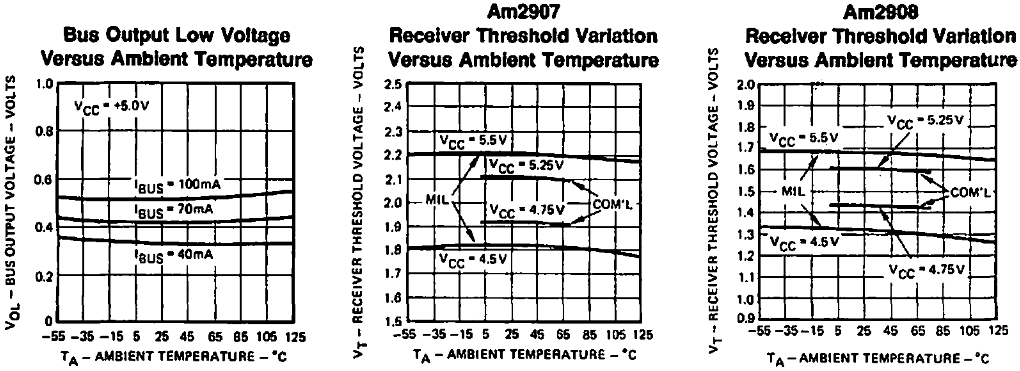
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

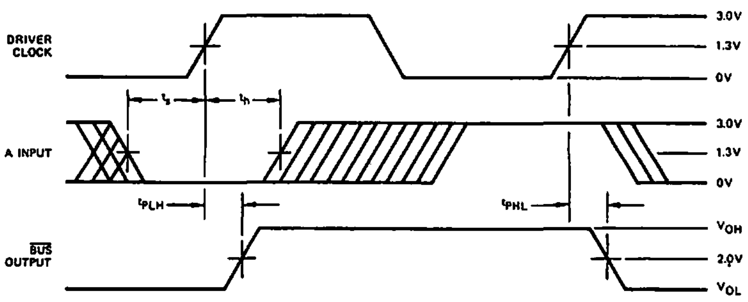
MPR-086

TYPICAL PERFORMANCE CURVES



MPR-087 MPR-088 MPR-508

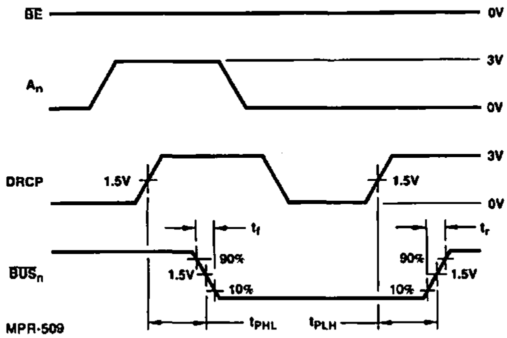
Am2907/08 SWITCHING WAVEFORMS



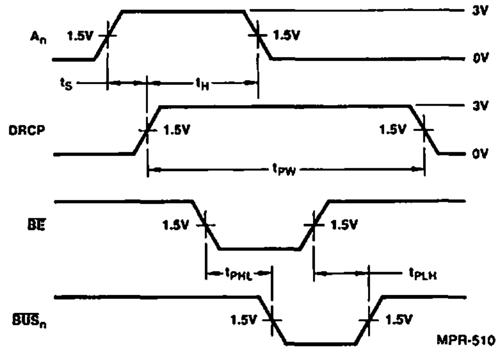
1. INPUT SET-UP AND HOLD TIMES.

MPR-089

Am2907/08 SWITCHING WAVEFORMS AND LOAD TEST CIRCUITS

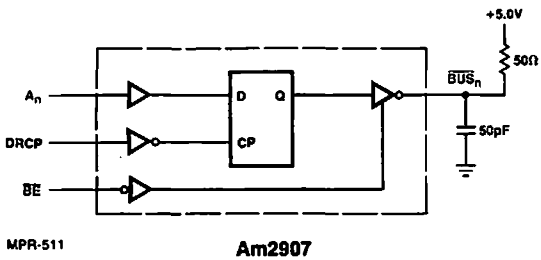


2. DRIVER CLOCK (DRCP) TO BUS

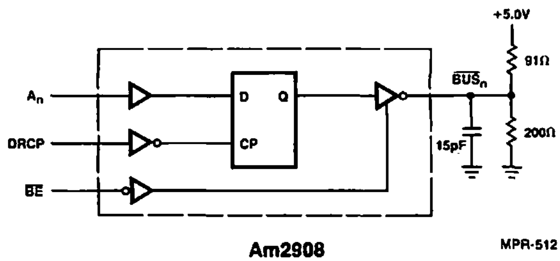


3. BUS ENABLE ($\overline{BE}$) TO BUS

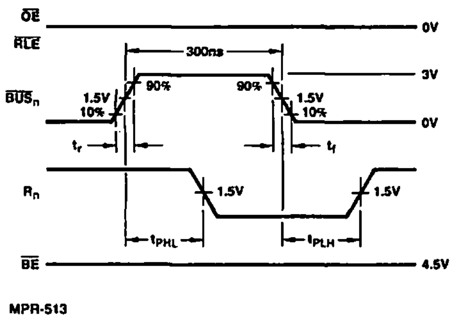
DRIVER SWITCHING WAVEFORMS



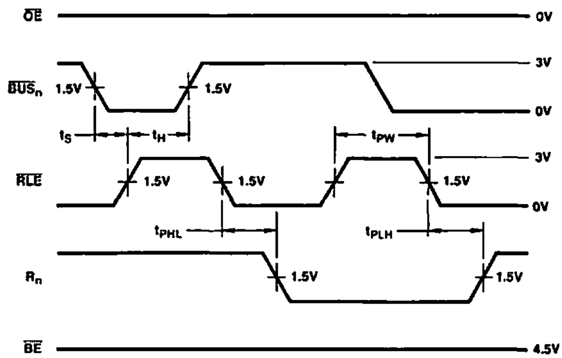
Am2907
DRIVER LOAD TEST CIRCUIT



Am2908
DRIVER LOAD TEST CIRCUIT



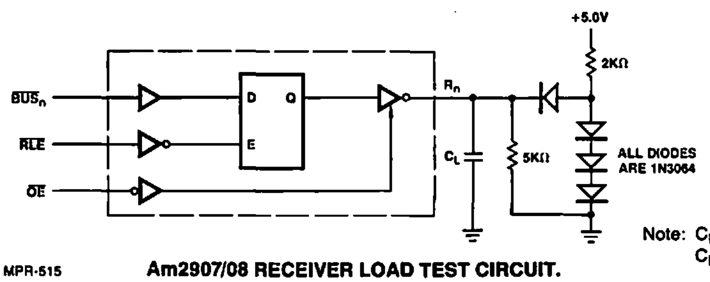
4. BUS TO RECEIVER OUTPUT (LATCH ENABLED)



5. LATCH ENABLE TO OUTPUT

MPR-514

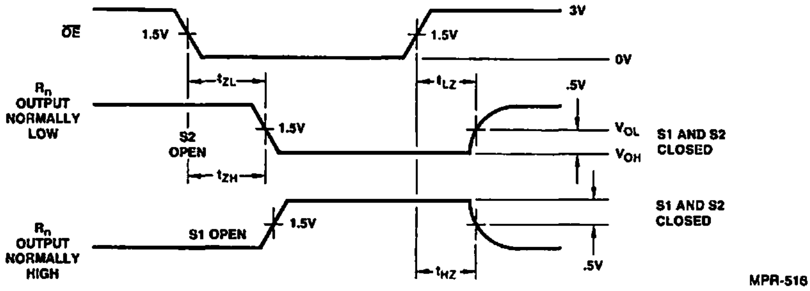
RECEIVER SWITCHING WAVEFORMS



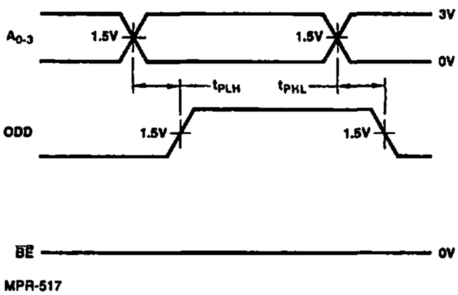
Note: C_L = 15pF for Am2907
C_L = 50pF for Am2908

Am2907/08 RECEIVER LOAD TEST CIRCUIT.

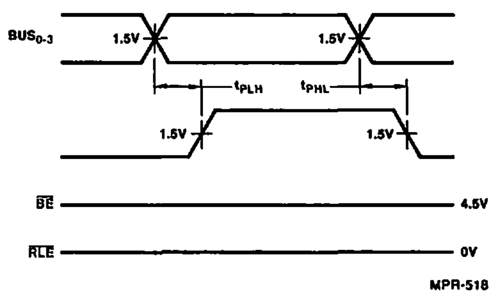
Am2907/08 SWITCHING WAVEFORMS AND LOAD TEST CIRCUITS (Cont.)



6. RECEIVER TRI-STATE WAVEFORMS

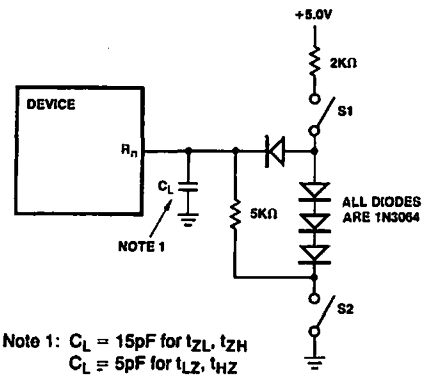


7. A INPUT TO PARITY OUTPUT



8. BUS TO PARITY OUTPUT

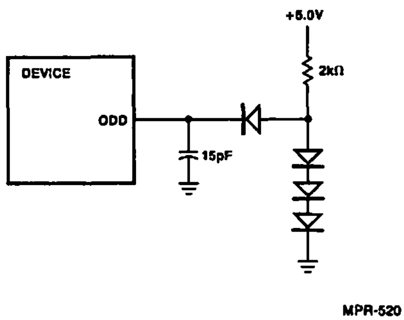
ODD PARITY OUTPUT WAVEFORMS



Note 1: C_L = 15pF for t_{ZL}, t_{ZH}
C_L = 5pF for t_{LZ}, t_{HZ}

MPR-519

LOAD FOR RECEIVER TRI-STATE TEST



LOAD FOR PARITY OUTPUT

TRUTH TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	B_i	R_i	
X	X	H	X	X	X	X	H	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = High Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

DEFINITION OF FUNCTIONAL TERMS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is LOW, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

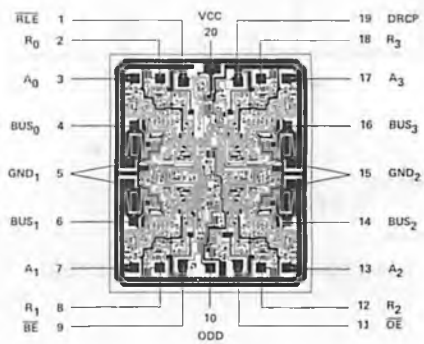
R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

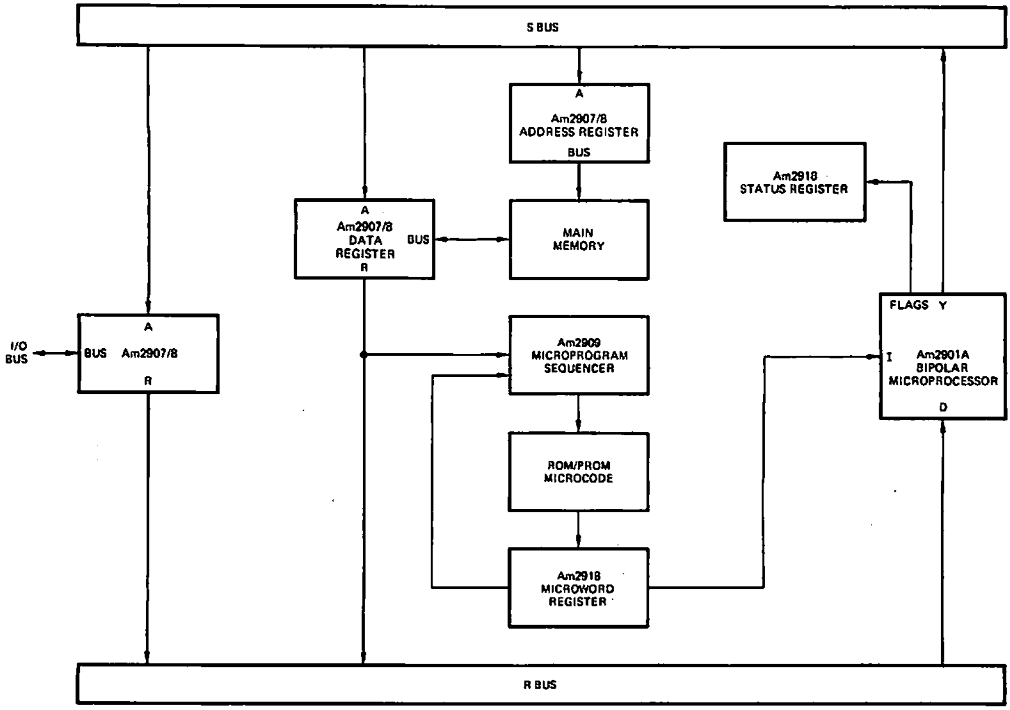
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

Metallization and Pad Layout



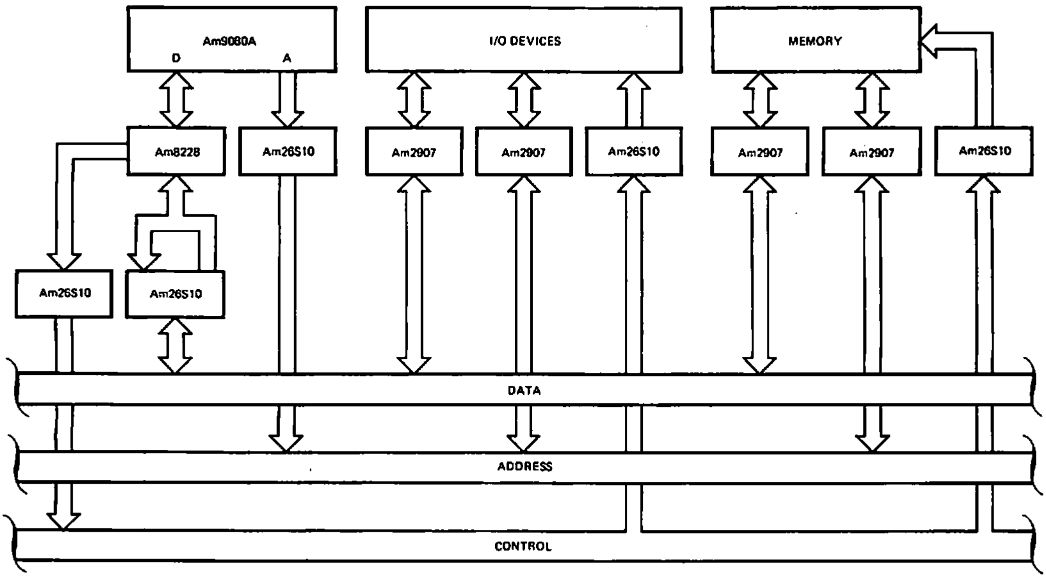
DIE SIZE 0.088" X 0.103"

APPLICATIONS



The Am2907 can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

MPR-091



Using the Am2907 and Am26S10 in a terminated Bus system for the Am9080 MOS Microprocessor.

MPR-092

Am2915A

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

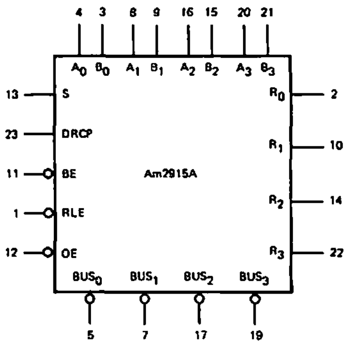
The Am2915A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input (BE) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The V_{OH} and V_{OL} of the bus driver are selected for compatibility with standard and Low-Power Schottky inputs.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and OE LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

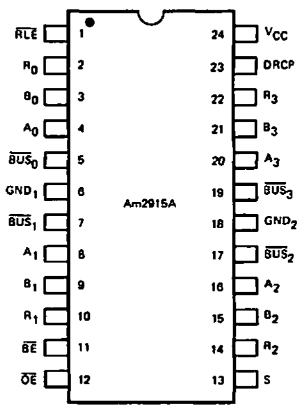
LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

MPR-159

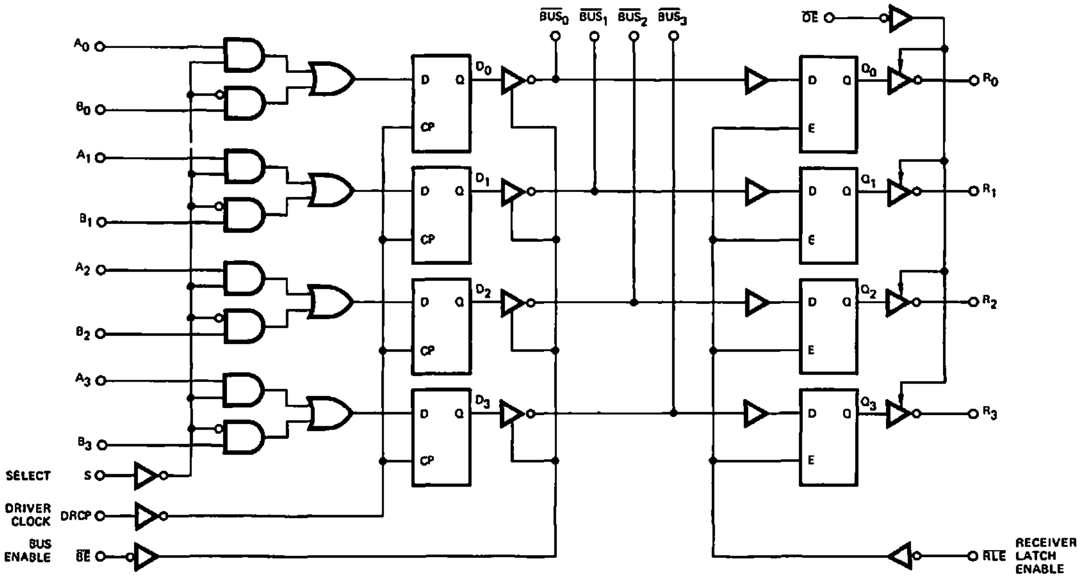
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-160

LOGIC DIAGRAM



MPR-161

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915AXC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2915AXM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V, V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0V		−50	−120	−225	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC}MIN. = 4.75 V V_{CC}MAX. = 5.25 V
Am2915AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC}MIN. = 4.50 V V_{CC}MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

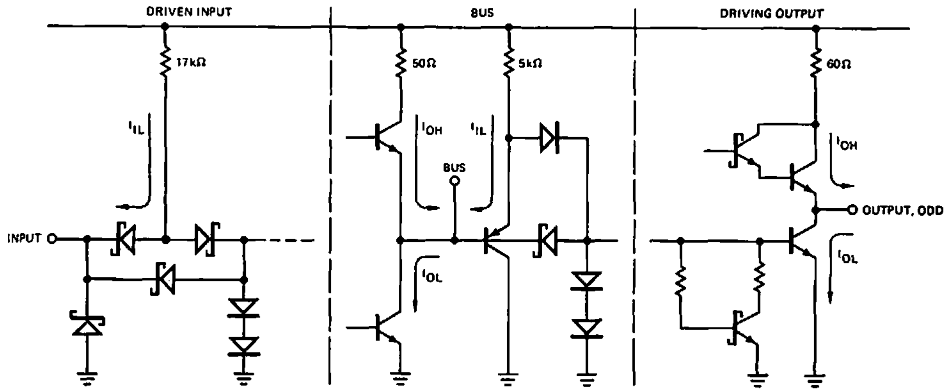
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0mA$	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6mA$	2.4	3.4		
		V_{CC} = 5.0V, $I_{OH} = -100\mu A$		3.5			
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4.0mA		0.27	0.4	Volts
			I_{OL} = 8.0mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4 V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0 V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		−30		−130	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4 V			50	μA
			V_O = 0.4 V			−50	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2915AXM Min.	Am2915AXM Typ. (Note 2)	Am2915AXM Max.	Am2915AXC Min.	Am2915AXC Typ. (Note 2)	Am2915AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	Data Inputs (A or B)	C_L = 15pF, R_L = 2.0kΩ	15			12			ns
t_h			8.0			6.0			
t_s	Select Input (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)			18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{ZH}, t_{ZL}	Output Control to Receiver Output			14	26		14	23	ns
t_{HZ}, t_{LZ}		C_L = 5pF, R_L = 2.0kΩ		14	26		14	23	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

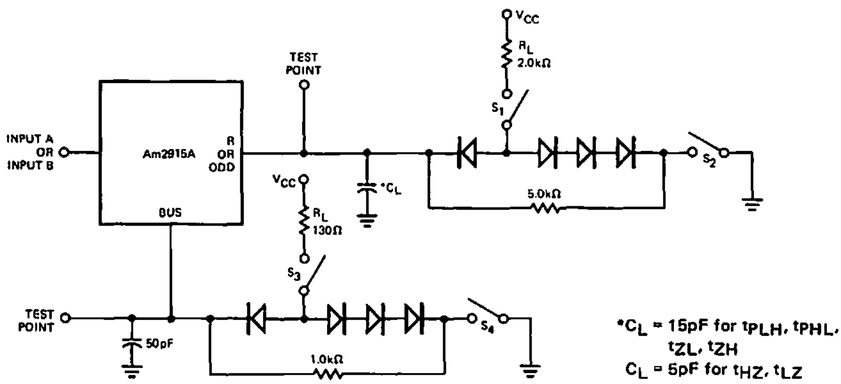
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

MPR-162

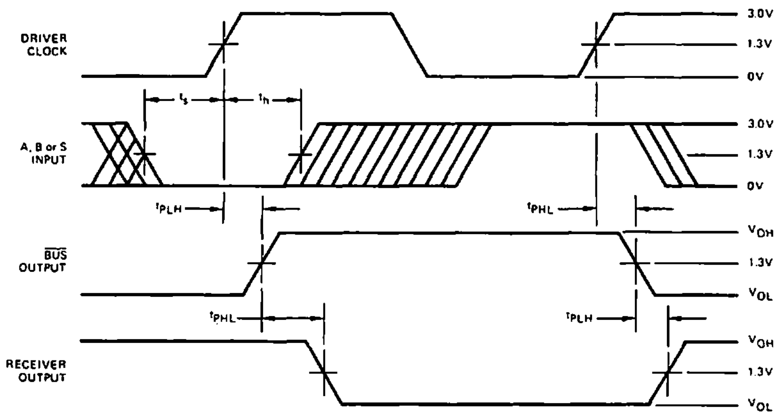
SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

MPR-163

SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{\text{BUS}}$ to R combinatorial delay.

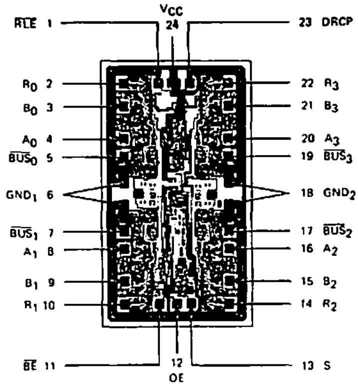
MPR-164

FUNCTIONAL TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care I = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



DIE SIZE .074" X .130"

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

$\overline{BUS}_0, \overline{BUS}_1, \overline{BUS}_2, \overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

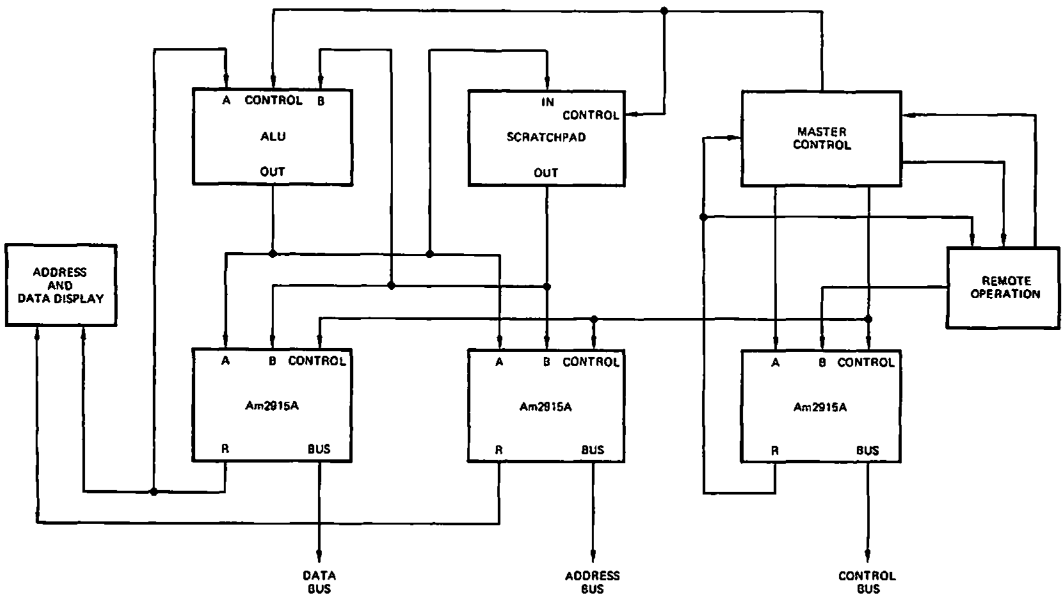
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2915APC	P-24	C	C-1
AM2915ADC	D-24	C	C-1
AM2915ADC-B	D-24	C	B-1
AM2915ADM	D-24	M	C-3
AM2915ADM-B	D-24	M	B-3
AM2915AFM	F-24	M	C-3
AM2915AFM-B	F-24	M	B-3
AM2915AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2915AXM	Dice	M	

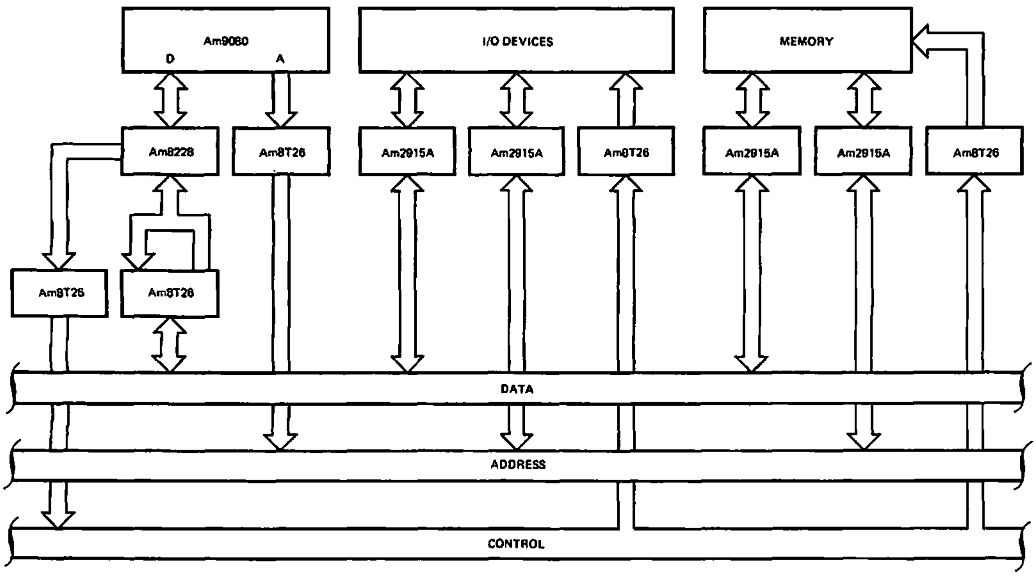
Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATIONS



The Am2915A is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.

MPR-165



Using the Am2915A and Am8T26 in a terminated Bus system for the Am9080 MOS Microprocessor.

MPR-166

Am2916A

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

The Am2916A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

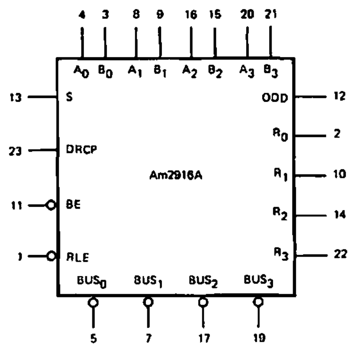
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data in non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2916A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

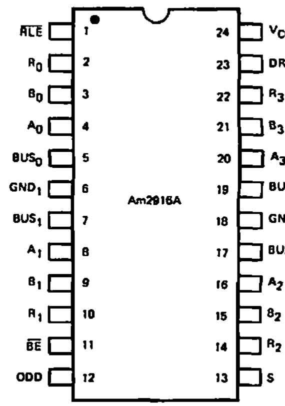
LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

MPR-167

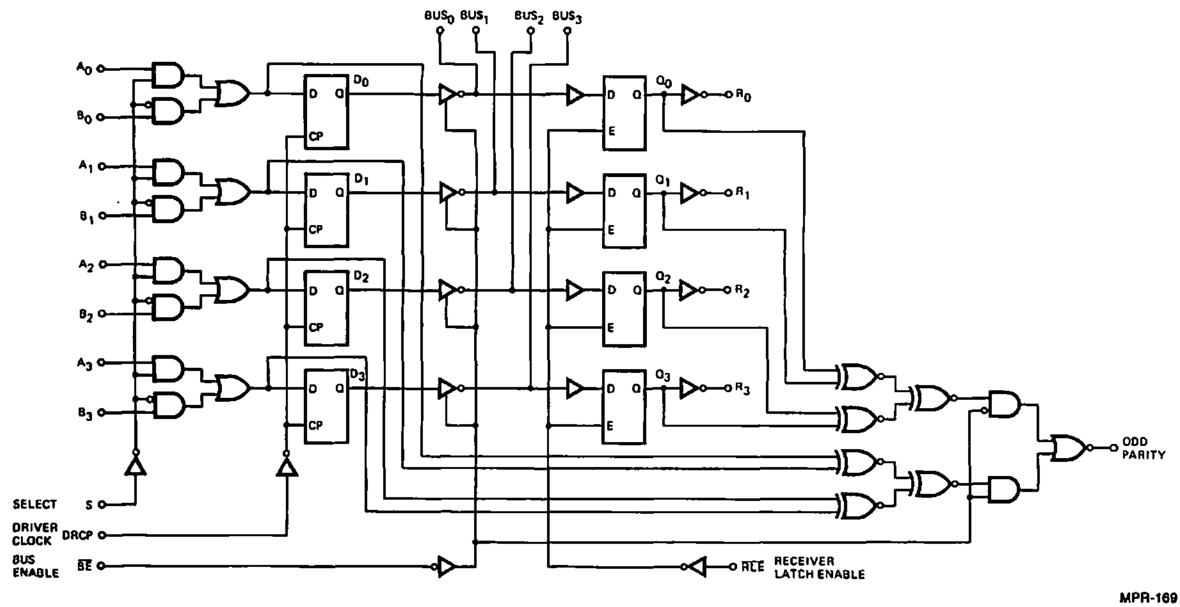
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-168

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916AXC (COM'L)	T_A = 0°C to +70°C	V_{CC}MIN. = 4.75V	V_{CC}MAX. = 5.25V
Am2916AXM (MIL)	T_A = −55°C to +125°C	V_{CC}MIN. = 4.50V	V_{CC}MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V, V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0V		−50	−120	−225	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916AXC (COM'L)	T_A = 0°C to +70°C	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2916AXM (MIL)	T_A = −55°C to +125°C	V_{CC} MIN. = 4.50V	V_{CC} MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

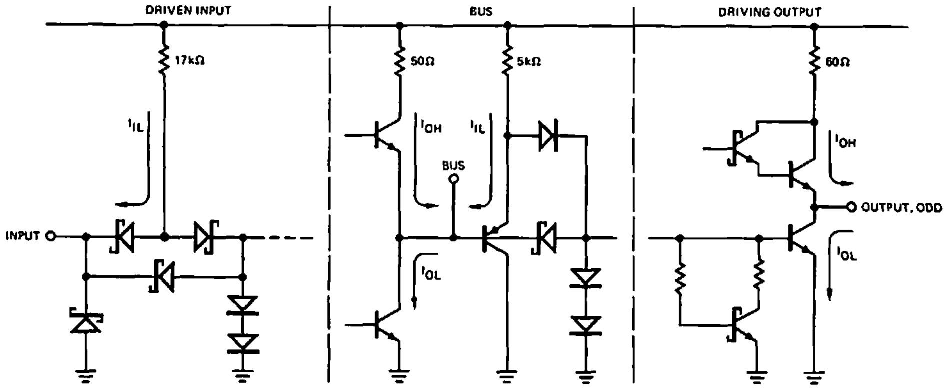
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IL} or V_{IH}	MIL: I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L: I_{OH} = −2.6mA	2.4	3.4		
		V_{CC} = 5.0V, I_{OH} = −100μA		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −660μA V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN. V_{IN} = V_{IL} or V_{IH}	I_{OL} = 4.0mA		0.27	0.4	Volts
			I_{OL} = 8.0mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.	RECEIVER	−30		−130	mA
			PARITY	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND			75	110	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2916AXM Min.	Am2916AXM Typ. (Note 2)	Am2916AXM Max.	Am2916AXC Min.	Am2916AXC Typ. (Note 2)	Am2916AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF R_L (BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	Data Inputs (A or B)		15			12			ns
t_h			8.0			6.0			
t_s	Select Inputs (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)	C_L = 15pF R_L = 2.0kΩ		18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			32	46		32	42	ns
t_{PHL}				26	40		26	36	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}				21	36		21	32	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test shoul not exceed one second.

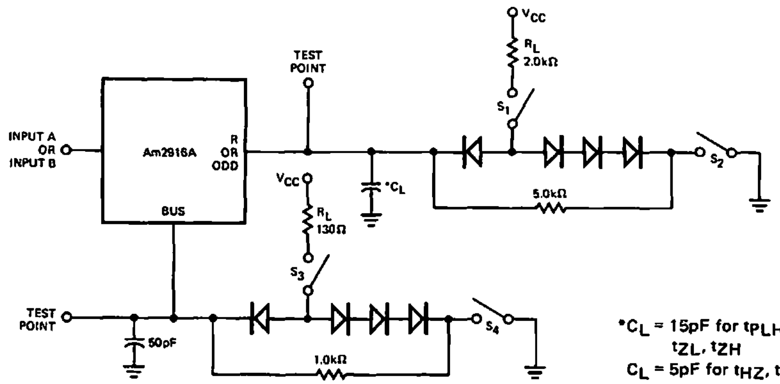
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

MPR-170

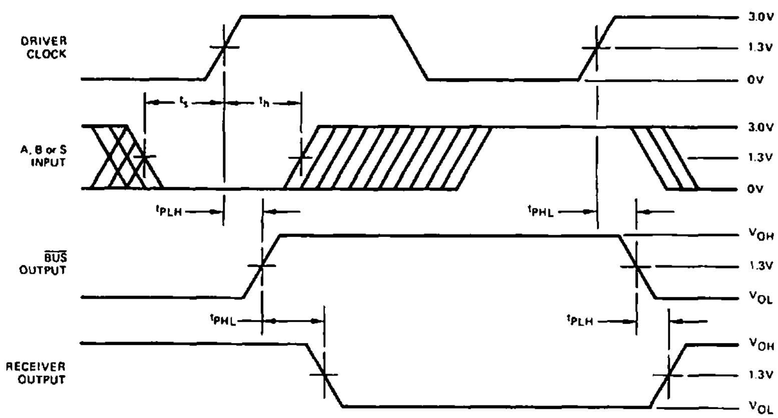
SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

MPR-171

SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

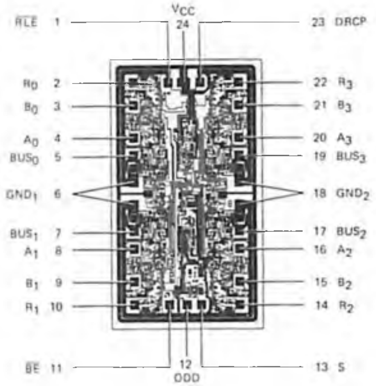
MPR-172

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS_i}$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



DIE SIZE .074" X .130"

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

$\overline{BUS_0}, \overline{BUS_1}, \overline{BUS_2}, \overline{BUS_3}$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

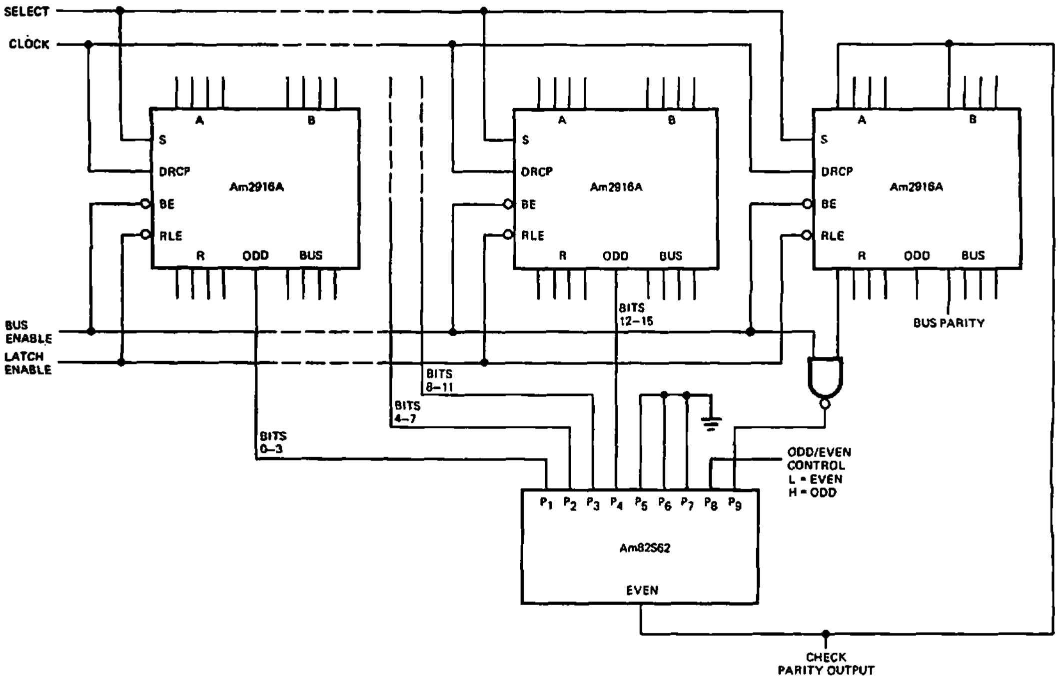
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2916APC	P-24	C	C-1
AM2916ADC	D-24	C	C-1
AM2916ADC-B	D-24	C	B-1
AM2916ADM	D-24	M	C-3
AM2916ADM-B	D-24	M	B-3
AM2916AFM	F-24	M	C-3
AM2916AFM-B	F-24	M	B-3
AM2916AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2916AXM	Dice	M	

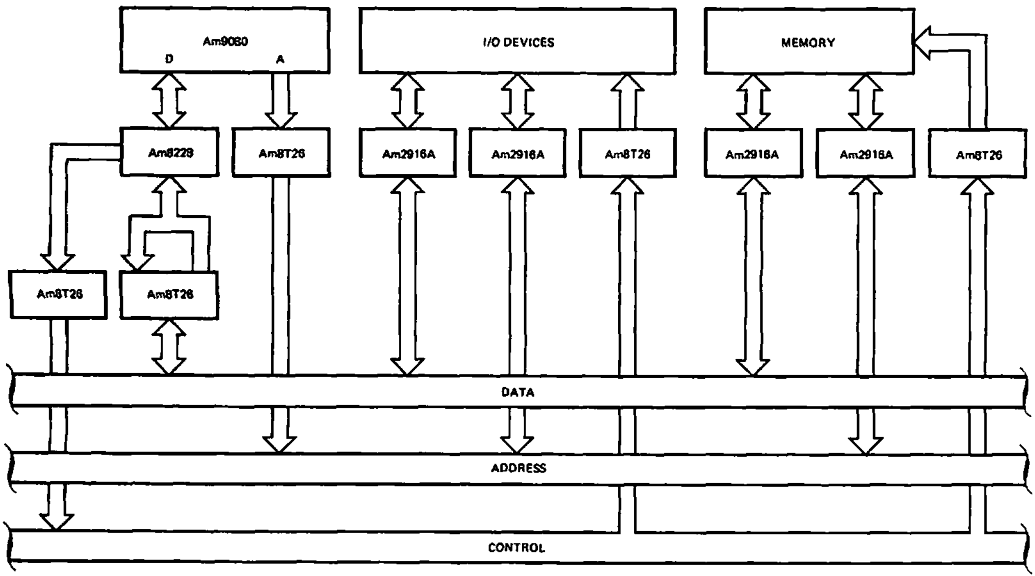
Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATIONS



Generating or checking parity for 16 data bits.

MPR-173



Using the Am2916A and Am8T26 in a terminated Bus system for the Am9080 MOS Microprocessor.

MPR-174

Am2917A

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

The Am2917A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

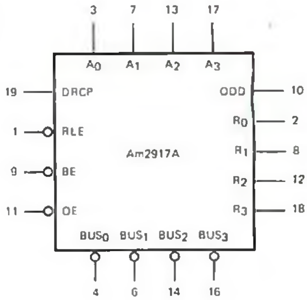
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2917A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

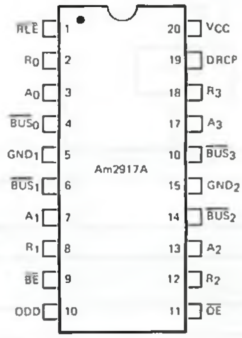
LOGIC SYMBOL



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

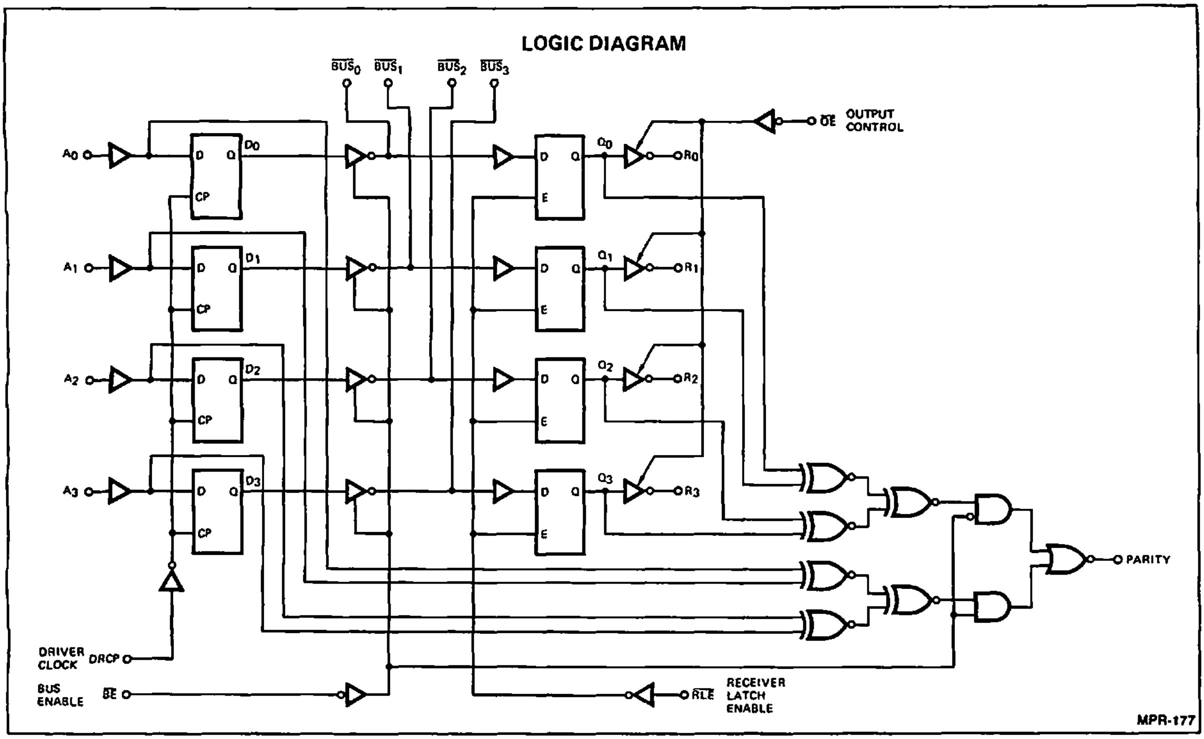
MPR-175

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-176



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential	–0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	–0.5 V to $+V_{CC}$ max.
DC Input Voltage	–0.5 V to +7 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	100 mA
DC Input Current	–30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917AXC (COM'L)	T_A = 0°C to +70°C	V_{CC} MIN. = 4.75 V	V_{CC} MAX. = 5.25 V
Am2917AXM (MIL)	T_A = –55°C to +125°C	V_{CC} MIN. = 4.50 V	V_{CC} MAX. = 5.50 V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = –20mA	2.4			Volts
			MIL, I_{OH} = –15mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4 V	V_O = 0.4 V			–200	μA
			V_O = 2.4 V			50	
			V_O = 4.5 V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5 V, V_{CC} = 0 V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4 V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4 V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0 V		–50	–120	–225	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2917AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

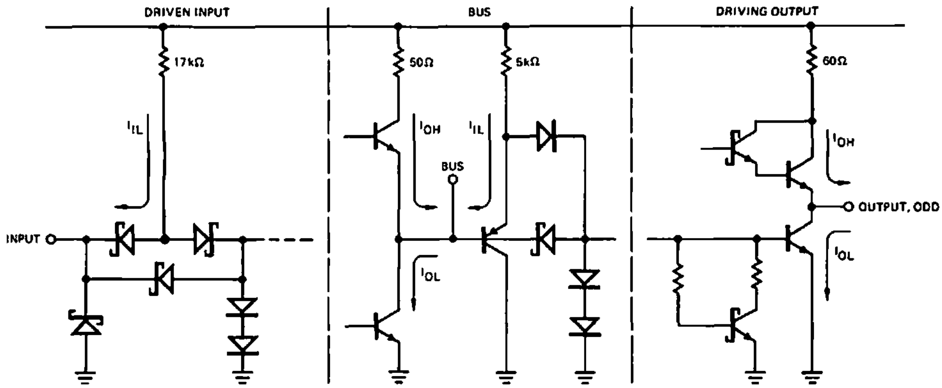
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	MIL: I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L: I_{OH} = −2.6mA	2.4	3.4		
		V_{CC} = 5.0V, I_{OH} = −100μA		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −660μA $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4.0mA		0.27	0.4	Volts
			I_{OL} = 8.0mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.	RECEIVER	−30		−130	mA
			PARITY	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = MAX.			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4V			50	μA
			V_O = 0.4V			−50	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2917AXM Min.	Am2917AXM Typ. (Note 2)	Am2917AXM Max.	Am2917AXC Min.	Am2917AXC Typ. (Note 2)	Am2917AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF R_L BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	A Data Inputs	C_L = 15pF R_L = 2.0kΩ	15			12			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)			32	46		32	42	ns
t_{PHL}				26	40		26	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{ZH}, t_{ZL}	Output Control to Output			14	26		14	23	ns
t_{HZ}, t_{LZ}		C_L = 5pF, R_L = 2.0kΩ		14	26		14	23	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

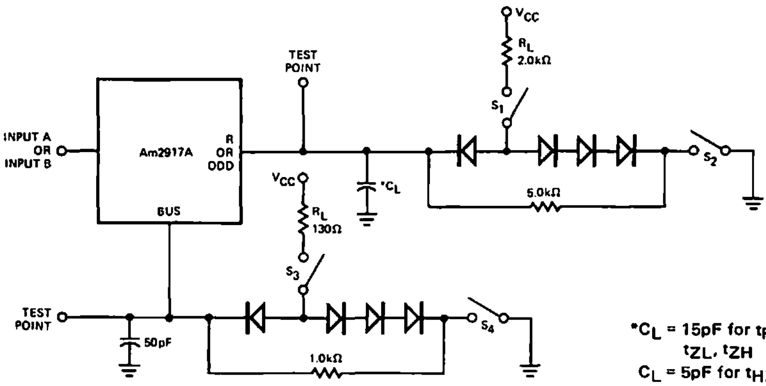
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

MPR-178

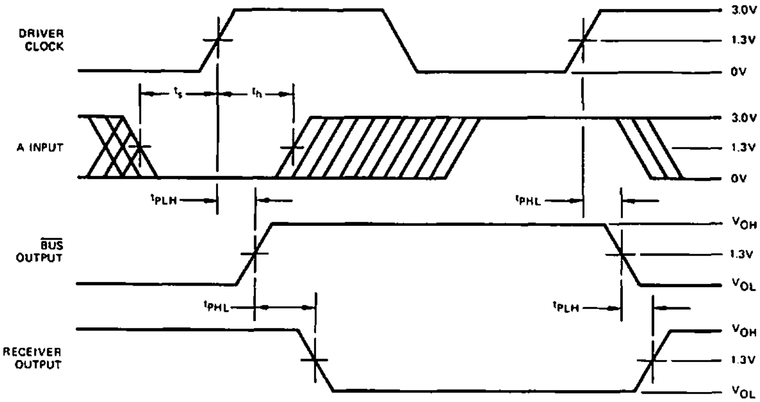
SWITCHING TEST CIRCUIT



$^*C_L$ = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

MPR-179

SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

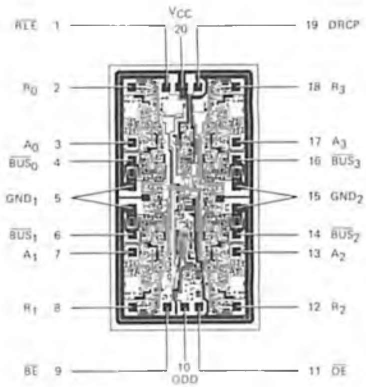
MPR-180

FUNCTION TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS_i}$	R_i	
X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



DIE SIZE .074" X .130"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2917APC	P-20	C	C-1
AM2917ADC	D-20	C	C-1
AM2917ADC-B	D-20	C	B-1
AM2917ADM	D-20	M	C-3
AM2917ADM-B	D-20	M	B-3
AM2917AFM	F-20	M	C-3
AM2917AFM-B	F-20	M	B-3
AM2917AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2917AXM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

DEFINITION OF FUNCTIONAL TERMS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{\textbf{BE}}$ Bus Enable. When the Bus Enable is LOW, the four drivers are in the high impedance state.

$\overline{BUS_0}$, $\overline{BUS_1}$, $\overline{BUS_2}$, $\overline{BUS_3}$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{\textbf{RLE}}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

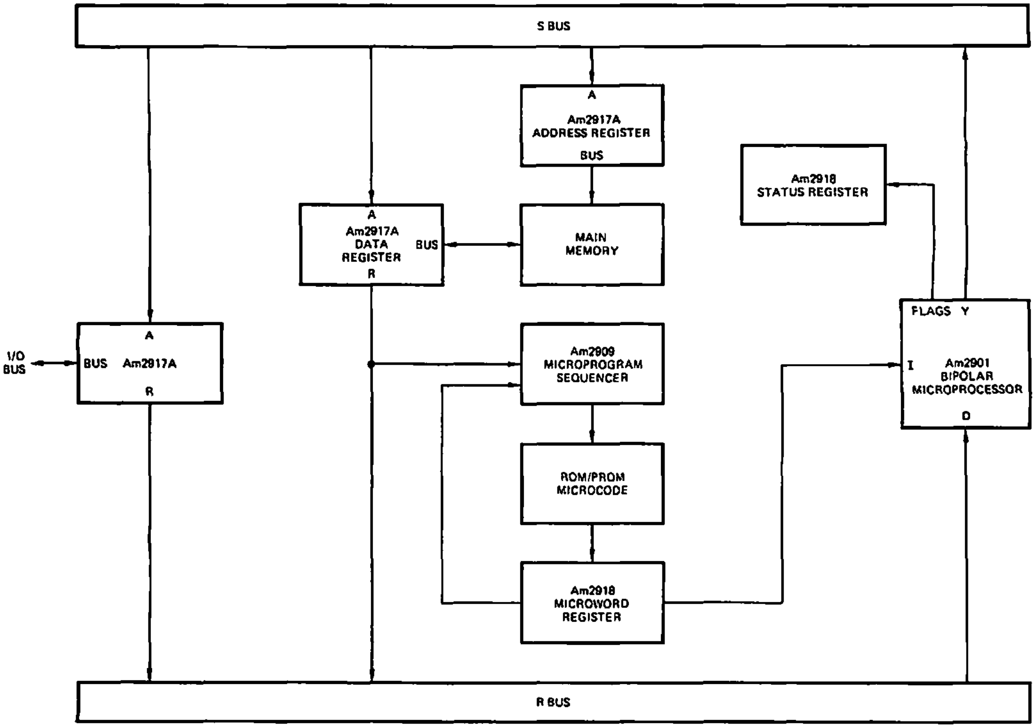
ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

$\overline{\textbf{OE}}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

PARITY OUTPUT FUNCTION TABLE

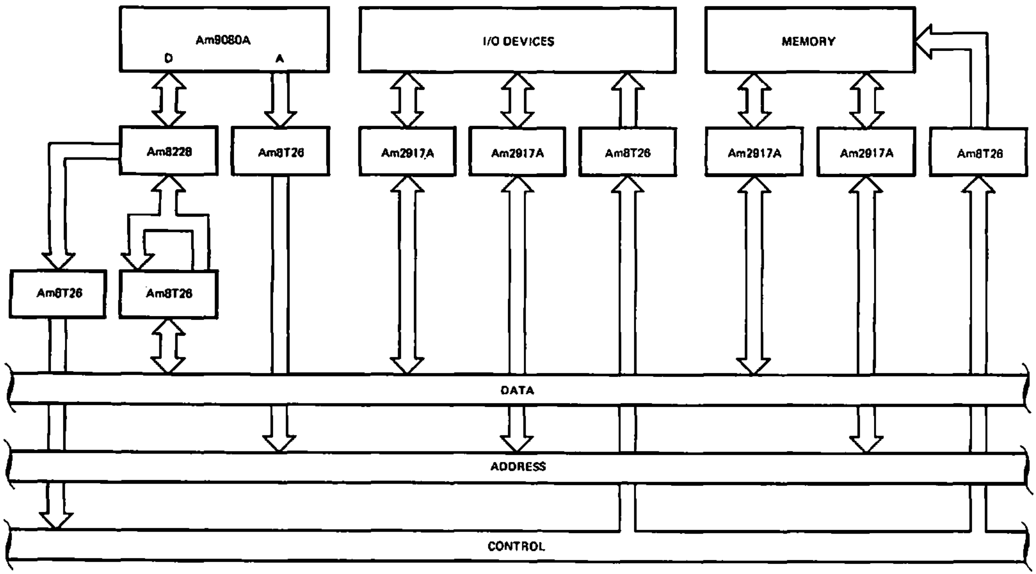
$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

APPLICATIONS



The Am2917A can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

MPR-181



Using the Am2917A and Am8T26 in a terminated Bus system for the Am9080 MOS Microprocessor.

MPR-182

Am3212•Am8212

Eight-Bit Input/Output Port

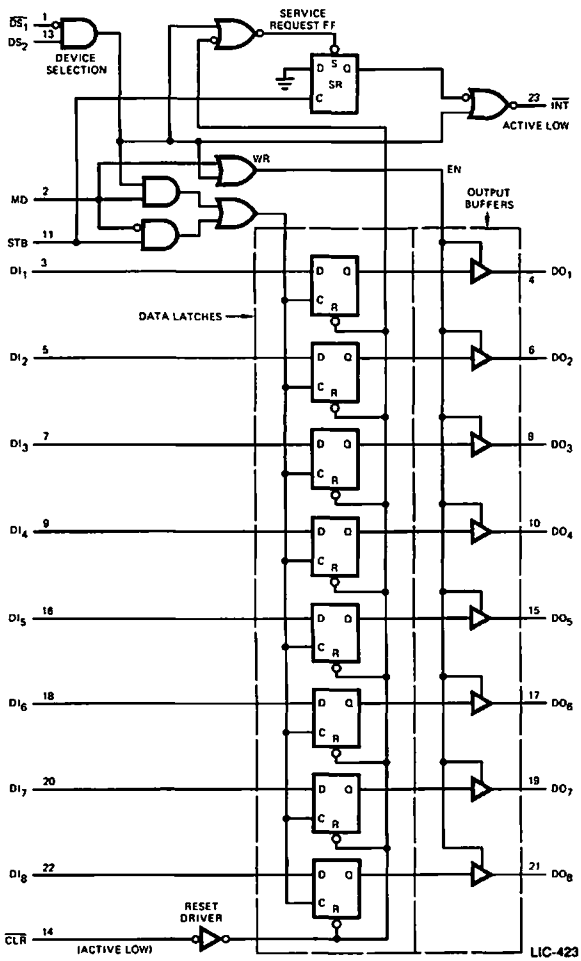
Distinctive Characteristics

- Fully parallel, 8-bit data register and buffer replacing latches, multiplexers and buffers needed in microprocessor systems.
- 4.0V output high voltage for direct interface to MOS microprocessors, such as the Am9080A family.
- Input load current 250μA max.
- Reduces system package count
- Available for operation over both commercial and military temperature ranges.
- Advanced Schottky processing with 100% reliability assurance testing in compliance with MIL-STD-883.
- Service request flip-flop for interrupt generation
- Three-state outputs sink 15mA
- Asynchronous register clear with clock over-ride

FUNCTIONAL DESCRIPTION

All of the principal peripheral and input/output functions of a Microcomputer System can be implemented with the Am3212 • Am8212. The Am3212 • Am8212 input/output port consists of an 8-latch with 3-state output buffers along with control and device selection logic, which can be used to implement latches, gated buffers or multiplexers.

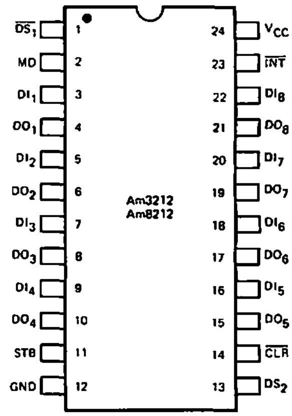
LOGIC DIAGRAM



LIC-423

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

LIC-424

PIN DEFINITION

$DI_1 - DI_8$	DATA IN
$DO_1 - DO_8$	DATA OUT
$\overline{DS_1} - DS_2$	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	–55°C to +125°C	AM8212DM
Hermetic DIP	0°C to +70°C	D8212
Molded DIP	0°C to +70°C	P8212
Dice	0°C to +70°C	AM8212XC
Hermetic DIP	0°C to +70°C	D3212
Hermetic DIP	–55°C to +125°C	MD3212
Molded DIP	0°C to +70°C	P3212

FUNCTIONAL DESCRIPTION (Cont'd)

Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overrides Reset ($\overline{CLR}$)).

Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state). This high-impedance state allows the Am3212 • Am8212 to be connected directly onto the microprocessor bi-directional data bus.

Control Logic

The Am3212 • Am8212 has control inputs $\overline{DS}_1$, DS_2, MD And STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

$\overline{DS}_1$, DS_2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS}_1$ is low and DS_2 is high ($\overline{DS}_1 \cdot DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS}_1 \cdot DS_2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS}_1 \cdot DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Request Flip-Flop

The SR flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS}_1 \cdot DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

TRUTH TABLE

STB	MD	$\overline{DS}_1 - DS_2$	Data Out Equals
0	0	0	Three-State
1	0	0	Three-State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

CLR	$\overline{DS}_1 - DS_2$	STB	SR*	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	1	$\searrow$	0	0
1	1	0	1	0
1	0	0	1	1
1	1	$\searrow$	1	0

$\overline{CLR}$ – Resets Data Latch
– Sets SR Flip-Flop (no effect on Output Buffer)
* Internal SR Flip-Flop

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage	−0.5V to +7.0V
Output Voltage	−0.5V to +7.0V
Input Voltages	−1.0V to +5.5V
Output Current (Each Output)	125mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

P8212, D8212, P3212, D3212 (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$
Am8212DM, MD3212 (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$

DC CHARACTERISTICS

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
I_F	Input Load Current ACK, DS_2, CR, $DI_1 - DI_8$ Inputs	$V_F = 0.45V$				−0.25	mA
I_F	Input Load Current MD Input	$V_F = 0.45V$				−0.75	mA
I_F	Input Load Current DS_1 Input	$V_F = 0.45V$				−1.0	mA
I_R	Input Leakage Current ACK, DS, CR, $DI_1 - DI_8$ Inputs	$V_R = 5.25V$				10	μA
I_R	Input Leakage Current MO Input	$V_R = 5.25V$				30	μA
I_R	Input Leakage Current DS_1 Input	$V_R = 5.25V$				40	μA
V_C	Input Forward Voltage Clamp	$I_C = -5.0mA$	COM'L			−1.0	Volts
			MIL			−1.2	
V_{IL}	Input LOW Voltage		COM'L			0.85	Volts
			MIL			0.80	
V_{IH}	Input HIGH Voltage			2.0			Volts
V_{OL}	Output LOW Voltage	$I_{OL} = 15mA$				0.45	Volts
V_{OH}	Output HIGH Voltage	$I_{OH} = -1.0mA$	COM'L	3.65	4.0		Volts
			MIL	3.3	4.0		
		$I_{OH} = -0.5mA$	MIL	3.4	4.0		
I_{SC}	Short Circuit Output Current	$V_O = 0V$		−15		−75	mA
$\|I_O\|$	Output Leakage Current High Impedance	$V_O = 0.45V/5.25V$				20	μA
I_{CC}	Power Supply Current	Note 2			90	130	mA

AC CHARACTERISTICS (Note 3)

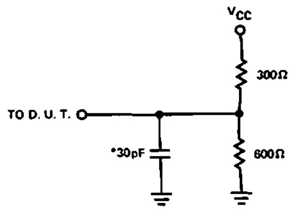
Parameters	Description	Min.	Typ. (Note 1)	Max.	Units
t_{pw}	Pulse Width	30	8		ns
t_{pd}	Data to Output Delay		12	30	ns
t_{we}	Write Enable to Output Delay		18	40	ns
t_{set}	Data Set-up Time	15			ns
t_h	Data Hold Time	20			ns
t_r	Reset to Output Delay		18	40	ns
t_s	Set to Output Delay		15	30	ns
t_e	Output Enable/Disable Time		14	45	ns
t_c	Clear to Output Delay		25	55	ns

CAPACITANCE (Note 4)

F = 1.0MHz, $V_{BIAS} = 2.5V$, $V_{CC} = +5.0V$, $T_A = 25°C$

Parameters	Description	Typ.	Max.	Units
C_{IN}	DS_1 MD Input Capacitance	9.0	12	pF
C_{IN}	DS_2, CK, ACK, $DI_1 - DI_8$ Input Capacitance	5.0	9.0	pF
C_{OUT}	$DO_1 - DO_8$ Output Capacitance	8.0	12	pF

TEST LOAD (15mA and 30pF)

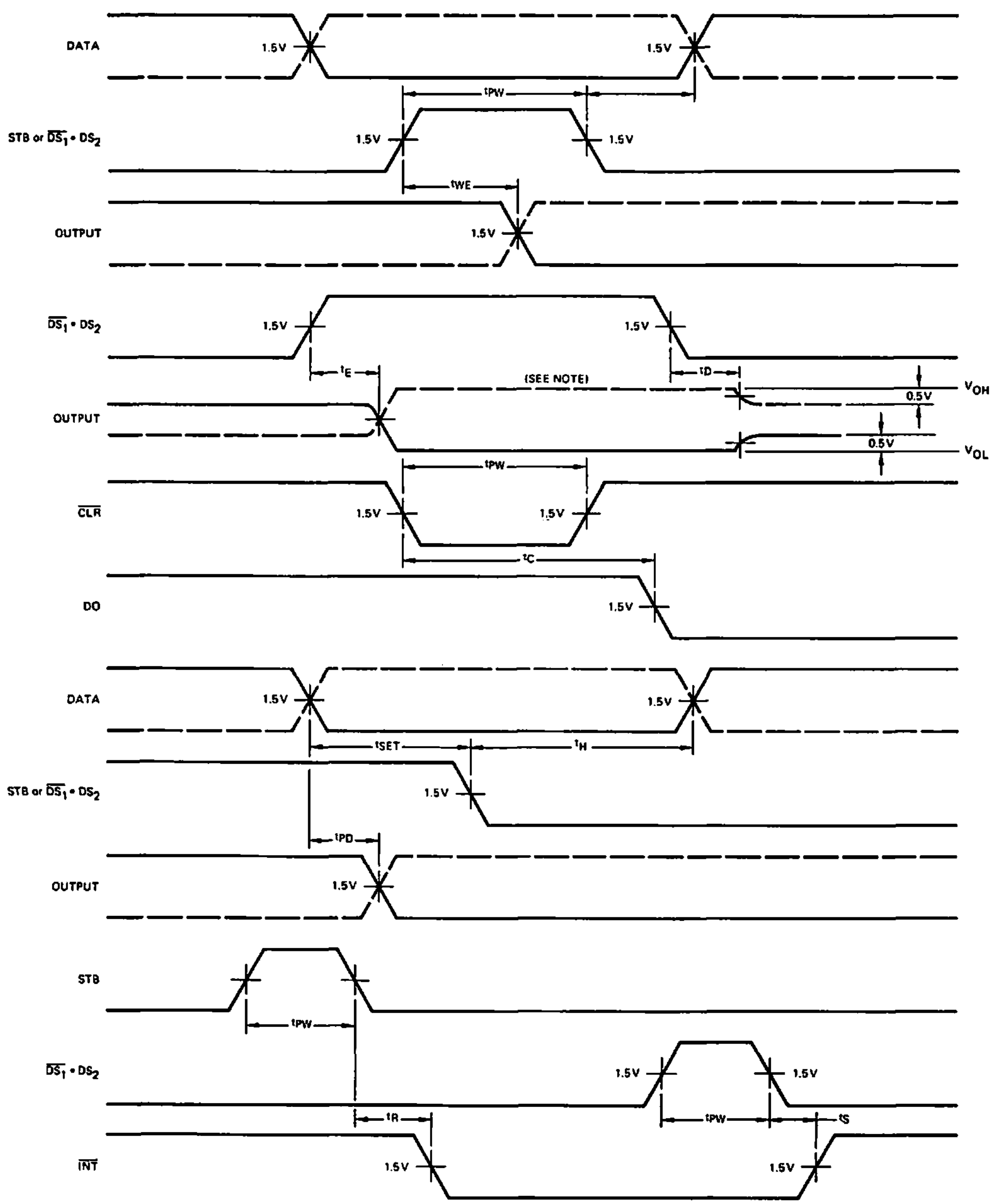


*Including Jig and Probe Capacitance.

LIC-425

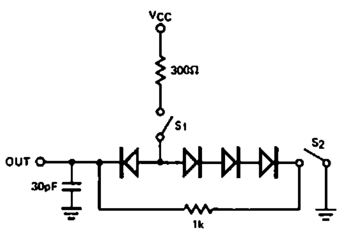
Notes: 1. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
2. CLR = STB = HIGH; $\overline{DS_1}$ = DS_2 = MD = LOW; all data inputs are gound, all data outputs are open.
3. Conditions of Test: a) Input pulse amplitude = 2.5V
b) Input rise and fall times 5.0ns
c) Between 1.0V and 2.0V measurements made at 1.5V with 15mA and 30pF Test Load.
4. This parameter is sampled and not 100% tested.

TIMING DIAGRAM



LIC-426

Note: Alternative Test Load.

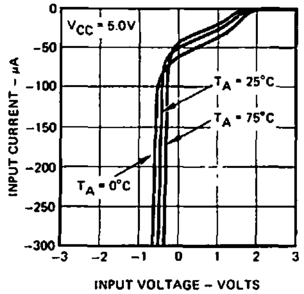


LIC-427

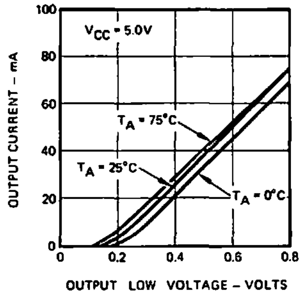
4

TYPICAL CHARACTERISTICS

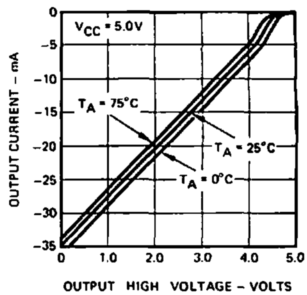
Input Current Versus Input Voltage



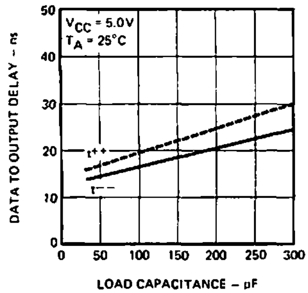
Output Current Versus Output LOW Voltage



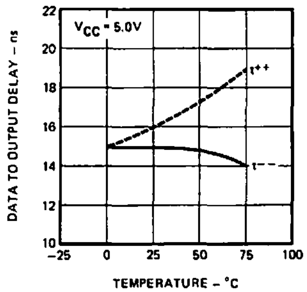
Output Current Versus Output HIGH Voltage



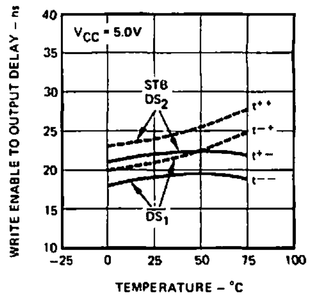
Data to Output Delay Versus Load Capacitance



Data to Output Delay Versus Temperature



Write Enable to Output Delay Versus Temperature

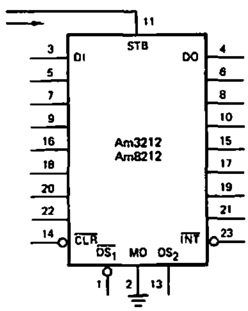


LIC-428

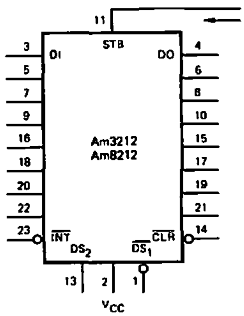
LOGIC SYMBOLS

INPUT DEVICE **OUTPUT DEVICE**

Detailed

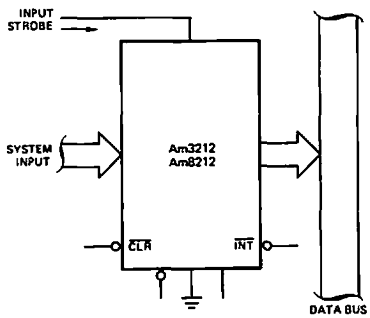


LIC-429

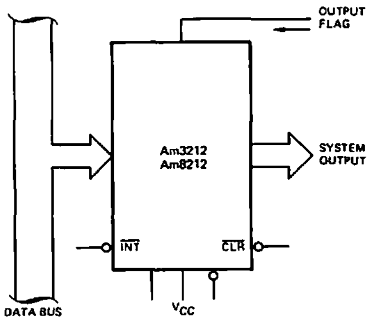


LIC-430

Symbolic



LIC-431



LIC-432

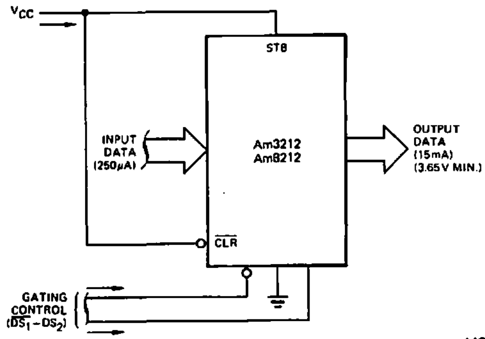
TYPICAL APPLICATIONS OF THE Am8212

GATED BUFFER (3-STATE)

By tying the mode signal low and the strobe input high, the data latch is acting as a straight through gate. The output buffers are then enabled from the device selection logic $\overline{DS_1}$ and DS_2.

When the device selection logic is false, the outputs are 3-state.

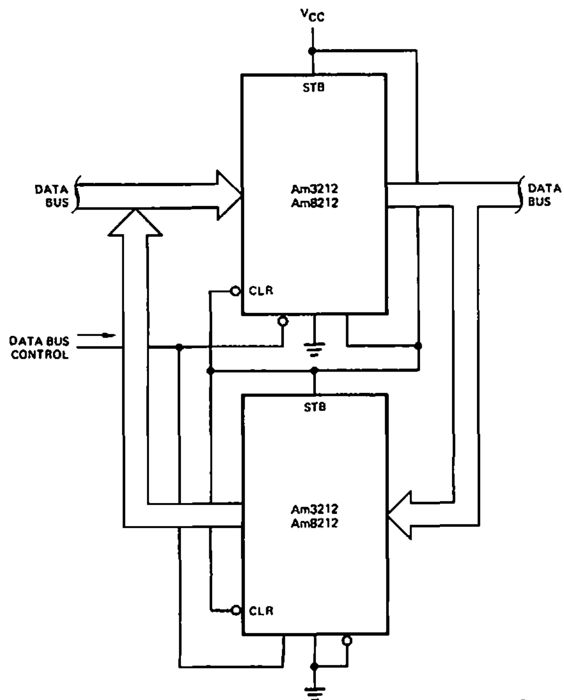
When the device selection logic is true, the input data from the system is directly transferred to the output.



LIC-433

Bi-Directional Bus Driver

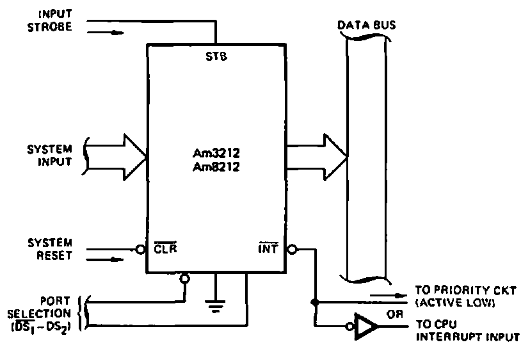
Two Am3212 • Am8212's wired back-to back can be used as a symmetrical drive, bi-directional bus driver. The devices are controlled by the data bus input control which is connected to $\overline{DS_1}$ on the first Am3212 • Am8212 and to DS_2 on the second. While one device is active, and acting as a straight through buffer the other is in its 3-state mode.



LIC-434

Interrupting Input Port

The Am3212 • Am8212 accepts a strobe from the system input source, which in turn clears the service request flip-flop and interrupts the processor. The processor then goes through a service routine, identifies the port, and causes the device selection logic to go true – enabling the system input data onto the data bus.

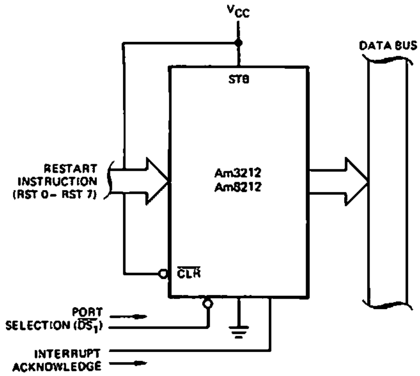


LIC-435

TYPICAL APPLICATIONS OF THE Am8212 (Cont'd)

Interrupt Instruction Port

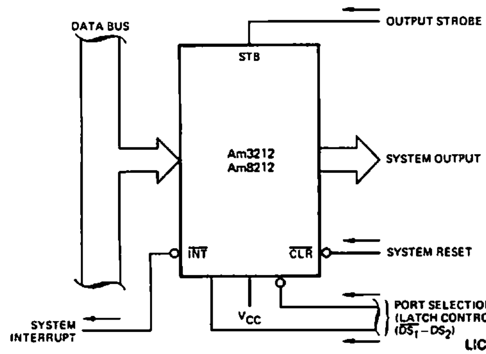
The Am3212 • Am8212 can be used to gate the interrupt instruction, normally RESTART instructions, onto the data bus. The device is enabled from the interrupt acknowledge signal from the microprocessor and from a port selection signal. This signal is normally tied to ground. ($\overline{DS}_1$ could be used to multiplex a variety of interrupt instruction ports onto a common bus).



LIC-436

Output Port (With Hand-Shaking)

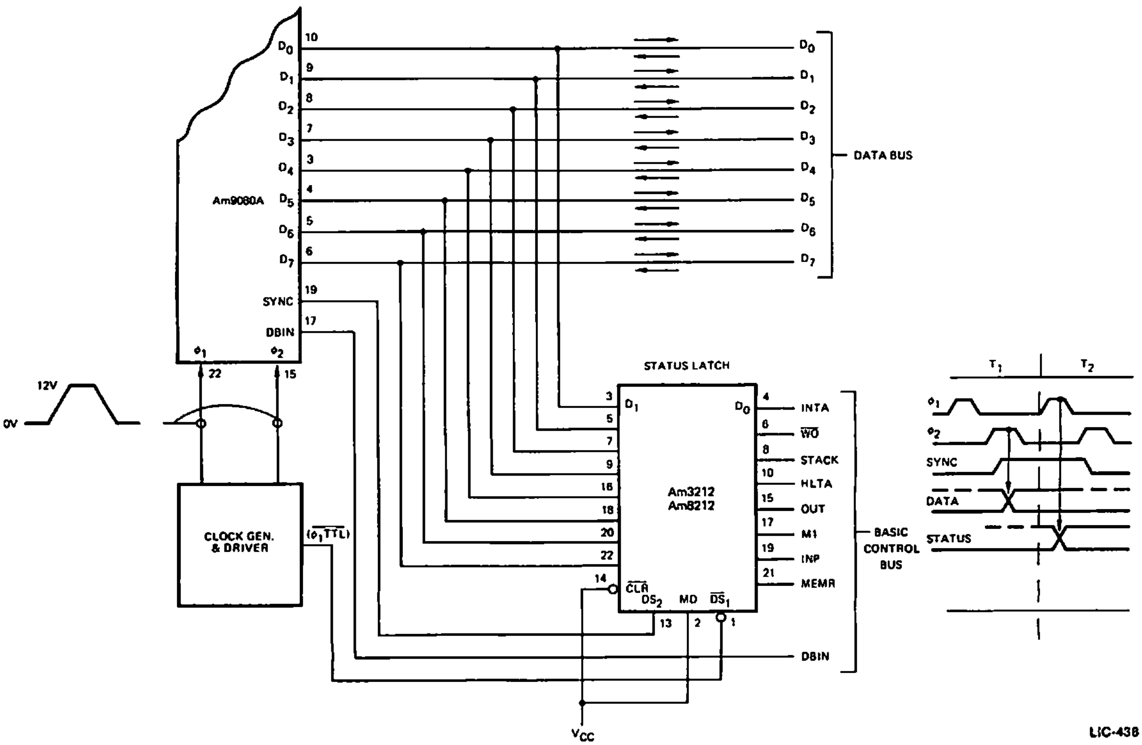
The Am3212 • Am8212 is used to transmit data from the data bus to a system output. The output strobe could be a hand-shaking signal such as "reception of data" from the device that the system is outputting to. It in turn, can interrupt the system signifying the reception of date. The selection of the port comes from the device selection logic. ($\overline{DS}_1 \cdot DS_2$).



LIC-437

Am9080A Status Latch

The input to the Am3212 • Am8212 latch comes directly from the Am9080A data bus. Timing shows that when the SYNC signal is true ($\overline{DS}_1$ input), and $\phi 1$ is true, ($\overline{DS}_1$ input) then the status data will be latched into the Am3212 • Am8212. The mode signal is tied high so that the output on the latch is active and evabled all the time.



LIC-438

Am3216 • Am3226 • Am8216 • Am8226

Four-Bit Parallel Bidirectional Bus Driver

Distinctive Characteristics

- Data bus buffer driver for 8080 type CPU's
- Low input load current – 0.25mA maximum
- High output drive capability for driving system data bus – 50mA at 0.5V
- 100% reliability assurance testing in compliance with MIL-STD-883
- Am3216 and Am8216 have non-inverting outputs
- Output high voltage compatible with direct interface to MOS
- Three-state outputs
- Advanced Schottky processing
- Available in military and commercial temperature range
- Am3226 and Am8226 have inverting outputs

FUNCTIONAL DESCRIPTION

The Am3216, Am3226, Am8216 and Am8226 are four-bit, bi-directional bus drivers for use in bus oriented applications. The non-inverting Am3216 and Am8216, and inverting Am3226 and Am8226 drivers are provided for flexibility in *system design.*

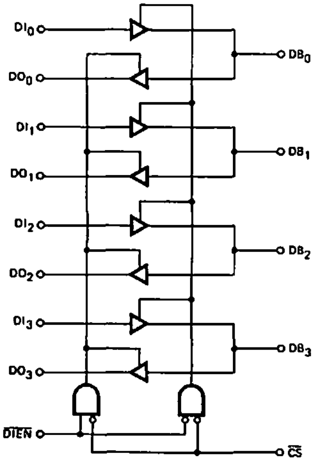
Each buffered line of the four bit driver consists of two separate buffers that are three-state to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this side is used to interface to the system side components such as memories, I/O, etc., because its interface is TTL compatible and it has high drive (50mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bi-directional bus. The DO outputs on this side of the driver have a special high voltage output drive capability so that direct interface to the 8080 type CPUs is achieved with an adequate amount of noise immunity.

The $\overline{CS}$ input is a device enable. When it is "high" the output drivers are all forced to their high-impedance state. When it is a "LOW" the device is enabled and the direction of the data flow is determined by the $\overline{DIEN}$ input.

The $\overline{DIEN}$ input controls the direction of data flow which is accomplished by forcing one of the pair of buffers into its high impedance state and allowing the other to transmit its data. A simple two gate circuit is used for this function.

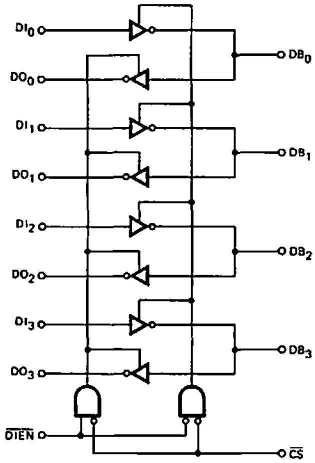
LOGIC DIAGRAMS

Am3216 • Am8216



LIC-439

Am3226 • Am8226



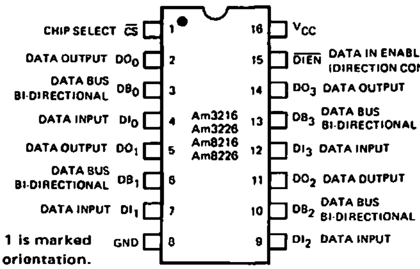
LIC-440

ORDERING INFORMATION

Package Type	Temperature Range	Am3216 Am8216 Order Number	Am3226 Am8226 Order Number
Hermetic DIP	–55°C to +125°C	MD3216	MD3226
Hermetic DIP	0°C to +70°C	D3216	D3226
Molded DIP	0°C to +70°C	P3216	P3226
Hermetic DIP	–55°C to +125°C	MD8216	MD8226
Hermetic DIP	0°C to +70°C	D8216	D8226
Molded DIP	0°C to +70°C	P8216	P8226
Dice	0°C to +70°C	AM8216XC	AM8226XC

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

LIC-441

MAXIMUM RATINGS (Above which the useful life may be impaired)

Temperature (Ambient) Under Bias	−55°C to +125°C
Storage Temperature	−65°C to +150°C
All Output and Supply Voltages	−0.5V to +7.0V
All Input Voltages	−1.0V to +5.5V
Output Currents	125mA

Am3216, Am3226, Am8216 AND Am8226 MILITARY ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (−55°C to +125°C)

The following conditions apply unless otherwise specified:

MD3216, MD8216, MD3226, MD8226 (MIL) T_A = −55°C to +125°C V_{CC} = 5.0V ± 10%

DC CHARACTERISTICS

Parameters	Description		Test Conditions		Min.	Typ. (Note 1)	Max.	Units
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$		V_F = 0.45			−0.15	−0.5	mA
I_{F2}	Input Load Current All Other Inputs		V_F = 0.45			−0.08	−0.25	mA
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$		V_R = 5.5V				80	μA
I_{R2}	Input Leakage Current DI Inputs		V_R = 5.5V				40	μA
V_C	Input Forward Voltage Clamp		I_C = −5.0mA				−1.2	Volts
V_{IL}	Input LOW Voltage	Am3216, Am8216					0.95	Volts
		Am3226, Am8226					0.9	
V_{IH}	Input HIGH Voltage				2.0			Volts
I_O	Output Leakage Current (Three-State)	DO	V_O = 0.45V/5.5V				20	μA
		DB					100	
I_{CC}	Power Supply Current	Am3216, Am8216				95	130	mA
		Am3226, Am8226				85	120	
V_{OL1}	Output LOW Voltage		DO Outputs I_{OL} = 15mA DB Outputs I_{OL} = 25mA			0.3	0.45	Volts
V_{OL2}	Output LOW Voltage		DB Outputs I_{OL} = 45mA			0.5	0.6	Volts
V_{OH1}	Output HIGH Voltage		DO Outputs	I_{OH} = −0.5mA	3.4	4.0		Volts
				I_{OH} = −2.0mA	2.4			
V_{OH2}	Output HIGH Voltage		DB Outputs I_{OH} = −5.0mA		2.4	3.0		Volts
I_{OS}	Output Short Circuit Current		DO Outputs ≅ 0V, V_{CC} = 5.0V		−15	−35	−65	mA
			DB Outputs = 0V, V_{CC} = 5.0V		−30	−75	−120	

AC CHARACTERISTICS

Parameters	Description		Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_{PD1}	Input to Output Delay DO Outputs		C_L = 30pF, R_1 = 300Ω, R_2 = 600Ω		15	25	ns
t_{PD2}	Input to Output Delay DB Outputs	Am3216, Am8216	C_L = 300pF, R_1 = 90Ω, R_2 = 180Ω		20	33	ns
		Am3226, Am8226			16	25	
t_E	Output Enable Time	Am3216	Note 3		45	75	ns
		Am8216	Note 2		45	75	
		Am3226, Am8226	Note 3		35	62	
t_D	Output Disable Time	Am3216, Am8216	Note 4		20	40	ns
		Am3226, Am8226			16	38	

Am3216, Am3226, Am8216 AND Am8226 COMMERCIAL ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (0°C to +70°C)

The following conditions apply unless otherwise specified:

D3216, D8216, D3226, D8226, P3216, P8216, P3226, P8226 (COM'L) T_A = 0°C to +70°C V_{CC} = 5.0V ± 5%

DC CHARACTERISTICS

Parameters	Description		Test Conditions	Min.	Typ. (Note 1)	Max.	Units
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$		V_F = 0.45		−0.15	−0.5	mA
I_{F2}	Input Load Current All Other Inputs		V_F = 0.45		−0.08	−0.25	mA
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$		V_R = 5.25V			20	μA
I_{R2}	Input Leakage Current DI Inputs		V_R = 5.25V			10	μA
V_C	Input Forward Voltage Clamp		I_C = −5.0mA			−1.0	Volts
V_{IL}	Input LOW Voltage					0.95	Volts
V_{IH}	Input HIGH Voltage			2.0			Volts
$\|I_{O}\|$	Output Leakge Current (Three-State)	DO	V_O = 0.45V/5.5V			20	μA
		DB				100	
I_{CC}	Power Supply Current	Am3216, Am8216			95	130	mA
		Am3226, Am8226			85	120	
V_{OL1}	Output LOW Voltage		DB Outputs I_{OL} = 15mA DB Outputs IOL = 25mA		0.3	0.45	Volts
V_{OL2}	Output LOW Voltage	Am3216, Am8216	DB Outputs I_{OL} = 55mA		0.5	0.6	Volts
		Am3226, Am8226	DB Outputs I_{OL} = 50mA		0.5	0.6	
V_{OH1}	Output HIGH Voltage		DO Outputs I_{OH} = −1.0mA COM'L	3.65	4.0		Volts
V_{OH2}	Output HIGH Voltage		DB Outputs I_{OH} = −10mA	2.4	3.0		Volts
I_{OS}	Output Short Circuit Current		DO Outputs ≅ 0V	−15	−35	−65	mA
			DB Outputs V_{CC} = 5.0V	−30	−75	−120	

4

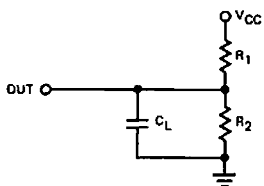
AC CHARACTERISTICS

Parameters	Description		Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_{PD1}	Input to Output Delay DO Outputs		C_L = 30pF, R_1 = 300Ω, R_2 = 600Ω		15	25	ns
t_{PD2}	Input to Output Delay DB Outputs	Am3216, Am8216	C_L = 300pF, R_1 = 90Ω, R_2 = 180Ω		20	30	ns
		Am3226, Am8226			16	25	
t_E	Output Enable Time	Am3216	Note 3		45	65	ns
		Am8216	Note 2		45	65	
		Am3226, Am8226	Note 3		35	54	
t_D	Output Disable Time		Note 4		20	35	ns

TEST CONDITIONS

Input pulse amplitude of 2.5V.
Input rise and fall times of 5.0ns between 1.0 and 2.0 volts.
Output loading is 5.0mA and 10pF.
Speed measurements are made at 1.5V levels.

TEST LOAD CIRCUIT



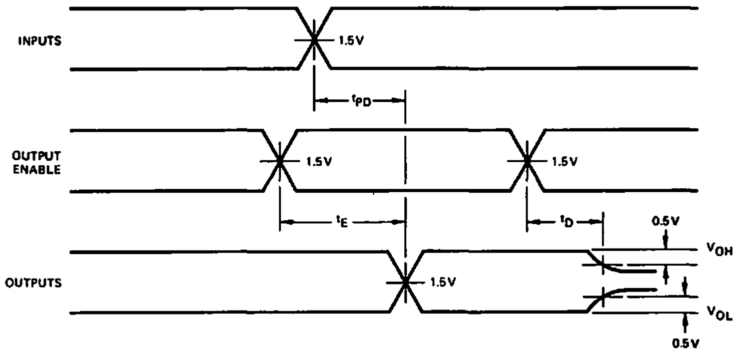
LIC-442

CAPACITANCE (Note 5)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
C_{IN}	Input Capacitance	$V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$ $T_A = 25°C$, f = 1.0MHz		4.0	8.0	pF
C_{OUT1}	Output Capacitance			6.0	10	pF
C_{OUT2}	Output Capacitance			13	18	pF

Notes: 1. Typical values are for $T_A = 25°C$, $V_{CC} = 5.0V$.
2. DO outputs, $C_L = 30pF$, $R_1 = 300/10k\Omega$, $R_2 = 180/1.0k\Omega$; DB outputs, $C_L = 300pF$, $R_1 = 90/10k\Omega$, $R_2 = 180/1.0k\Omega$.
3. DO outputs, $C_L = 30pF$, $R_1 = 300/10k\Omega$, $R_2 = 600/1.0k\Omega$; DB outputs, $C_L = 300pF$, $R_1 = 90/10k\Omega$, $R_2 = 180/1.0k\Omega$.
4. DO outputs, $C_L = 5.0pF$, $R_1 = 300/10k\Omega$, $R_2 = 600/1.0k\Omega$; DB outputs, $C_L = 5.0pF$, $R_1 = 90/10k\Omega$, $R_2 = 180/1.0k\Omega$.
5. This parameter is periodically sampled and not 100% tested.

SWITCHING WAVEFORMS



LIC-443

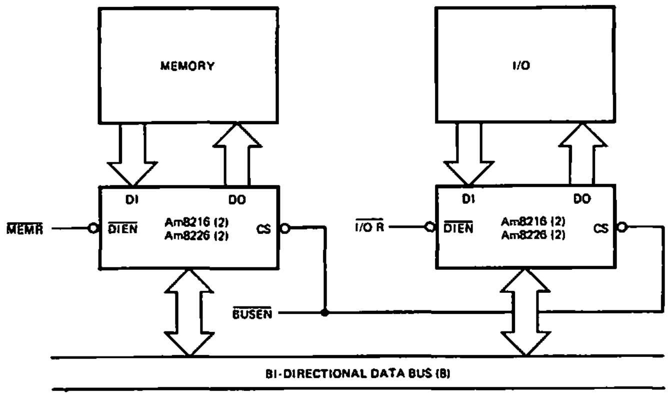
FUNCTION TABLE

$\overline{DIEN}$	$\overline{CS}$		8216 DB	8216 DO	8226 DB	8226 DO
L	L	DI → DB	DI	Z	$\overline{DI}$	Z
H	L	DB → DO	Z	DB	Z	$\overline{DB}$
L	H		Z	Z	Z	Z
H	H		Z	Z	Z	Z

H = HIGH
L = LOW

LIC-444

TYPICAL APPLICATION

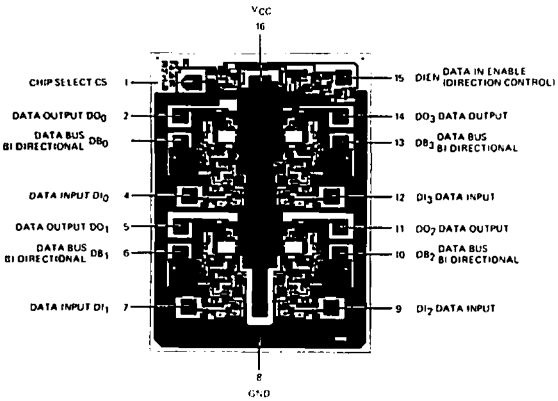


MEMORY AND I/O INTERFACE TO A BI-DIRECTIONAL BUS

LIC-445

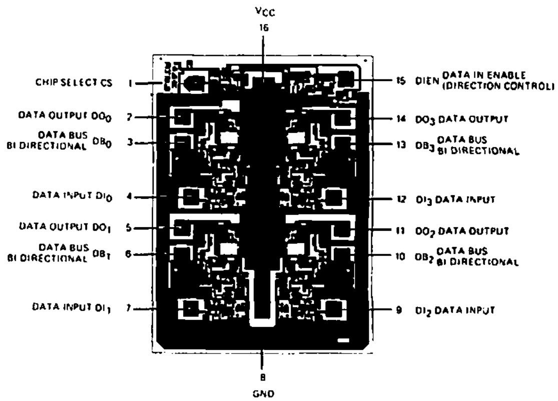
Metallization and Pad Layout

Am3216
Am8216



DIE SIZE 0.066" X 0.090"

Am3226
Am8226



DIE SIZE 0.066" X 0.090"

4

Am3448A

IEEE-488 Quad Bidirectional Transceiver

DISTINCTIVE CHARACTERISTICS

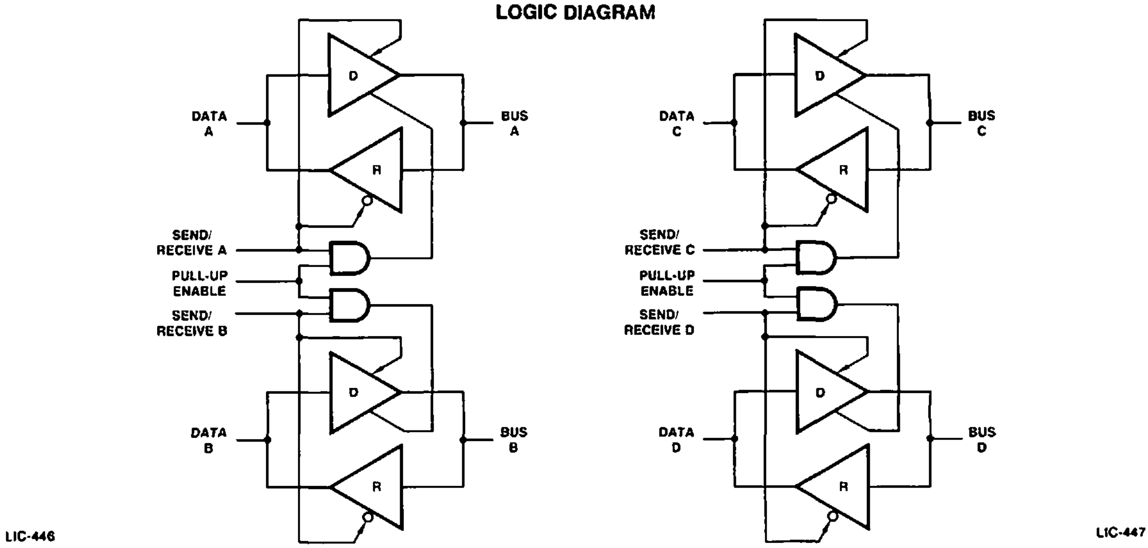
- Four independent driver/receiver pairs
- Three-state outputs
- High impedance inputs
- Receiver hysteresis – 600mV (Typ.)
- Fast Propagation Times – 50-20ns (Typ.)
- TTL compatible receiver outputs
- Single +5 volt supply
- Open collector driver output option with internal passive pull up
- Power up/power down protection (No invalid information transmitted to bus)
- No bus loading when power is removed from device
- Required termination characteristics provided
- Advanced Schottky processing
- 100% product assurance screening to MIL-STD-883 requirements

GENERAL DESCRIPTION

The Am3448A is a quad bidirectional transceiver meeting the requirement of IEEE-488 standard digital interface for programmable instrumentation for the driver, receiver, and composite device load. One pull-up enable input is provided for each pair of transceivers which controls the operating mode of the driver outputs as either an open collector or active pull-up configuration.

The receivers feature input hysteresis for improved noise immunity in system applications. The device bus (receiver input) changes from standard bus loading to a high impedance load when power is removed. In addition no spurious noise is generated on the bus during power-up or power-down.

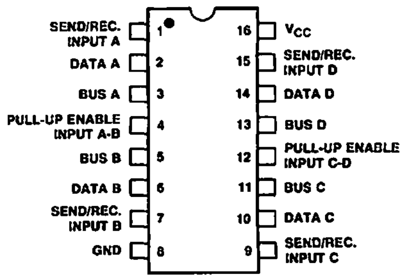
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +70°C	MC3448AL
Molded DIP	0°C to +70°C	MC3448AP
Dice	0°C to +70°C	AM3448AX

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation. LIC-448

ABSOLUTE MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Driver Output Current	150mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am3448A T_A = 0°C to 70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V

DC ELECTRICAL CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
Bus Characteristics						
$V_{(BUS)}$	Bus Voltage	Bus Pin Open, $V_{I(S/R)}$ = 0.8V	2.75	–	3.7	Volts
$V_{IC(BUS)}$		$I_{(BUS)}$ = −12mA	–	–	−1.5	
$I_{(BUS)}$	Bus Current	5.0V ≤ $V_{(BUS)}$ ≤ 5.5V	0.7	–	2.5	mA
		$V_{(BUS)}$ = 0.5V	−1.3	–	−3.2	
		V_{CC} = 0V, 0V ≤ $V_{(BUS)}$ ≤ 2.75V	–	–	0.04	
Driver Characteristics						
$V_{IC(D)}$	Driver Input Clamp Voltage	$V_{I(S/R)}$ = 2.0V, $I_{IC(D)}$ = −18mA	–	–	−1.5	Volts
$V_{OH(D)}$	Driver Output Voltage – High Logic State	$V_{I(S/R)}$ = 2.0V, $V_{IH(D)}$ = 2.0V, $V_{IH(E)}$ = 2.0V, I_{OH} = −5.2mA	2.5	–	–	Volts
$V_{OL(D)}$	Driver Output Voltage – Low Logic State	$V_{I(S/R)}$ = 2.0V, $I_{OL(D)}$ = 48mA	–	–	0.5	Volts
$I_{OS(O)}$	Output Short Circuit Current	$V_{I(S/R)}$ = 2.0V, $V_{IH(D)}$ = 2.0V $V_{IH(E)}$ = 2.0V	−30	–	−120	mA
$V_{IH(D)}$	Driver Input Voltage – High Logic State	$V_{I(S/R)}$ = 2.0V	2.0	–	–	Volts
$V_{IL(D)}$	Driver Input Voltage – Low Logic State	$V_{I(S/R)}$ = 2.0V	–	–	0.8	Volts
$I_{I(D)}$	Driver Input Current – Data Pins	$V_{I(S/R)}$ = $V_{I(E)}$ = 2.0V; 0.5 ≤ $V_{I(D)}$ ≤ 2.7V	−200	–	40	µA
$I_{IB(D)}$		$V_{I(S/R)}$ = $V_{I(E)}$ = 2.0V; $V_{I(D)}$ = 5.5V	–	–	200	
Receiver Characteristics						
$V_{HYS(R)}$	Receiver Input Hysteresis	$V_{I(S/R)}$ = 0.8V	400	600	–	mV
$V_{ILH(R)}$	Receiver Input Threshold	$V_{I(S/R)}$ = 0.8V, Low to High	–	1.6	1.8	Volts
$V_{IHL(R)}$		$V_{I(S/R)}$ = 0.8V, High to Low	0.8	1.0	–	
$V_{OH(R)}$	Receiver Output Voltage – High Logic State	$V_{I(S/R)}$ = 0.8V, $I_{OH(R)}$ = −800µA, $V_{(BUS)}$ = 2.0V	2.7	–	–	Volts
$V_{OL(R)}$	Receiver Output Voltage – Low Logic State	$V_{I(S/R)}$ = 0.8V, $I_{OL(R)}$ = 16mA, $V_{(BUS)}$ = 0.8V	–	–	0.5	Volts
$I_{OS(R)}$	Receiver Output Short Circuit Current	$V_{I(S/R)}$ = 0.8V, $V_{(BUS)}$ = 2.0V	−15	–	−75	mA
Enable, Send/Receive Characteristics						
$I_{I(S/R)}$	Input Current – Send/Receive	0.5 ≤ $V_{I(S/R)}$ ≤ 2.7V	−100	–	20	µA
$I_{IB(S/R)}$		$V_{I(S/R)}$ = 5.5V	–	–	100	
$I_{I(E)}$	Input Current – Enable	0.5 ≤ $V_{I(E)}$ ≤ 2.7V	−200	–	20	µA
$I_{IB(E)}$		$V_{I(E)}$ = 5.5V	–	–	100	
Power Supply Current						
I_{CCL}	Power Supply Current	Listening Mode – All Receivers On	–	63	85	mA
I_{CCH}		Talking Mode – All Drivers On	–	106	125	

Note 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C unless otherwise noted)

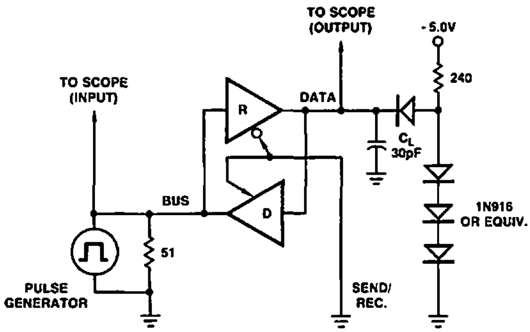
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
$t_{PLH(D)}$	Propagation Delay of Driver (Fig. 2)	Output Low to High	–		15	ns
$t_{PHL(D)}$		Output High to Low			17	
$t_{PLH(R)}$	Propagation Delay of Receiver (Fig. 1)	Output Low to High	–		25	ns
$t_{PHL(R)}$		Output High to Low	–		23	
$t_{PHZ(R)}$	Propagation Delay Time – Send/Receiver to Data (Fig. 4)	Logic High to Third State	–		30	ns
$t_{PZH(R)}$		Third State to Logic High	–		30	
$t_{PLZ(R)}$		Logic Low to Third State	–		30	
$t_{PZL(R)}$		Third State to Logic Low			30	
$t_{PHZ(D)}$	Propagation Delay Time – Send/Receiver to Bus (Fig. 3)	Logic High to Third State	–		30	ns
$t_{PZH(D)}$		Third State to Logic High	–		30	
$t_{PLZ(D)}$		Logic Low to Third State	–		30	
$t_{PZL(D)}$		Third State to Logic Low			30	
$t_{POFF(E)}$	Turn-On Time – Enable to Bus (Fig. 5)	Pull-Up Enable to Open Collector	–		30	ns
$t_{PON(E)}$		Open Collector to Pull-Up Enable	–		20	

TRUTH TABLE

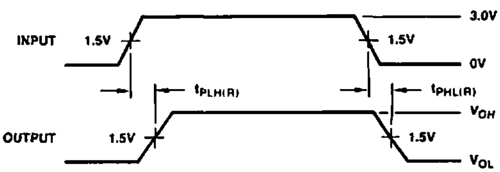
Send/Rec.	Enable	Into Flow	Comments
0	X	Bus → Data	
1	1	Data → Bus	Active Pull-Up
1	0	Data → Bus	Open Collector

X = Don't Care

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

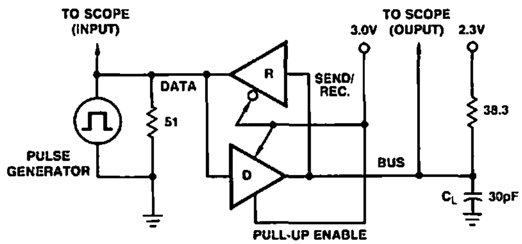


*Includes Jig and Probe Capacitance.

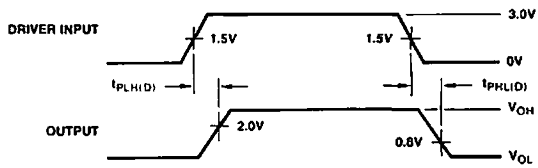


f = 1.0MHz
$t_{TLH} = t_{THL} \leq$ 5.0ns (10-90%)
Duty Cycle = 50%

LIC-449 **Figure 1. Bus Input to Data Output (Receiver).** LIC-450



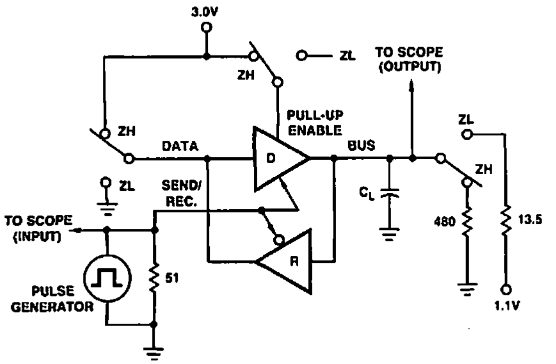
*Includes Jig and Probe Capacitance.



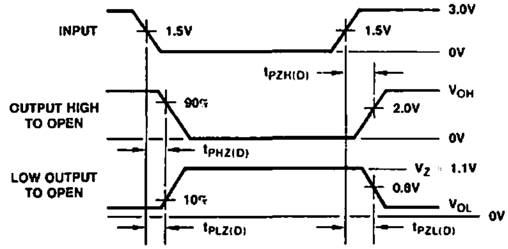
f = 1.0MHz
$t_{TLH} = t_{THL} \leq$ 5.0ns (10-90%)
Duty Cycle = 50%

LIC-451 **Figure 2. Data Input to Bus Output (Driver).** LIC-452

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS (Cont.)

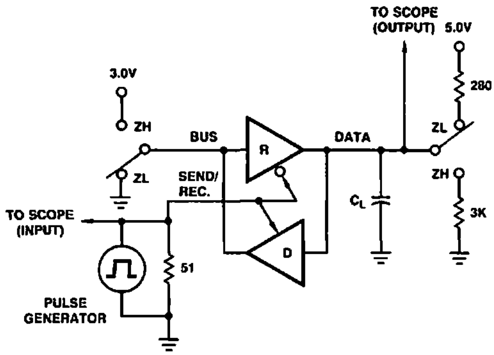


C_L = 15pF (Includes Jig and Probe Capacitance)

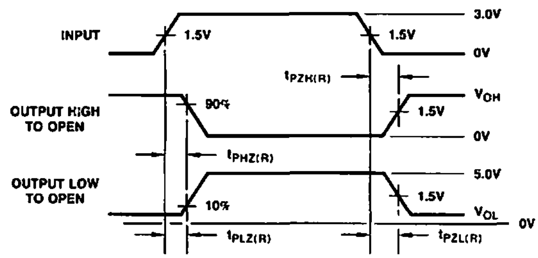


f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0ns$ (10-90%)
Duty Cycle = 50%

LIC-453 **Figure 3. Send/Receive Input to Bus Output (Driver).** LIC-454

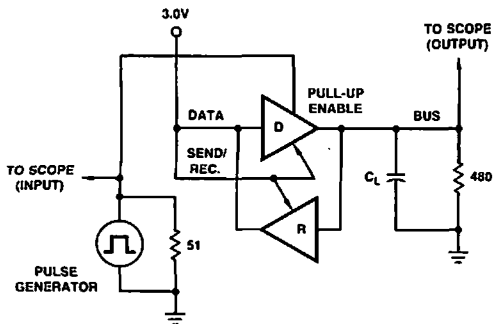


C_L = 15pF (Includes Jig and Probe Capacitance)

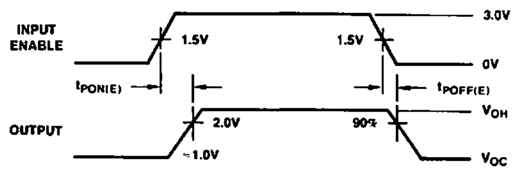


f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0ns$ (10-90%)
Duty Cycle = 50%

LIC-455 **Figure 4. Send/Receive Input to Data Output (Receiver).** LIC-456



C_L = 15pF (Includes Jig and Probe Capacitance)

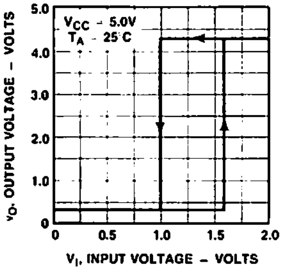


f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0ns$ (10-90%)
Duty Cycle = 50%

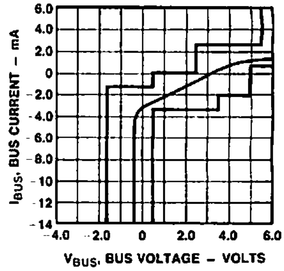
LIC-457 **Figure 5. Enable Input to Bus Output (Driver).** LIC-458

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS (Cont.)

TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

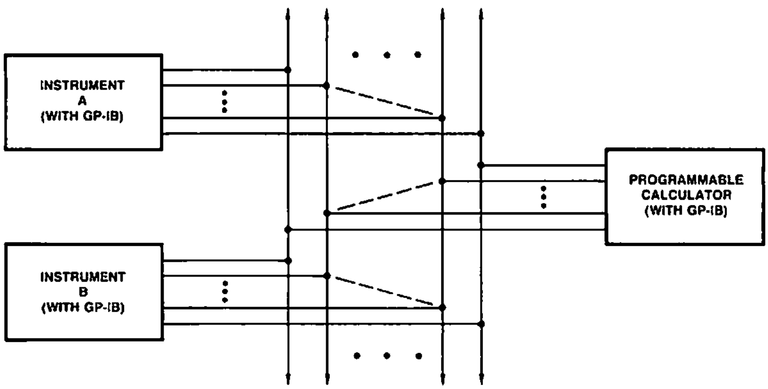


TYPICAL BUS LOAD LINE



LIC-459

TYPICAL APPLICATION



LIC-460

TYPICAL MEASUREMENT SYSTEM APPLICATION

Am54S/74S240 • Am54S/74S241
Am54S/74S242 • Am54S/74S243
Am54S/74S244

Octal Buffers/Line Drivers/Line Receivers With Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Advanced Schottky processing
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- V_{OL} of 0.55V at 64mA for Am74S; 48mA for Am54S
- Data-to-output propagation delay times:
  - Inverting – 7.0ns MAX
  - Non-inverting – 9.0ns MAX
- Enable-to-output – 15.0ns MAX
- 100% reliability assurance testing in compliance with MIL-STD-883
- 20 pin hermetic and molded DIP packages for Am54S/74S240, Am54S/74S241, and Am54S/74S244

FUNCTIONAL DESCRIPTION

These buffers/line drivers, used as memory-address drivers, clock drivers, and bus oriented transmitters/receivers, provide improved PC board density. The outputs of the commercial temperature range versions have 64mA sink and 15mA source capability, which can be used to drive terminated lines down to 133Ω. The outputs of the military temperature range versions have 48mA sink and 12mA source current capability.

Featuring 0.2V minimum guaranteed hysteresis at each low-current PNP data input, they provide improved noise rejection and high-fan-out outputs to restore Schottky TTL levels completely.

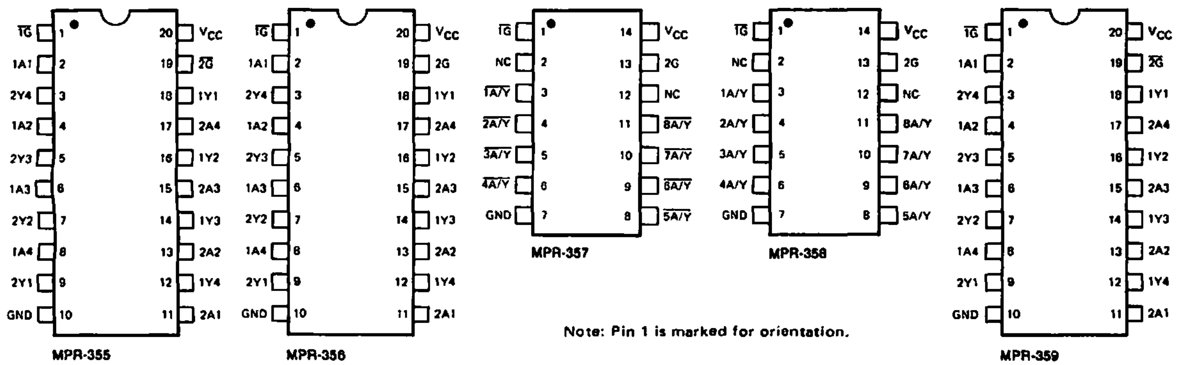
The Am54S/74S240, Am54S/74S241 and Am54S/74S244 have four buffers which are enabled from one common line, and the other four buffers are enabled from another common line. The Am54S/74S240 is inverting, while the Am54S/74S241 and Am54S/74S244 present true data at the outputs.

The Am54S/74S242 and Am54S/74S243 have the two 4-line data paths connected input-to-output on both sides to form an asynchronous transceiver/buffer with complementing enable inputs. The Am54S/74S242 is inverting, while the Am54S/74S243 presents non-inverting data at the outputs.

CONNECTION DIAGRAMS

Top Views

Am54S/74S240 Am54S/74S241 Am54S/74S242 Am54S/74S243 Am54S/74S244



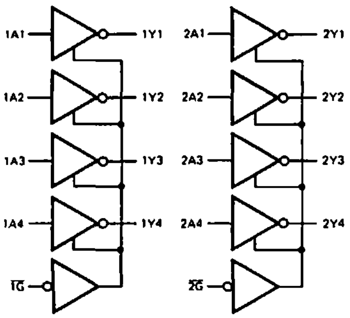
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number Am54S/74S240	Am54S/74S241	Am54S/74S242	Am54S/74S243	Am54S/74S244
Hermetic	–55°C to +125°C	SN54S240J	SN54S241J	SN54S242J	SN54S243J	SN54S244J
Dice	–55°C to +125°C	AM54S240X	AM54S241X	AM54S242X	AM54S243X	AM54S244X
Hermetic	0°C to +70°C	SN74S240J	SN74S241J	SN74S242J	SN74S243J	SN74S244J
Molded	0°C to +70°C	SN74S240N	SN74S241N			SN74S244N
Dice	0°C to +70°C	AM74S240X	AM74S241X	AM74S242X	AM74S243X	AM74S244X

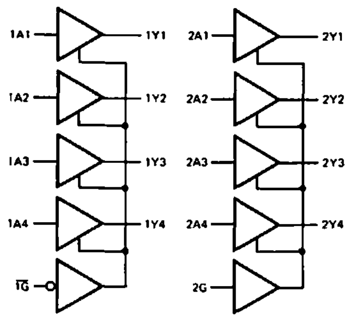
LOGIC DIAGRAMS

Am54S/74S240



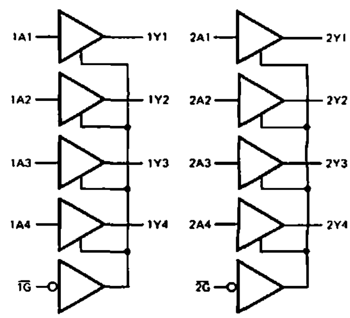
LIC-461

Am54S/74S241



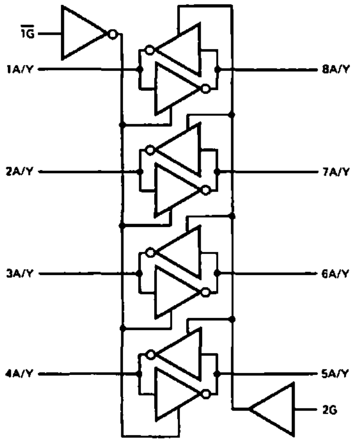
LIC-462

Am54S/74S244



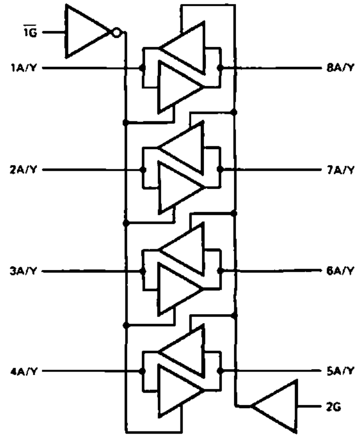
LIC-463

Am54S/74S242



LIC-464

Am54S/74S243



LIC-465

Note: All gates have input hysteresis.

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	–0.5V to $+V_{CC}$ max.
DC Input Voltage	–0.5V to +7.0V
DC Output Current	150mA
DC Input Current	–30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

Am54S240/S241/S242/S243/S244 (MIL)	$T_A = -55°C$ to $+125°C$	V_{CC}(MIN.) = 4.50V	V_{CC}(MAX.) = 5.50V
Am74S240/S241/S242/S243/S244 (COM'L)	$T_A = 0°C$ to $+70°C$	V_{CC}(MIN.) = 4.75V	V_{CC}(MAX.) = 5.25V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{IH}	High-Level Input Voltage				2.0			Volts
V_{IL}	Low-Level Input Voltage						0.8	Volts
V_{IK}	Input Clamp Voltage	V_{CC} = MIN., $I_I = -18mA$					−1.2	Volts
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN.			0.2	0.4		Volts
V_{OH}	High-Level Output Voltage	V_{CC} = MIN. V_{IL} = 0.8V	COM'L, $I_{OH} = -1mA$		2.7			Volts
			$I_{OH} = -3mA$		2.4	3.4		
		V_{CC} = MIN. V_{IL} = 0.5V	MIL, $I_{OH} = -12mA$		2.0			
			COM'L, $I_{OH} = -15mA$		2.0			
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN. V_{IL} = 0.8V	MIL, I_{OL} = 48mA				0.55	Volts
			COM'L, I_{OL} = 64mA				0.55	
I_{OZH}	Off-State Output Current, High-Level Voltage Applied	V_{CC} = MAX. V_{IH} = 2.0V V_{IL} = 0.8V	V_O = 2.4V	'S240, 'S241, 'S244			50	µA
				'S242, 'S243			100	
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied		V_O = 0.5V	'S240, 'S241, 'S244			−50	
				'S242, 'S243			−500	
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX., V_I = 5.5V					1.0	mA
I_{IH}	High-Level Input Current, Any Input	V_{CC} = MAX., V_{IH} = 2.7V					50	µA
I_{IL}	Low-Level Input Current — Any A	V_{CC} = MAX., V_{IL} = 0.5V					−400	µA
	Low-Level Input Current — Any G						−2.0	mA
I_{OS}	Short-Circuit Output Current (Note 3)	V_{CC} = MAX.			−50		−225	mA

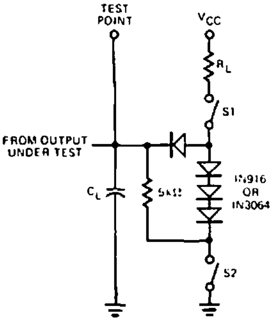
Parameter	Description	Device	Output State	Test Conditions		Typ.	Max.	Units
I_{CC}	Supply Current	Am54S/74S240 Am54S/74S242	All Outputs HIGH	V_{CC} = MAX. Outputs open	MIL	80	123	mA
					COM'L	80	135	
			All Outputs LOW		MIL	100	145	
					COM'L	100	150	
			Outputs at Hi-Z		MIL	100	145	
					COM'L	100	150	
		Am54S/74S241 Am54S/74S243 Am54S/74S244	All Outputs HIGH	V_{CC} = MAX. Outputs open	MIL	95	147	mA
					COM'L	95	160	
			All Outputs LOW		MIL	120	170	
					COM'L	120	180	
			Outputs at Hi-Z		MIL	120	170	
					COM'L	120	180	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25° C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

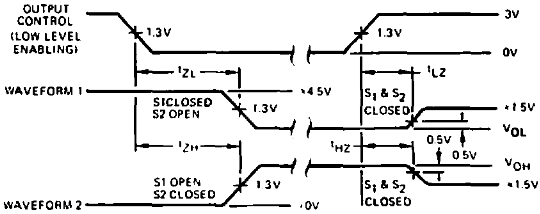
			Am54S/74S240/242			Am54S/74S241/243/244			
Parameter	Description	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	C_L = 50pF, R_L = 90Ω (Note 3)		4.5	7.0		6.0	9.0	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			4.5	7.0		6.0	9.0	ns
t_{ZL}	Output Enable Time to Low Level			10	15		10	15	ns
t_{ZH}	Output Enable Time to High Level			6.5	10		8.0	12	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5.0pF, R_L = 90Ω (Note 3)		10	15		10	15	ns
t_{HZ}	Output Disable Time from High Level			6.0	9.0		6.0	9.0	ns

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



LIC-466

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



LIC-467

Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily. PRR ≤ 1.0MHz, $Z_{OUT} \approx 50\Omega$ and $t_r \leq 2.5ns$, $t_f \leq 2.5ns$.

FUNCTION TABLES

Am54S/74S242

INPUTS			OUTPUTS
$\overline{1G}$	2G	A	Y
H	L	X	Z
L	H	L	H
L	H	H	L

Am54S/74S240

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Am54S/74S241 Am54S/74S243

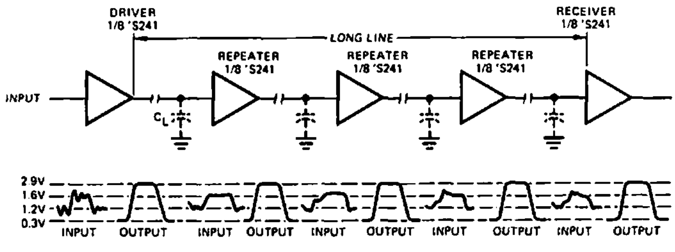
INPUTS			OUTPUTS
$\overline{1G}$	2G	A	Y
H	L	X	Z
L	H	H	H
L	H	L	L

Am54S/74S244

INPUTS		OUTPUT
$\overline{G}$	A	
H	X	Z
L	H	H
L	L	L

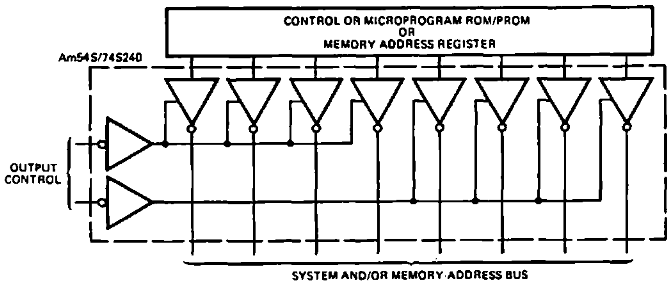
APPLICATIONS

Am54S/74S241'S USED AS REPEATER/LEVEL RESTORER



LIC-468

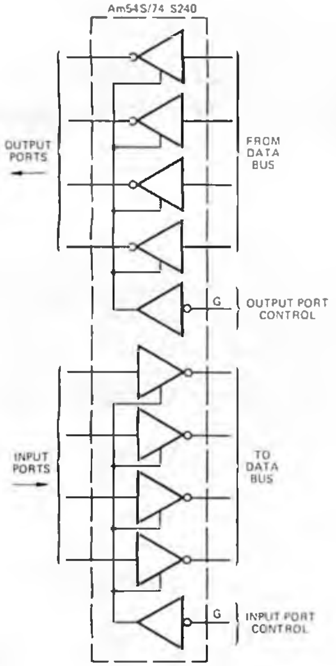
'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER – 4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



LIC-469

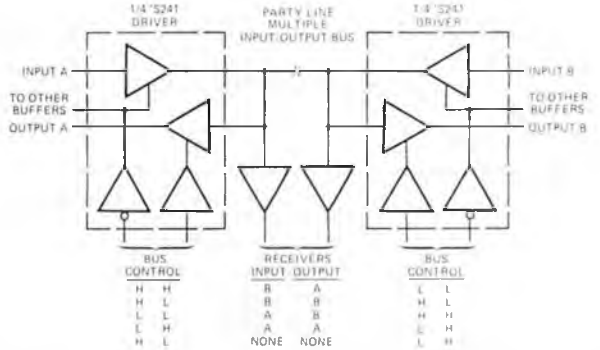
APPLICATIONS (Cont.)

INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



LIC-470

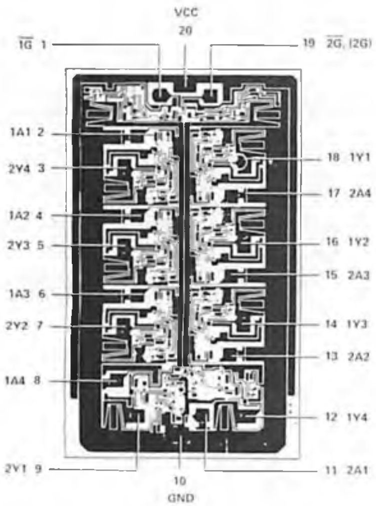
PARTY-LINE BUS SYSTEM WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS



LIC-471

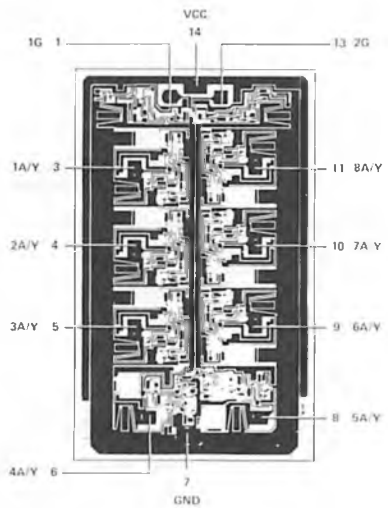
Metallization and Pad Layouts

Am54S/74S240
Am54S/74S241
Am54S/74S244



DIE SIZE 0.077" X 0.124"

Am54S/74S242
Am54S/74S243



DIE SIZE 0.077" X 0.124"

Am55/75107B • Am55/75108B

Dual Line Receivers

Distinctive Characteristics

- Input sensitivity 3mV typical
- Common mode range of ±3V
- Common mode range of more than ±15V using external attenuator
- TTL compatible output
- High common mode rejection ratio
- Blocking diodes provide high input impedance
- Strobe and gate inputs for flexibility
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am55/75107B and Am55/75108B are high speed dual line receivers designed for use as data receivers in balanced, unbalanced or party-line transmission systems. The two line receivers in each package share the common voltage and ground busses. The Am55/75107B has a standard active pull-up totem-pole output while the Am55/75108B has an open collector output for bus organized systems.

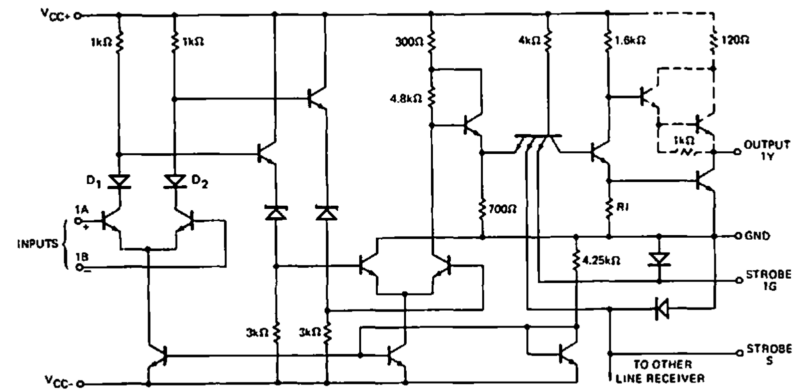
Each receiver has a high impedance differential input for minimum transmission line loading. The differential inputs of the Am55/75107B and Am55/75108B are designed to detect input signals of 25mV or greater and provide TTL compatible outputs.

All devices contain blocking diodes in the input differential transistor pair collectors to provide high input impedance in the power-off condition. The SN55/75107A and SN55/75108A are identical devices except for these input protection diodes.

Each receiver has a separate gate input, G. When the gate is LOW, the output is HIGH regardless of the other inputs. The device also has a common strobe, S, which can be used to gate both receivers simultaneously. When the strobe is LOW, the output is HIGH regardless of the other inputs.

Note: Output HIGH on the Am55/75108B is high impedance condition.

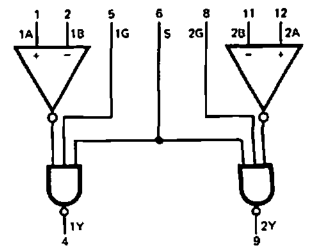
SCHEMATIC DIAGRAM
(One Receiver Shown)



Notes: 1. Components shown with dashed lines are applicable to the Am55/75107B
2. RI = 1kΩ for Am55/75107B and 750Ω for Am55/75108B
3. D1 and D2 are the input protection diodes.

LIC-472

LOGIC SYMBOL



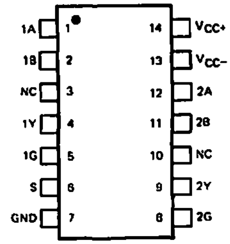
VCC− = Pin 13
VCC+ = Pin 14
GND = Pin 7

LIC-473

ORDERING INFORMATION

Package Type	Temperature Range	Am55/ 75107B Order Number	Am55/ 75108B Order Number
Molded DIP	0°C to +70°C	SN75107BN	SN75108BN
Hermetic DIP	0°C to +70°C	SN75107BJ	SN75108BJ
Dice	0°C to +70°C	AM75107BX	AM75108BX
Hermetic DIP	−55°C to +125°C	SN55107BJ	SN55108BJ
Dice	−55°C to +125°C	AM55107BX	AM55107BX

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.
NC = No connection.

LIC-474

MAXIMUM RATINGS (Above which the useful life may be impaired).

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Positive Supply Voltage V_{CC+} to Ground Potential Continuous	+7.0V
Negative Supply Voltage V_{CC-} to Ground Potential Continuous	−7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to $+V_{CC+}$ max.
DC Input Voltage – Strobe	−0.5V to +5.5V
Differential Input Voltage	±6.0V
Common Mode Input Voltage (with Respect to GND Terminal)	±5.0V
Any Differential Input to Ground	−5.0V to +3.0V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am75107B, Am75108B (COM'L)	T_A = 0°C to 70°C	V_{CC+} = 5.0 V ± 5%	V_{CC-} = −5.0 V ± 5% (COM'L)
Am55107B, Am55108B (MIL)	T_A = −55°C to +125°C	V_{CC+} = 5.0 V ± 10%	V_{CC-} = −5.0 V ± 5% (MIL)

Parameters	Description	Test Conditions (Notes 1, 4, & 5)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Am55/75107B Only)	V_{CC+} = MIN., V_{CC-} = MIN. I_{OH} = −400μA, V_{IC} = −3V to 3V		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC+} = MIN., V_{CC-} = MIN. I_{OL} = 16mA, V_{IC} = −3V to 3V				0.4	Volts
V_{IH}	Strobe or gate input HIGH Voltage	See Test Table		2.0			Volts
V_{IL}	Strobe or Gate Input LOW Voltage	See Test Table				0.8	Volts
V_{IDH}	Differential Input Voltage for Output HIGH	See Test Table		0.025		5.0	Volts
V_{IDL}	Differential Input Voltage for Output LOW	See Test Table		−5.0		−0.025	Volts
I_{IH}	Input HIGH Current into 1A or 2A	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Input LOW Current into 1A or 2A	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	Input HIGH Current	V_{CC+} = MAX., V_{CC-} = MAX. V_{IH} = 2.4V	S			80	μA
			G			40	
I_I	Input HIGH Current	V_{CC+} = MAX., V_{CC-} = MAX. V_{IH} = V_{CC+} MAX.	S			2	mA
			G			1	
I_{IL}	Input LOW Current	V_{CC+} = MAX., V_{CC-} = MAX. V_{IL} = 0.4V	S			−3.2	mA
			G			−1.6	
I_{OH}	HIGH Level Output Leakage (Am55/75108B Only)	V_{CC+} = MIN., V_{CC-} = MIN. V_{OH} = V_{CC+} MAX.				250	μA
I_{SC}	Output Short Circuit Current (Note 3) (Am55/75107B Only)	V_{CC+} = MAX., V_{CC-} = MAX.		−18		−70	mA
I_{CCH+}	Positive Power Supply Current	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = 25mV, T_A = 25°C			18	30	mA
I_{CCH-}	Negative Power Supply Current	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = 25mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage, S or G	V_{CC+} = MIN., V_{CC-} = MIN. I_{IN} = −12mA, T_A = 25°C			−1	−1.5	Volts

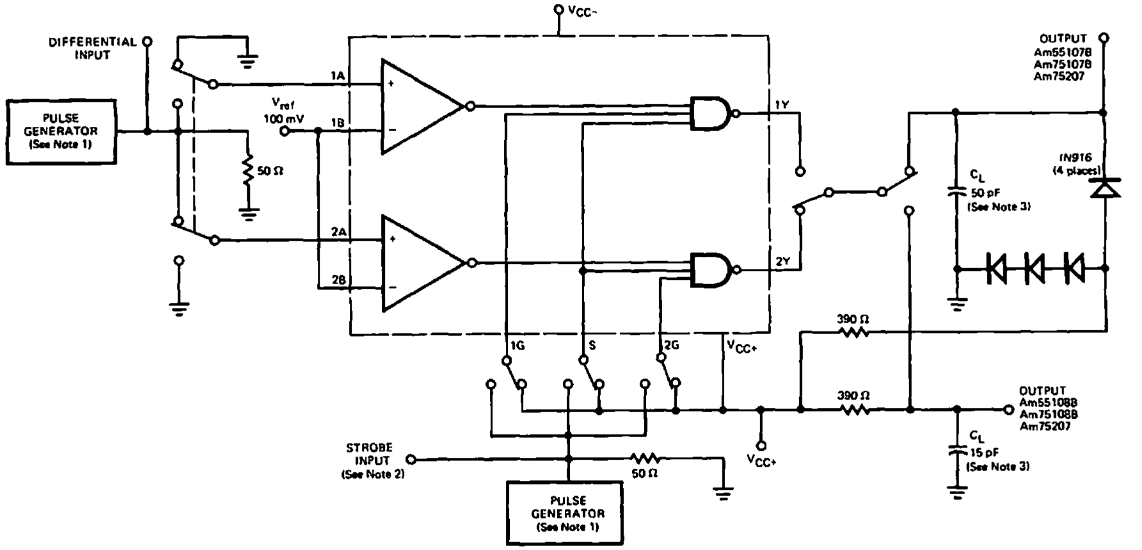
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC+} = 5.0V, V_{CC-} = −5.0V, T_A = 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. V_{IC} = common mode voltage with respect to GND terminal.
V_{ID} = differential voltage ($V_A - V_B$).

SWITCHING CHARACTERISTICS (T_A = +25°C, $V_{CC}+$ = 5V, $V_{CC}-$ = –5V)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
Am55/75107B Only						
t_{PLH}	A and B to Output	R_L = 390Ω C_L = 50 pF		17	25	ns
t_{PHL}	A and B to Output			17	25	ns
t_{PLH}	G or S to Output			10	15	ns
t_{PHL}	G or S to Output			8	15	ns
Am55/75108B Only						
t_{PLH}	A and B to Output	R_L = 390Ω C_L = 15 pF		19	25	ns
t_{PHL}	A and B to Output			19	25	ns
t_{PLH}	G or S to Output			13	20	ns
t_{PHL}	G or S to Output			13	20	ns

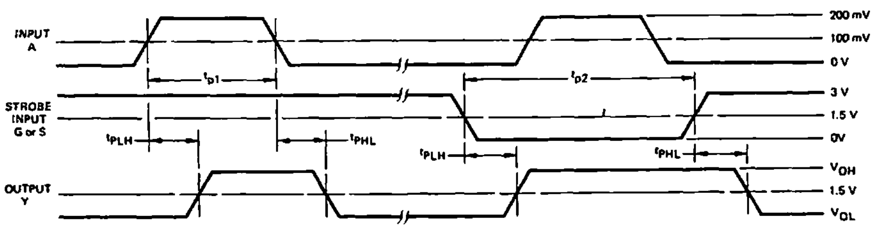
AC PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT



LIC-475

VOLTAGE WAVEFORMS



Notes: 1. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = t_f = 10 ± 5 ns, t_{p1} = 500 ns, PRR = 1 MHz, t_{p2} = 1 ms, PRR = 500 kHz.

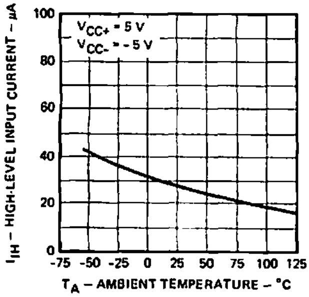
2. Strobe input pulse is applied to Strobe 1G when inputs 1A – 1B are being tested, to Strobe S when inputs 1A – 1B or 2A – 2B are being tested, and to Strobe 2G when inputs 2A – 2B are being tested.

3. C_L includes probe and jig capacitance.

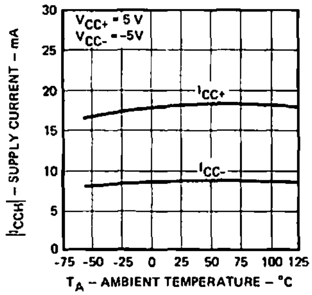
LIC-476

PERFORMANCE CURVES

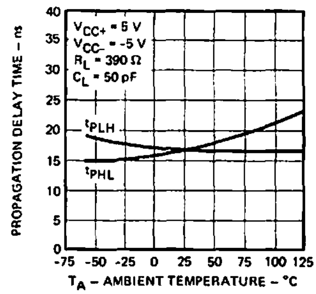
High-Level Input Current Into 1A or 2A Versus Ambient Temperature



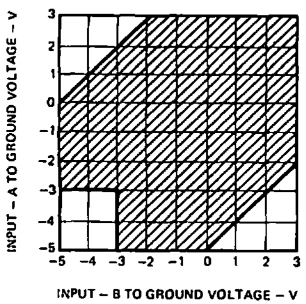
High-Logic-Level Supply Current Versus Ambient Temperature



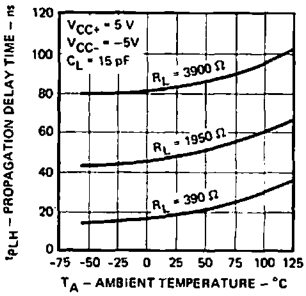
Am55107B, Am75107B Propagation Delay Time Differential Inputs Versus Ambient Temperature



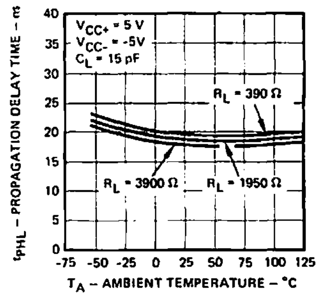
Recommended Combinations of Input Voltage for Line Receivers



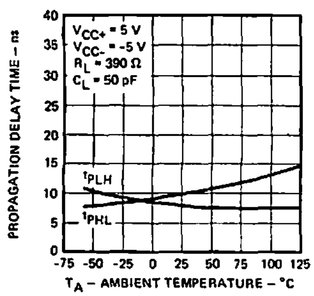
Am55108B, Am75108B Propagation Delay Time Low-to-High Level Differential Inputs Versus Ambient Temperature



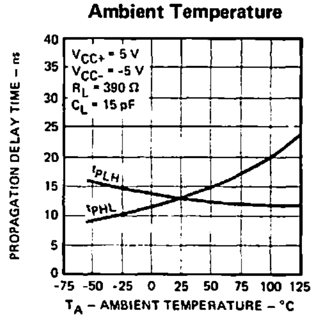
Am55108B, Am75108B Propagation Delay Time High-to-Low Level Differential Inputs Versus Ambient Temperature



Am55107B, Am75107B Propagation Delay Time Strobe Inputs Versus Ambient Temperature



Am55108B, Am75108B Propagation Delay Time Strobe Inputs Versus Ambient Temperature



Note: Use 0°C to +70°C temperature range only for commercial (Am75 Series) devices.

LIC-477

FUNCTION TABLE

Differential Input Voltage $V_{ID} = V_A - V_B$	Inputs: Gate G	Inputs: Strobe S	Output Y
$V_{ID} \geq +25mV$	X	X	H
$-25mV < V_{ID} < +25mV$	H	H	?
$V_{ID} \leq -25mV$	H	H	L
X	L	X	H
X	X	L	H

H = HIGH
L = LOW
X = Don't Care
? = Don't Know

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

DEFINITION OF FUNCTIONAL TERMS

1A, 2A The non-inverting input of the line receivers.

1B, 2B The inverting input of the line receivers.

1Y, 2Y The output of each line receiver.

1G, 2G The gate input of each line receiver. A LOW on the gate input forces the output HIGH.

S The strobe input that is common to both line receivers. A LOW on the strobe forces both (1Y and 2Y) outputs HIGH.

V_{IC} Input Common Mode voltage with respect to ground terminal.

V_{ID} Differential Input voltage ($V_A - V_B$).

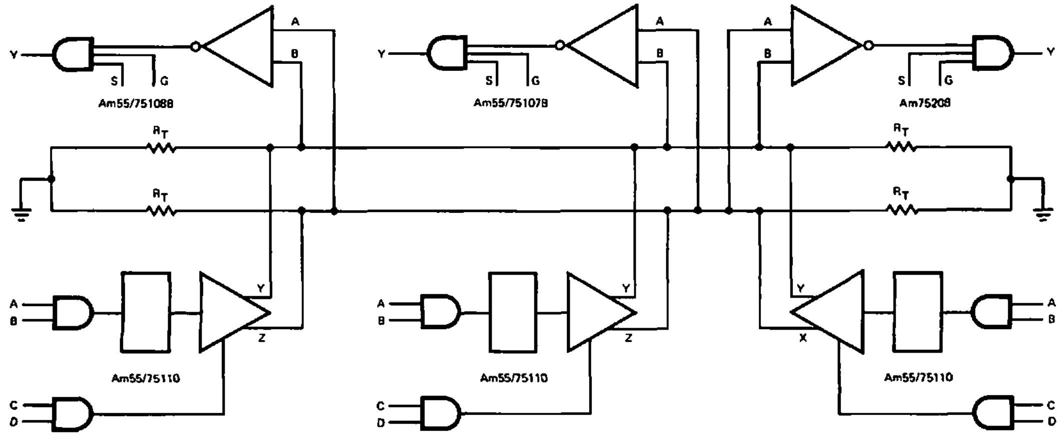
DC TEST TABLE

Parameter	1A	2A	1B 2B	V_{IC} (Common Mode)	V_{ID} (Differential)	1Y 2Y	1G	2G	S	Note
V_{IDH}	–		–	–3V to 3V	Test	–400μA (Note 2)	+5V		+5V	1
V_{IDL}	–		–	–3V to 3V	Test	16mA	+5V		+5V	1
I_{IH} @ A	–		–	–3V to 3V	+0.5V	Open	Open		Open	1
I_{IL} @ A	–		–	–3V to 3V	–2V	Open	Open		Open	1
V_{OL} @ Y	–		–	–3V to 3V	–25mV	16mA	V_{IH}		V_{IH}	1
V_{OH} @ Y	–		–	–3V to 3V	+25mV	–400μA	V_{IH}		V_{IH}	1 & 2
V_{OH} @ Y	–		–	–3V to 3V	–25mV	–400μA	V_{IL}		V_{IH}	1 & 2
V_{OH} @ Y	–		–	–3V to 3V	–25mV	–400μA	V_{IH}		V_{IL}	1 & 2
I_{OH} @ Y	–		–	–3V to 3V	+25mV	V_{CC+}MAX.	V_{IH}		V_{IH}	1 & 3
I_{OH} @ Y	–		–	–3V to 3V	–25mV	V_{CC+}MAX.	V_{IL}		V_{IH}	1 & 3
I_{OH} @ Y	–		–	–3V to 3V	–25mV	V_{CC+}MAX.	V_{IH}		V_{IL}	1 & 3
I_{IH} @ 1G	+25mV	GND	GND	–	–	Open	V_{IH}	GND	GND	–
I_{IH} @ 2G	GND	+25mV	GND	–	–	Open	GND	V_{IH}	GND	–
I_{IH} @ S	+25mV	+25mV	GND	–	–	Open	GND	GND	V_{IH}	–
I_{IL} @ 1G	–25mV	GND	GND	–	–	Open	V_{IL}	GND	4.5V	–
I_{IL} @ 2G	GND	–25mV	GND	–	–	Open	GND	V_{IL}	4.5V	–
I_{IL} @ S	–25mV	–25mV	GND	–	–	Open	4.5V	4.5V	V_{IL}	–
I_{OS} @ Y	+25mV		GND	–	–	GND	GND		GND	–
I_{CC+}	+25mV		GND	–	–	Open	+5V		+5V	–
I_{CC-}	+25mV		GND	–	–	Open	+5V		+5V	–

Notes: 1. When testing one channel, the inputs of the other channels are grounded.
2. Am55/75107B only.
3. Am55/75108B only.

APPLICATIONS

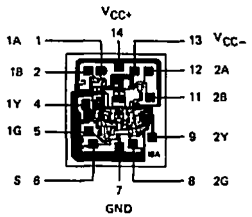
BUS-ORGANIZED SYSTEM



LIC-478

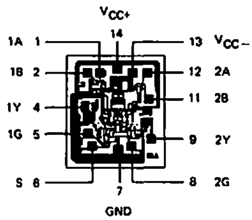
Metallization and Pad Layouts

Am55/75107B



DIE SIZE: 0.049" X 0.056"

Am55/75108B



DIE SIZE: 0.049" X 0.056"

Am55/75109 • Am55/75110

Dual Line Drivers

Distinctive Characteristics

- Input is TTL compatible.
- High common-mode output range of −3V to +10V.
- Separate and common output inhibits.
- Open-collector differential outputs for bus-organized systems.
- 100% reliability assurance testing in compliance with MIL-STD-883.

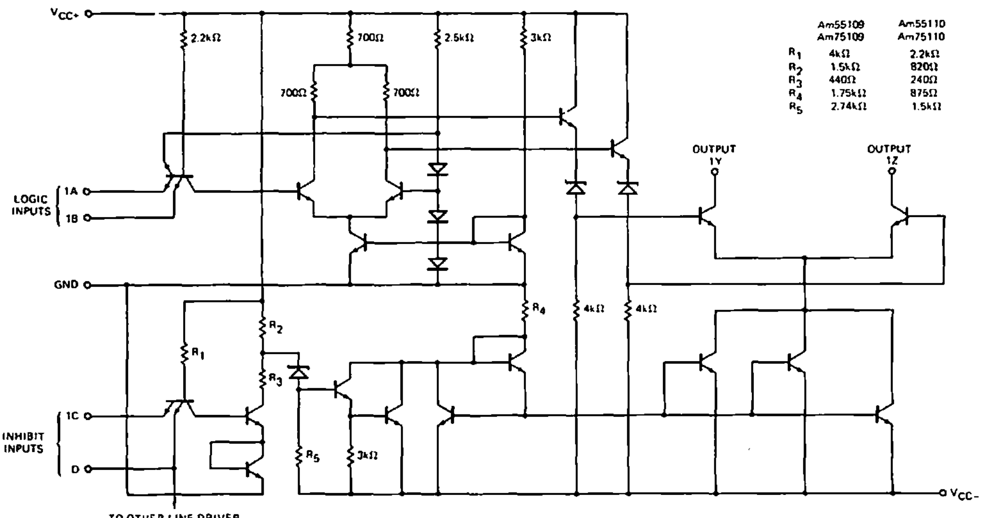
FUNCTIONAL DESCRIPTION

The Am55/75109 and Am55/75110 are dual line drivers characterized for applications in balanced, unbalanced, and party-line systems. The drivers provide a constant current output that is switched to either of the two differential output terminals under the control of the A and B inputs. When A and B are HIGH, the Y output is HIGH and Z output is LOW

These drivers feature a separate inhibit input, C, that is used to switch off the constant current output. This leaves the driver differential output in the high impedance state for use in bus organized systems. A LOW on the C input forces the driver to the OFF state by switching off the current source of the differential output transistor pair. Likewise, the two drivers have a common inhibit input, D, that forces both drivers to the OFF state. A LOW on the D inputs turns off the output current sources of both drivers such that both differential outputs are in the high impedance state.

The driver outputs have a common mode voltage range of −3V to +10V. The Am55/75109 output current is typically 6mA while the Am55/75110 output current is typically 12mA.

SCHEMATIC DIAGRAM
(One Driver Shown)



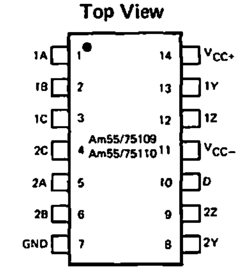
Notes: 1. Component values shown are nominal.
2. Resistance values are in ohms.

LIC-479

ORDERING INFORMATION

Package Type	Temperature Range	Am55/75109 Order Number	Am55/75110 Order Number
Molded DIP	0°C to +70°C	SN75109N	SN75110N
Hermetic DIP	0°C to +70°C	SN75109J	SN75110J
Dice	0°C to +70°C	AM75109X	AM75110X
Hermetic DIP	−55°C to +125°C	SN55109J	SN55110J
Dice	−55°C to +125°C	AM55109X	AM55110X

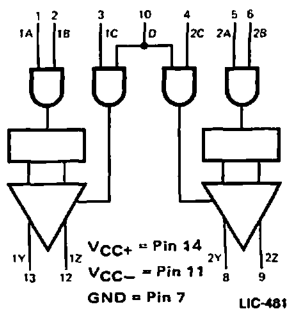
CONNECTION DIAGRAM
Top View



LIC-480

Note:
Pin 1 is marked for orientation.

LOGIC SYMBOL



LIC-481

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC+} Supply Voltage to Ground Potential	+7V
V_{CC-} Supply Voltage to Ground Potential	−7V
Common Mode DC Voltage Applied to Outputs	−5V to +12V
DC Input Voltage	−0.5V to $+V_{CC+}$max.
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am75109, Am75110	V_{CC+} MIN. = 4.75V	V_{CC+} MAX. = 5.25V,	V_{CC-} MIN. = −4.75V	V_{CC-} MAX. = −5.25V;	T_A = 0°C to +70°C
Am55109, Am55110	V_{CC+} MIN. = 4.5V	V_{CC+} MAX. = 5.5V,	V_{CC-} MIN. = −4.5V	V_{CC-} MAX. = −5.5V;	T_A = −55°C to +125°C

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0		5.5	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		0		0.8	Volts
I_{IL} (Note 3)	Input Low Current Am55/75109	V_{CC+} = MAX., V_{IN} = 0.4 V, V_{CC-} = MAX.	A, B			−3	mA
			C			−1.6	
			D			−3	
I_{IL} (Note 3)	Input LOW Current Am55/75110	V_{CC+} = MAX., V_{IN} = 0.4 V, V_{CC-} = MAX.	A, B, C			−3	mA
			D			−6	
I_{IH} (Note 3)	Input HIGH Current	V_{CC+} = MAX., V_{IN} = 2.4 V, V_{CC-} = MAX.	A, B, C			40	µA
			D			80	
I_I	Input HIGH Current	V_{CC+} = MAX., V_{IN} = MAX., V_{CC-} = MAX.	A, B, C			1	mA
			D			2	
I_O(on)	Output Current On-State	V_{CC+} = MAX., V_{CC-} = MAX.	109			7	mA
			110			15	
I_O(on)	Output Current On-State	V_{CC+} = MIN., V_{CC-} = MAX.	109	3.5			mA
			110	6.5			
I_O(off)	Output Current Off-State	V_{CC+} = MIN., V_{CC-} = MIN.				100	µA
I_{CC+}(on)	Positive Supply Current; Driver Enabled	A and B = 0.4V, C and D = 2.0V	109		18	30	mA
			110		23	35	
I_{CC-}(on)	Negative Supply Current; Driver Enabled	A and B = 0.4V, C and D = 2.0V	109		−18	−30	mA
			110		−34	−50	
I_{CC+}(off)	Positive Supply Current; Driver Disabled	All Inputs = 0.4V	109		18		mA
			110		21		
I_{CC-}(off)	Negative Supply Current; Driver Disabled	All Inputs = 0.4V	109		−10		mA
			110		−17		

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC+} = 5.0V, V_{CC-} = −5.0V, T_A = 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current X Input Load Factor (See Loading Rules).

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	A or B to Y or Z	V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, R_L = 50Ω, C_L = 40 pF		9	15	ns
t_{PHL}	A or B to Y or Z			9	15	ns
t_{PLH}	C or D to Y or Z			16	25	ns
t_{PHL}	C or D to Y or Z			13	25	ns

FUNCTION TABLE

LOGIC INPUTS		INHIBIT INPUTS		OUTPUTS	
A	B	C	D	Y	Z
X	X	L	X	OFF	OFF
X	X	X	L	OFF	OFF
L	X	H	H	ON	OFF
X	L	H	H	ON	OFF
H	H	H	H	OFF	ON

H = HIGH
L = LOW
ON = I_O(on) Current
OFF = I_O(off) Current
X = Don't Care

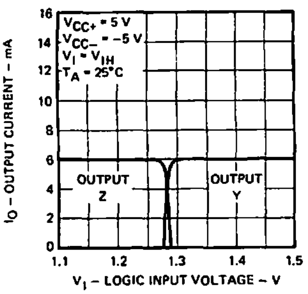
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load Am55/ 75109	Input Unit Load Am55/ 75110	Fan-out Output HIGH	Fan-out Output LOW
1A	1	1-7/8	1-7/8	–	–
1B	2	1-7/8	1-7/8	–	–
1C	3	1	1-7/8	–	–
2C	4	1	1-7/8	–	–
2A	5	1-7/8	1-7/8	–	–
2B	6	1-7/8	1-7/8	–	–
GND	7	–	–	–	–
2Y	8	–	–	(Diff output)	–
2Z	9	–	–		
D	10	1-7/8	3-3/4	–	–
V_{CC-}	11	–	–	–	–
1Z	12	–	–	(Diff output)	–
1Y	13	–	–		
V_{CC+}	14	–	–	–	–

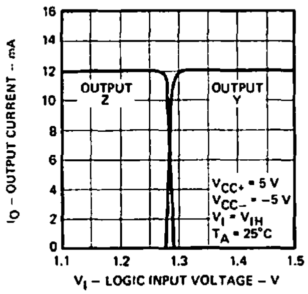
A TTL Unit Load is defined as 40 μA measured at 2.4 V HIGH and −1.6mA measured at 0.4 V LOW.

PERFORMANCE CURVES
(Typical)

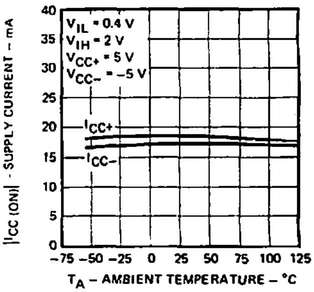
Am55109, Am75109
Output Current Versus Logic Input Voltage



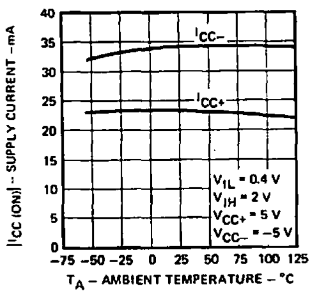
Am55110, Am75110
Output Current Versus Logic Input Voltage



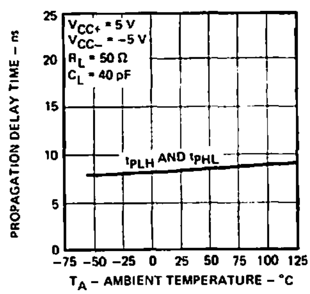
Am55109, Am75109
Supply Current With Driver Enabled Versus Ambient Temperature



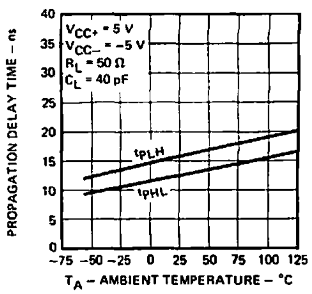
Am55110, Am75110
Supply Current With Driver Enabled Versus Ambient Temperature



Propagation Delay Time Logic Inputs Versus Ambient Temperature



Propagation Delay Time Inhibit Inputs Versus Ambient Temperature



Note: For Am75 Series use 0°C to +70°C temperature range only.

LIC-482

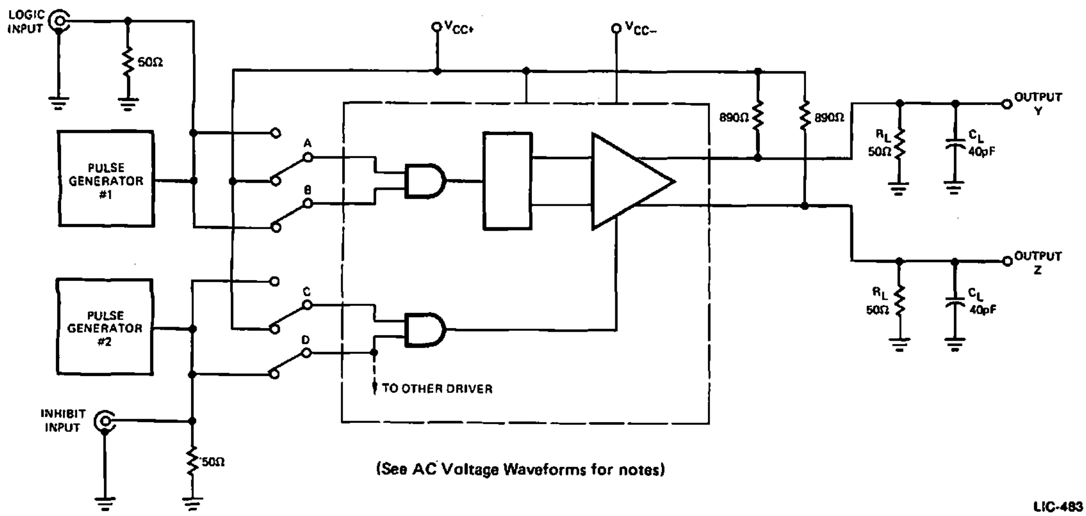
DC TEST TABLE

Parameter	INPUTS A	B	C	D	OUTPUTS Y	Z
V_{IH}	Test	Open	V_{IH}	V_{IH}	OFF	ON
V_{IH}	Open	Test	V_{IH}	V_{IH}	OFF	ON
V_{IL}	Test	V_{CC+}	V_{IH}	V_{IH}	ON	OFF
V_{IL}	V_{CC+}	Test	V_{IH}	V_{IH}	ON	OFF
I_{IH}	Test	GND	V_{IH}	V_{IH}	GND	GND
I_{IH}	GND	Test	V_{IH}	V_{IH}	GND	GND
I_{IL}	Test	4.5 V	V_{IH}	V_{IH}	GND	GND
I_{IL}	4.5 V	Test	V_{IH}	V_{IH}	GND	GND
V_{IH}	V_{IH}	V_{IH}	Test	Open	OFF	ON
V_{IH}	V_{IH}	V_{IH}	Open	Test	OFF	ON
V_{IH}	V_{IL}	V_{IL}	Test	Open	ON	OFF
V_{IH}	V_{IL}	V_{IL}	Open	Test	ON	OFF
V_{IL}	V_{IH}	V_{IH}	Test	Open	OFF	OFF
V_{IL}	V_{IH}	V_{IH}	Open	Test	OFF	OFF
V_{IL}	V_{IL}	V_{IL}	Test	V_{CC+}	OFF	OFF
V_{IL}	V_{IL}	V_{IL}	V_{CC+}	Test	OFF	OFF
I_{IH}	GND	GND	Test	GND	GND	GND
I_{IH}	GND	GND	GND	Test	GND	GND
I_{IL}	GND	GND	Test	4.5 V	GND	GND
I_{IL}	GND	GND	4.5 V	Test	GND	GND
$I_{O(on)}$	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Test	Note 1
$I_{O(on)}$	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Test	Note 1
$I_{O(on)}$	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Test	Note 1
$I_{O(on)}$	V_{IH}	V_{IH}	V_{IH}	V_{IH}	Note 1	Test
$I_{O(off)}$	V_{IH}	V_{IH}	V_{IH}	V_{IH}	Test	Note 1
$I_{O(off)}$	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Note 1	Test
$I_{O(off)}$	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Note 1	Test
$I_{O(off)}$	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Note 1	Test
$I_{O(off)}$	X	X	V_{IL}	V_{IL}	Test	Test
$I_{O(off)}$	X	X	V_{IL}	V_{IH}	Test	Test
$I_{O(off)}$	X	X	V_{IH}	V_{IL}	Test	Test
$I_{CC+(on)}$	V_{IL}	V_{IL}	V_{IH}	V_{IH}	GND	GND
$I_{CC-(on)}$	V_{IL}	V_{IL}	V_{IH}	V_{IH}	GND	GND
$I_{CC+(off)}$	V_{IL}	V_{IL}	V_{IL}	V_{IL}	GND	GND
$I_{CC-(off)}$	V_{IL}	V_{IL}	V_{IL}	V_{IL}	GND	GND

X = Don't Care; Note 1: Output not under test must have a low impedance (<50Ω) termination to GND.

AC PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

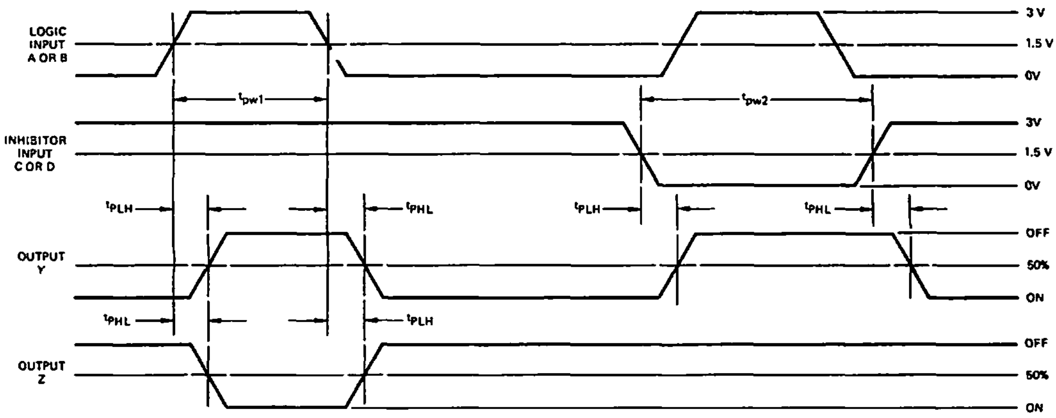


(See AC Voltage Waveforms for notes)

LIC-483

4

AC VOLTAGE WAVEFORMS



Notes: 1. The pulse generators have the following characteristics: $Z_{out} = 50\Omega$, $t_r = t_f = 10 \pm 5ns$; $t_{pw1} = 500ns$, PRR = 1 MHz; $t_{pw2} = 1\mu s$, PRR = 500kHz.

2. C_L includes probe and jig capacitance.

3. For simplicity, only one channel and the inhibitor connections are shown.

LIC-484

UNIT LOAD DEFINITIONS

SERIES	HIGH Current	HIGH Measure Voltage	LOW Current	LOW Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0mA	0.5V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

DEFINITION OF FUNCTIONAL TERMS

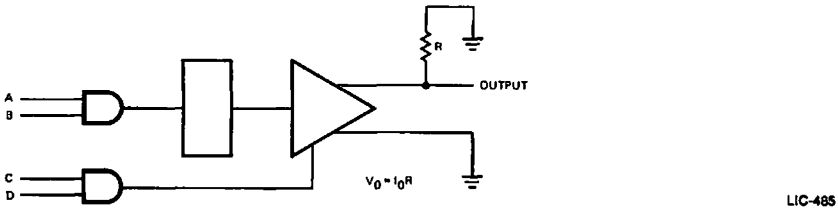
1A, 2A, 1B, 2B The TTL data inputs to each driver.

1C, 2C The TTL inhibit inputs to each driver. A LOW input forces both outputs to the off-state.

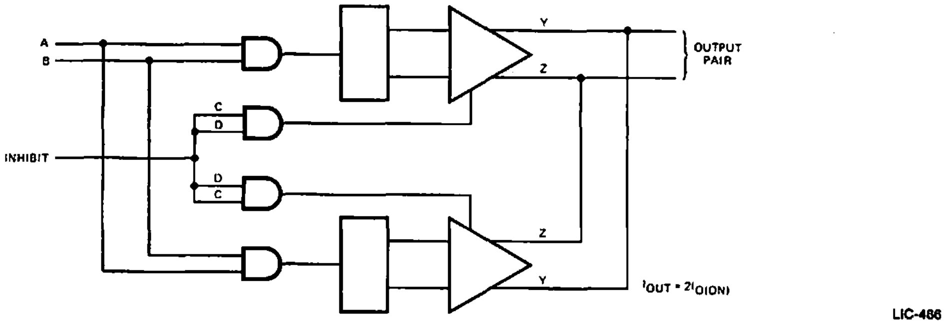
D The common TTL inhibit input to both drivers. A LOW input forces all four outputs to the off-state.

1Y, 2Y, 1Z, 2Z The differential output of each driver.

APPLICATIONS



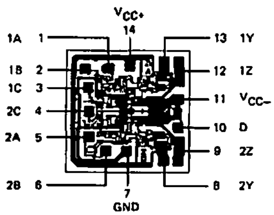
Am55/75109 or Am55/75110 in a unbalanced or single-ended connection.



Two line drivers connected in parallel for higher current.

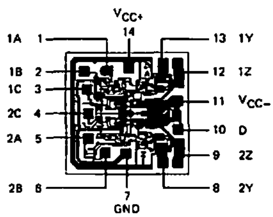
Metallization and Pad Layouts

Am55/75109



DIE SIZE 0.056" X 0.056"

Am55/75110



DIE SIZE 0.056" X 0.056"

Am71/81LS95 • Am71/81LS96
Am71/81LS97 • Am71/81LS98

Three-State Octal Buffers

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus line directly
- Typical propagation delay
  Am71/81LS95, Am71/81LS97 13ns
  Am71/81LS96, Am71/81LS98 10ns
- Typical power dissipation
  Am71/81LS95, Am71/81LS97 80mW
  Am71/81LS96, Am71/81LS98 65mW
- PNP inputs reduce DC loading on bus lines
- Am71/81LS96 and Am71/81LS98 are inverting; Am71/81LS95 and Am71/81LS97 are non-inverting
- 20-pin hermetic and molded DIP packages
- 100% product assurance testing to MIL-STD-883 requirements

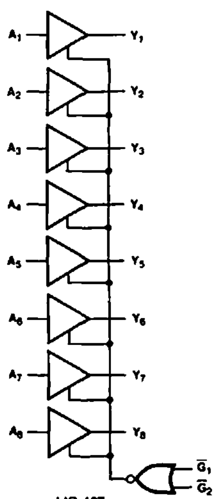
GENERAL DESCRIPTION

The Am71/81LS95, Am71/81LS96, Am71/81LS97 and Am71/81LS98 are octal buffers fabricated using Advanced Low-Power Schottky technology. The 20-pin package provides improved printed circuit board density for use in memory address and clock driver applications.

The Am71/81LS95 and Am71/81LS97 present true data at the outputs, while the Am71/81LS96 and Am71/81LS98 are inverting. The Am71/81LS95 and Am71/81LS96 have a common enable for all eight buffers with access through a 2-input NOR gate. The Am71/81LS97 and Am71/81LS98 octal buffers have four buffers enabled from one common line, and the other four buffers enabled from another common line. In all cases the outputs are placed in the three-state condition by applying a high logic level to the enable pins. All parts feature low current PNP inputs.

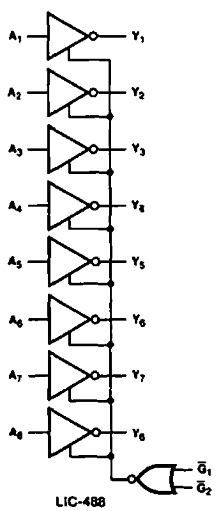
LOGIC DIAGRAMS

Am71/81LS95



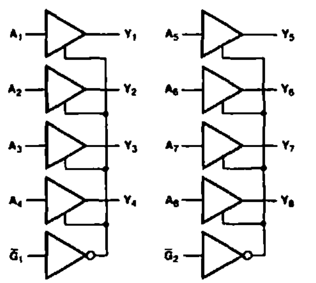
LIC-487

Am71/81LS96



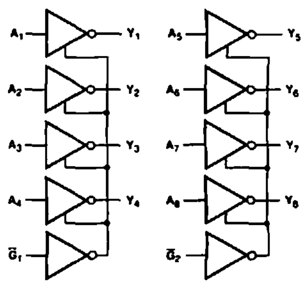
LIC-488

Am71/81LS97



LIC-489

Am71/81LS98



LIC-490

'LS95

INPUTS			OUTPUT
$\overline{G}_1$	$\overline{G}_2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

'LS96

INPUTS			OUTPUT
$\overline{G}_1$	$\overline{G}_2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

'LS97

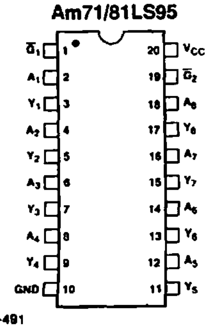
INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

'LS98

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

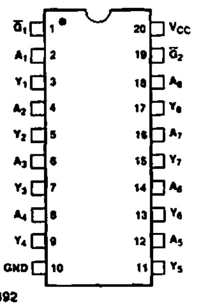
CONNECTION DIAGRAMS – Top Views

Am71/81LS95



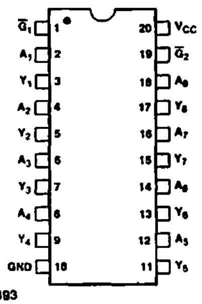
LIC-491

Am71/81LS96



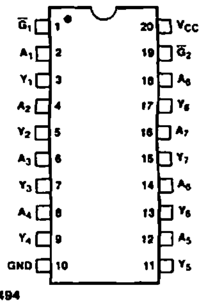
LIC-492

Am71/81LS97



LIC-493

Am71/81LS98



LIC-494

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to $+V_{CC}$ max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current	150mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Am71/81LS95
Am71/81LS96
Am71/81LS97
Am71/81LS98

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{IH}	High Level Input Voltage		2			Volts
V_{IL}	Low Level Input Voltage				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min., I_I = −18mA			−1.5	Volts
I_{OH}	High Level Output Current	MIL			−1.0	mA
		COM'L			−2.6	
V_{OH}	High Level Output Voltage	V_{CC} = Min., V_{IH} = 2.0V, V_{IL} = 0.8V; COM'L, I_{OH} = −5.0mA	2.4			Volts
		V_{CC} = Min., V_{IH} = 2.0V, V_{IL} = 0.8V; COM'L, I_{OH} = −2.6mA	2.7			
		V_{CC} = Min., V_{IH} = 2.0V, V_{IL} = 0.8V; MIL, I_{OH} = −1.0mA	2.5			
I_{OL}	Low Level Output Current	COM'L			16	mA
		MIL			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min., V_{IH} = 2.0V, V_{IL} = 0.8V; COM'L, I_{OL} = 16mA			0.5	V
		V_{CC} = Min., V_{IH} = 2.0V, V_{IL} = 0.8V; MIL, I_{OL} = 8.0mA			0.4	
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max., V_{IH} =2.0V, V_{IL} = 0.8V; V_O = 0.4V			−20	μA
		V_{CC} = Max., V_{IH} =2.0V, V_{IL} = 0.8V; V_O = 2.4V			20	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max., V_I = 7.0V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max., V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current, A Input	V_{CC} = Max.; Both $\overline{G}$ Inputs at 2.0V; V_I = 0.5V			−50	μA
	Low Level Input Current, A Input	V_{CC} = Max.; Both $\overline{G}$ Inputs at 0.4V; V_I = 0.4V			−0.36	mA
	Low Level Input Current, $\overline{G}$ Input	V_{CC} = Max.; V_I = 0.4V			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max. (Note 2)	−30	−60	−130	mA
I_{CC}	Supply Current	V_{CC} = Max.; Am71/81LS95, Am71/81LS97		16	26	mA
		V_{CC} = Max.; Am71/81LS96, Am71/81LS98		13	21	

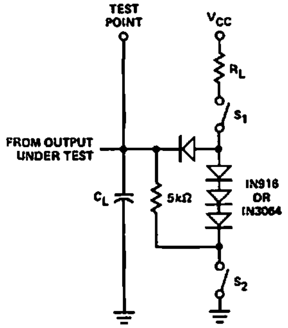
Notes: 1. All typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Not more than output should be shorted at a time, and duration of the short circuit should not exceed one second.

SWITCHING CHARACTERISTICS V_{CC} = 5.0V, T_A = 25°C

Parameters	Description	Test Conditions	Am71/81LS95, Am71/81LS97 Min.	Typ.	Max.	Am71/81LS96, Am71/81LS98 Min.	Typ.	Max.	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15pF, R_L = 2kΩ		11	16		6	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15pF, R_L = 2kΩ		15	22		13	17	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15pF, R_L = 2kΩ		16	25		17	27	ns
t_{ZL}	Output Enable Time to Low Level	C_L = 15pF, R_L = 2kΩ		13	20		16	25	ns
t_{HZ}	Output Disable Time from HIGH Level	C_L = 5pF, R_L = 2kΩ		13	20		13	20	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5pF, R_L = 2kΩ		19	27		18	27	

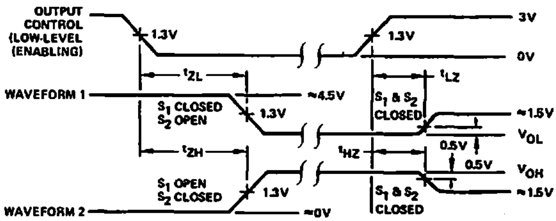
SWITCHING CHARACTERISTICS TEST CONDITIONS

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



LIC-495

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

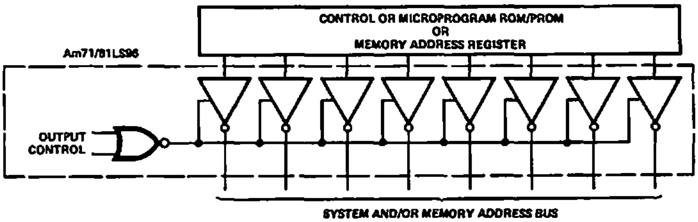


LIC-496

Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
4. Pulse generator characteristics: PRR < 1MHz, $Z_{OUT} \approx 50\Omega$, $t_r < 15$ns, $t_f < 6$ns.
5. When measuring t_{PLH} and t_{PHL}, switches S_1 and S_2 are closed.

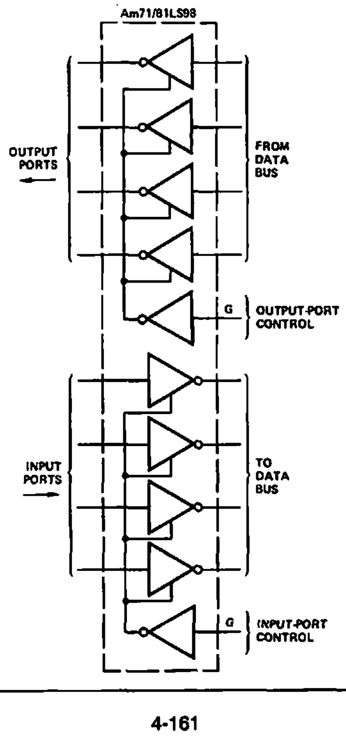
APPLICATIONS

Am71/81LS96 USED AS SYSTEM AND/OR MEMORY BUS DRIVER



LIC-497

INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



LIC-498

ORDERING INFORMATION

Package Type	Temperature Range	Order Number Am71/81LS95	Am71/81LS96	Am71/81LS97	Am71/81LS98
Molded DIP	0°C to +70°C	DM81LS95N	DM81LS96N	DM81LS97N	DM81LS98N
Hermetic DIP	0°C to +70°C	DM81LS95J	DM81LS96J	DM81LS97J	DM81LS98J
Hermetic DIP	−55°C to +125°C	DM71LS95J	DM71LS96J	DM71LS97J	DM71LS98J
Dice	0°C to +70°C	AM81LS95X	AM81LS96X	AM81LS97X	AM81LS98X

4

Am73/8303B

Octal Three-State Inverting Bidirectional Transceiver

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- Three-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- $V_{CC}-1.15V$ V_{OH} interfaces with TTL, MOS, and CMOS
- 48mA, 300pF bus drive capability
- Transmit/$\overline{\text{Receive}}$ and Chip Disable simplify control logic
- 20 pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

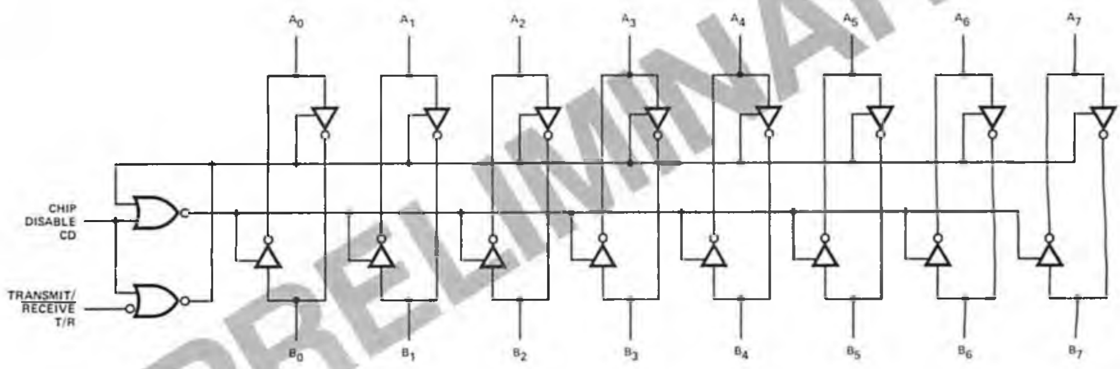
GENERAL DESCRIPTION

The Am73/8303Bs are 8-bit three-state Schottky inverting transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 16mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/$\overline{\text{Receive}}$ determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a three-state condition.

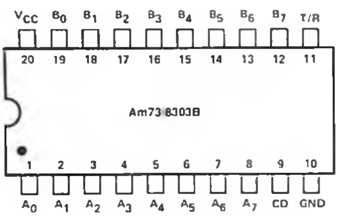
The output high voltage (V_{OH}) is specified at $V_{CC}-1.15V$ minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

LOGIC DIAGRAM



LIC-499

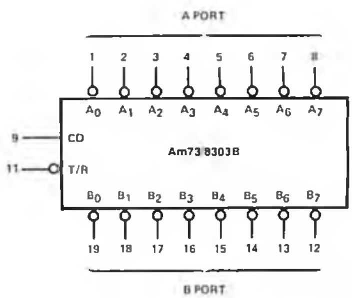
CONNECTION DIAGRAM
Top View



LIC-500

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LIC-501

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

Am7303B	T_A = −55°C to +125°C	V_{CC}MIN = 4.5V	V_{CC}MAX = 5.5V
Am8303B	T_A = 0°C to +70°C	V_{CC}MIN = 4.75V	V_{CC}MAX = 5.25V

DC ELECTRICAL CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
A PORT (A_0-A_7)							
V_{IH}	Logical "1" Input Voltage	CD = 0.8V, T/$\overline{R}$ = 2.0V		2.0			Volts
V_{IL}	Logical "0" Input Voltage	CD = 0.8V, T/$\overline{R}$ = 2.0V	Am8303B			0.8	Volts
			Am7303B			0.7	
V_{OH}	Logical "1" Output Voltage	CD = 0.8V, T/$\overline{R}$ = 0.8V	I_{OH} = −0.4mA	V_{CC}−1.15	V_{CC}−0.7		Volts
			I_{OH} = −3.0mA	2.7	3.95		
V_{OL}	Logical "0" Output Voltage	CD = 0.8V, T/$\overline{R}$ = 0.8V	I_{OL} = 8mA		0.3	0.4	Volts
			Am8303B, I_{OL} = 16mA		0.35	0.50	
I_{OS}	Output Short Circuit Current	CD = 0.8V, T/$\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = MAX., Note 2		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = 0.8V, T/$\overline{R}$ = 2.0V, V_I = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = MAX., V_I = V_{CC} MAX.				1	mA
I_{IL}	Logical "0" Input Current	CD = 0.8V, T/$\overline{R}$ = 2.0V, V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input Three-State Current	CD = 2.0V	V_O = 0.4V			−200	μA
			V_O = 4.0V			80	
B PORT (B_0-B_7)							
V_{IH}	Logical "1" Input Voltage	CD = 0.8V, T/$\overline{R}$ = 0.8V		2.0			Volts
V_{IL}	Logical "0" Input Voltage	CD = 0.8V, T/$\overline{R}$ = 0.8V	Am8303B			0.8	Volts
			Am7303B			0.7	
V_{OH}	Logical "1" Output Voltage	CD = 0.8V, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4mA	V_{CC}−1.15	V_{CC}−0.8		Volts
			I_{OH} = −5mA	2.7	3.9		
			I_{OH} = −10mA	2.4	3.6		
V_{OL}	Logical "0" Output Voltage	CD = 0.8V, T/$\overline{R}$ = 2.0V	I_{OL} = 20mA		0.3	0.4	Volts
			I_{OL} = 48mA		0.4	0.5	
I_{OS}	Output Short Circuit Current	CD = 0.8V, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = MAX., Note 2		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = 0.8V, T/$\overline{R}$ = 0.8V, V_I = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = MAX., V_I = V_{CC} MAX.				1	mA
I_{IL}	Logical "0" Input Current	CD = 0.8V, T/$\overline{R}$ = 0.8V, V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input Three-State Current	CD = 2.0V	V_O = 0.4V			−200	μA
			V_O = 4.0V			200	
CONTROL INPUTS CD, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			Volts
V_{IL}	Logical "0" Input Voltage					0.8	Volts
I_{IH}	Logical "1" Input Current	V_I = 2.7V			0.5	20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX., V_I = V_{CC} MAX.				1.0	mA
I_{IL}	Logical "0" Input Current	V_I = 0.4V	T/$\overline{R}$		−0.1	−.25	mA
			CD		−0.25	−.5	
V_C	Input Clamp Voltage	I_{IN} = −12mA			−0.8	−1.5	Volts
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	CD = 2.0V, V_{CC} = MAX., V_{IN} = 0.4V			60	130	mA
		CD = V_{INA} = 0.4V, T/$\overline{R}$ = 2V, V_{CC} = MAX.			80	160	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

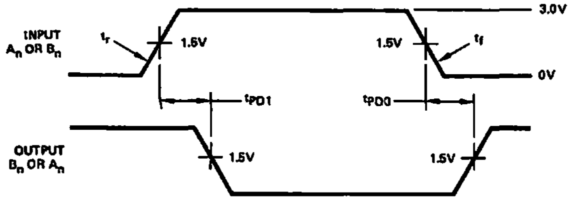
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF		8		ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF		7		ns
t_{PLZA}	Propagation Delay from a Logical "0" to Three-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF		11		ns
t_{PHZA}	Propagation Delay from a Logical "1" to Three-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF		8		ns
t_{PZLA}	Propagation Delay from Three-State to a Logical "0" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF		27		ns
t_{PZHA}	Propagation Delay from Three-State to a Logical "1" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF		19		ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF		12		ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF		7		
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF		10		ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF		7		
t_{PLZB}	Propagation Delay from a Logical "0" to Three-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF		13		ns
t_{PHZB}	Propagation Delay from a Logical "1" to Three-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF		8		ns
t_{PZLB}	Propagation Delay from Three-State to a Logical "0" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF		32		ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF		16		
t_{PZHB}	Propagation Delay from Three-State to a Logical "1" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF		26		ns
		S_3 = 0, R_5 = 667Ω, C_4 = 45pF		14		
TRANSMIT RECEIVE MODE SPECIFICATIONS						
t_{PHZR}	Propagation Delay from a Logical "1" to Three-State from T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 0, R_3 = 1k, C_2 = 15pF		7		ns
t_{PLZR}	Propagation Delay from a Logical "0" to Three-State from T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 1, R_3 = 1k, C_2 = 15pF		10		ns
t_{PHZT}	Propagation Delay from a Logical "1" to Three-State from T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 15pF S_2 = 1, R_3 = 5k, C_2 = 30pF		16		ns
t_{PLZT}	Propagation Delay from a Logical "0" to Three-State from T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 1k, C_3 = 15pF S_2 = 0, R_3 = 1k, C_2 = 30pF		17		ns
t_{PRL}	Propagation Delay from Transmit Mode to a Logical "0", T/$\overline{R}$ to A Port	$t_{PRL} = t_{PHZT} + t_{PDHLA}$		23		ns
t_{PRH}	Propagation Delay from Transmit Mode to a Logical "1", T/$\overline{R}$ to A Port	$t_{PRH} = t_{PLZT} + t_{PDLHA}$		28		ns
t_{PTL}	Propagation Delay from Receive Mode to a Logical "0", T/$\overline{R}$ to B Port	$t_{PTL} = t_{PHZR} + t_{PDHLB}$		23		ns
t_{PTH}	Propagation Delay from Receive Mode to a Logical "1", T/$\overline{R}$ to B Port	$t_{PTH} = t_{PLZR} + t_{PDLHB}$		24		ns

Notes: 1. All typical values given are for V_{CC} = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

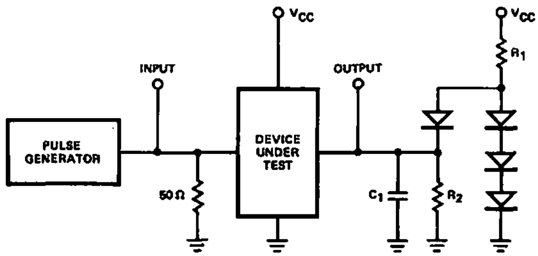
FUNCTIONAL TABLE

Inputs	Conditions		
Chip Disable	0	0	1
Transmit/$\overline{\text{Receive}}$	0	1	X
A Port	Out	In	HI-Z
B Port	In	Out	HI-Z

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS



$t_r = t_f < 10ns$
10% to 90%

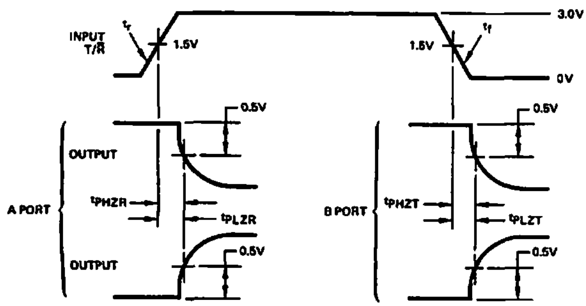


Note: C_1 includes test fixture capacitance.

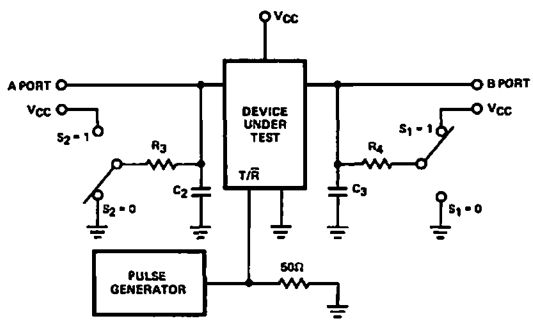
LIC-502

Figure 1. Propagation Delay from A Port to B Port or from B Port to A Port.

LIC-503



$t_r = t_f < 10ns$
10% to 90%

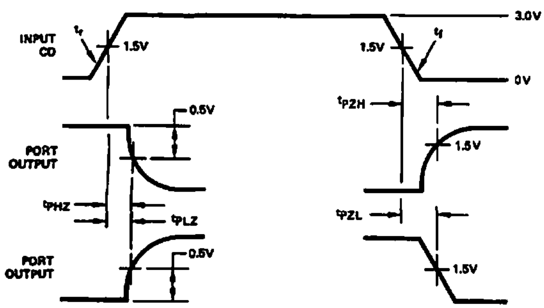


Note: C_2 and C_3 include test fixture capacitance.

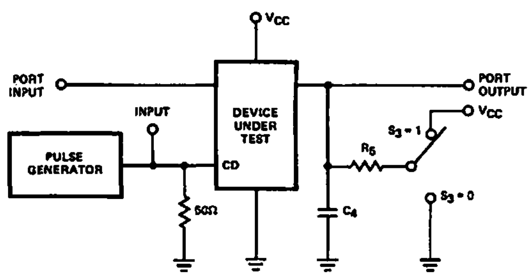
LIC-504

Figure 2. Propagation Delay from T/R̄ to A Port or B Port.

LIC-505



$t_r = t_f < 10ns$
10% to 90%



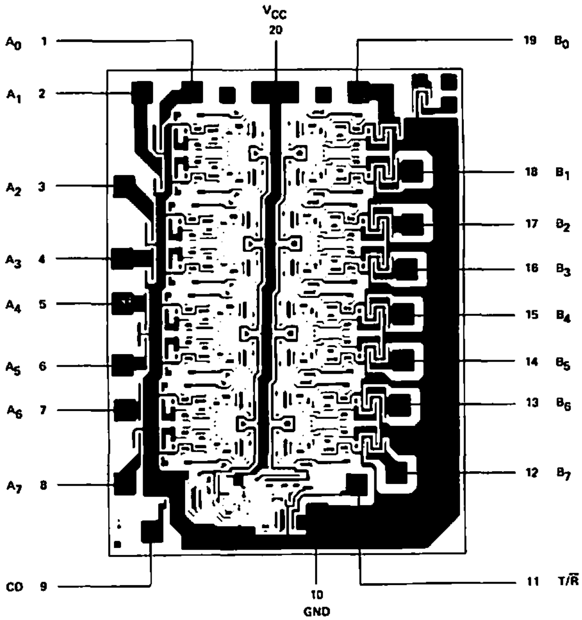
Note: C_4 includes test fixture capacitance.
Port input is in a fixed logical condition.

LIC-506

Figure 3. Propagation Delay from CD to A Port or B Port.

LIC-507

Metallization and Pad Layout



DIE SIZE 0.066" x 0.086"

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	DP7303BJ
Hermetic DIP	0°C to +70°C	DP8303BJ
Molded DIP	0°C to +70°C	DP8303BN
Dice	0°C to +70°C	AM8303BX

Am73/8304B

Octal Three-State Bidirectional Transceiver

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- Three-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- $V_{CC}-1.15V$ V_{OH} interfaces with TTL, MOS, and CMOS
- 48mA, 300pF bus drive capability
- Transmit/$\overline{\text{Receive}}$ and Chip Disable simplify control logic
- 20 pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

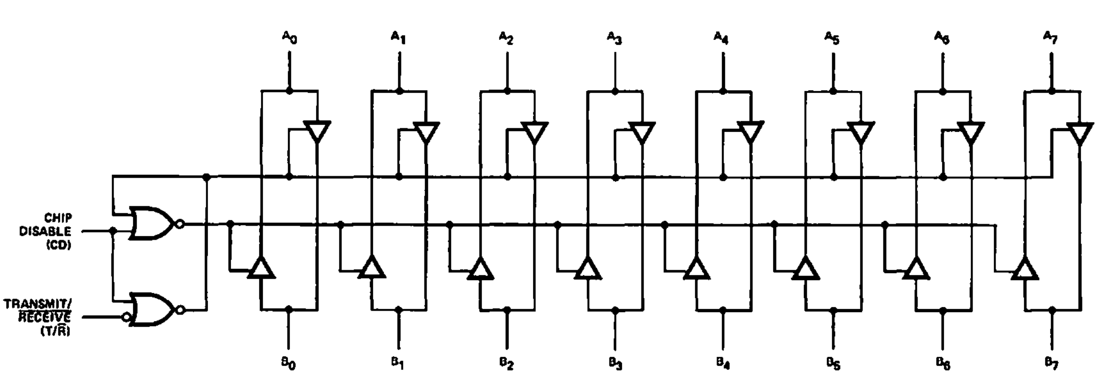
GENERAL DESCRIPTION

The Am73/8304Bs are 8-bit three-state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 16mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/$\overline{\text{Receive}}$ determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a three-state condition.

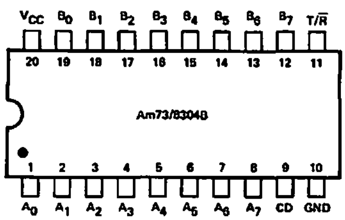
The output high voltage (V_{OH}) is specified at $V_{CC}-1.15V$ minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

LOGIC DIAGRAM



LIC-508

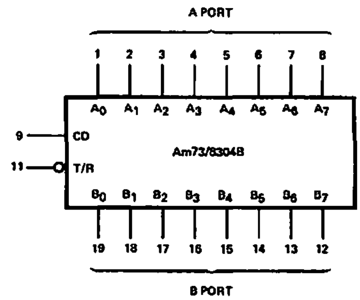
CONNECTION DIAGRAM
Top View



LIC-509

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LIC-510

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

Am7304B	T_A = −55°C to +125°C	V_{CC}MIN = 4.5V	V_{CC}MAX = 5.5V
Am8304B	T_A = 0°C to +70°C	V_{CC}MIN = 4.75V	V_{CC}MAX = 5.25V

DC ELECTRICAL CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
A PORT (A_0-A_7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL} MAX., T/$\overline{R}$ = 2.0V		2.0			Volts
V_{IL}	Logical "0" Input Voltage	CD = V_{IL} MAX., T/$\overline{R}$ = 2.0V	Am8304B			0.8	Volts
			Am7304B			0.7	
V_{OH}	Logical "1" Output Voltage	CD = V_{IL} MAX., T/$\overline{R}$ = 8.0V	I_{OH} = −0.4mA	V_{CC}−1.15	V_{CC}−0.7		Volts
			I_{OH} = −3.0mA	2.7	3.95		
V_{OL}	Logical "0" Output Voltage	CD = V_{IL} MAX., T/$\overline{R}$ = 8.0V	I_{OL} = 8mA		0.3	0.4	Volts
			Am8304B, I_{OL} = 16mA		0.35	0.50	
I_{OS}	Output Short Circuit Current	CD = V_{IL} MAX., T/$\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = MAX., Note 2		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL} MAX., T/$\overline{R}$ = 2.0V, V_I = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = MAX., V_I = V_{CC} MAX.				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL} MAX., T/$\overline{R}$ = 2.0V, V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input Three-State Current	CD = 2.0V	V_O = 0.4V			−200	μA
			V_O = 4.0V			80	
B PORT (B_0-B_7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL} MAX., T/$\overline{R}$ = V_{IL} MAX.		2.0			Volts
V_{IL}	Logical "0" Input Voltage	CD = V_{IL} MAX., T/$\overline{R}$ = V_{IL} MAX.	Am8304B			0.8	Volts
			Am7304B			0.7	
V_{OH}	Logical "1" Output Voltage	CD = V_{IL} MAX., T/$\overline{R}$ = 2.0V	I_{OH} = −0.4mA	V_{CC}−1.15	V_{CC}−0.8		Volts
			I_{OH} = −5mA	2.7	3.9		
			I_{OH} = −10mA	2.4	3.6		
V_{OL}	Logical "0" Output Voltage	CD = V_{IL} MAX., T/$\overline{R}$ = 2.0V	I_{OL} = 20mA		0.3	0.4	Volts
			I_{OL} = 48mA		0.4	0.5	
I_{OS}	Output Short Circuit Current	CD = V_{IL} MAX., T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = MAX., Note 2		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL} MAX., T/$\overline{R}$ = V_{IL} MAX., V_I = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = MAX., V_I = V_{CC} MAX.				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL} MAX., T/$\overline{R}$ = V_{IL} MAX., V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input Three-State Current	CD = 2.0V	V_O = 0.4V			−200	μA
			V_O = 4.0V			200	
CONTROL INPUTS CD, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			Volts
V_{IL}	Logical "0" Input Voltage		Am8304B			0.8	Volts
			Am7304B			0.7	
I_{IH}	Logical "1" Input Current	V_I = 2.7V			0.5	20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX., V_I = V_{CC} MAX.				1.0	mA
I_{IL}	Logical "0" Input Current	V_I = 0.4V	T/$\overline{R}$		−0.1	−.25	mA
			CD		−0.25	−.5	
V_C	Input Clamp Voltage	I_{IN} = −12mA			−0.8	−1.5	Volts
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	CD = 2.0V, V_{CC} = MAX., V_{IN} = 0.4V			60	100	mA
		CD = V_{INA} = 0.4V, T/$\overline{R}$ = 2V, V_{CC} = MAX.			80	130	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

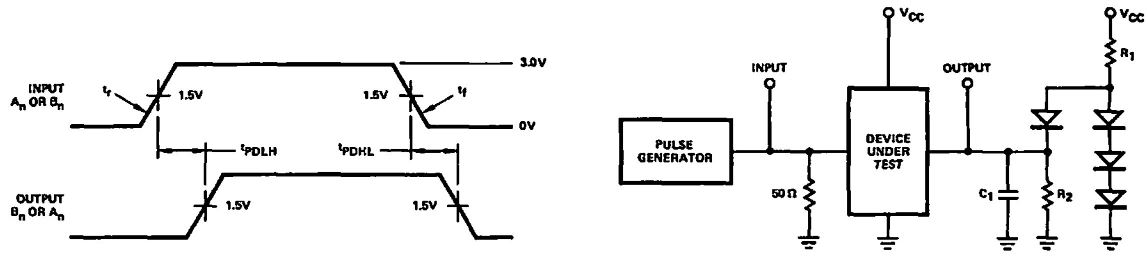
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF		14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF		13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to Three-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF		11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to Three-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF		8	15	ns
t_{PZLA}	Propagation Delay from Three-State to a Logical "0" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF		27	35	ns
t_{PZHA}	Propagation Delay from Three-State to a Logical "1" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF		19	25	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF		18	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF		11	18	
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF		16	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF		11	18	
t_{PLZB}	Propagation Delay from a Logical "0" to Three-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to Three-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF		8	15	ns
t_{PZLB}	Propagation Delay from Three-State to a Logical "0" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF		32	40	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF		16	22	
t_{PZHB}	Propagation Delay from Three-State to a Logical "1" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF		26	35	ns
		S_3 = 0, R_5 = 667Ω, C_4 = 45pF		14	22	
TRANSMIT RECEIVE MODE SPECIFICATIONS						
t_{PHZR}	Propagation Delay from a Logical "1" to Three-State from T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 0, R_3 = 1k, C_2 = 15pF		7	12	ns
t_{PLZR}	Propagation Delay from a Logical "0" to Three-State from T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 1, R_3 = 1k, C_2 = 15pF		10	14	ns
t_{PHZT}	Propagation Delay from a Logical "1" to Three-State from T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 15pF S_2 = 1, R_3 = 5k, C_2 = 30pF		16	22	ns
t_{PLZT}	Propagation Delay from a Logical "0" to Three-State from T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 1k, C_3 = 15pF S_2 = 0, R_3 = 1k, C_2 = 30pF		17	22	ns
t_{PRL}	Propagation Delay from Transmit Mode to a Logical "0", T/$\overline{R}$ to A Port	$t_{PRL} = t_{PHZT} + t_{PDHLA}$		25	40	ns
t_{PRH}	Propagation Delay from Transmit Mode to a Logical "1", T/$\overline{R}$ to A Port	$t_{PRH} = t_{PLZT} + t_{PDLHA}$		30	40	ns
t_{PTL}	Propagation Delay from Receive Mode to a Logical "0", T/$\overline{R}$ to B Port	$t_{PTL} = t_{PHZR} + t_{PDHLB}$		25	35	ns
t_{PTH}	Propagation Delay from Receive Mode to a Logical "1", T/$\overline{R}$ to B Port	$t_{PTH} = t_{PLZR} + t_{PDLHB}$		26	35	ns

Notes: 1. All typical values given are for V_{CC} = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

FUNCTIONAL TABLE

Inputs	Conditions		
Chip Disable	0	0	1
Transmit/$\overline{\text{Receive}}$	0	1	X
A Port	Out	In	HI-Z
B Port	In	Out	HI-Z

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS



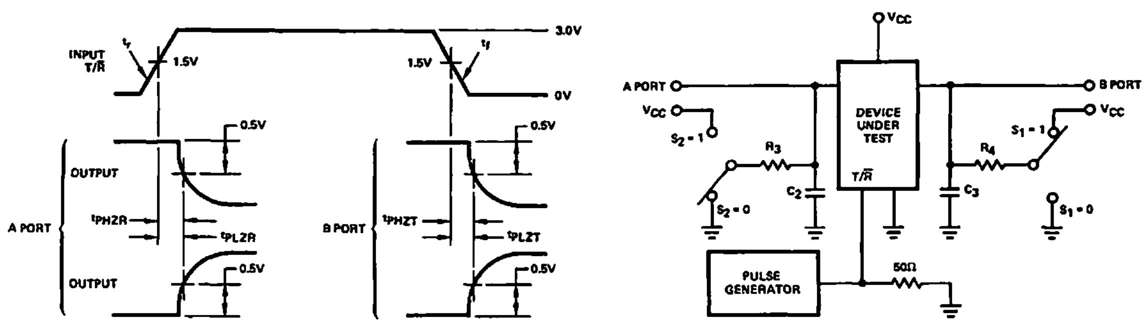
$t_r = t_f < 10ns$
10% to 90%

Note: C_1 includes test fixture capacitance.

LIC-511

Figure 1. Propagation Delay from A Port to B Port or from B Port to A Port.

LIC-512



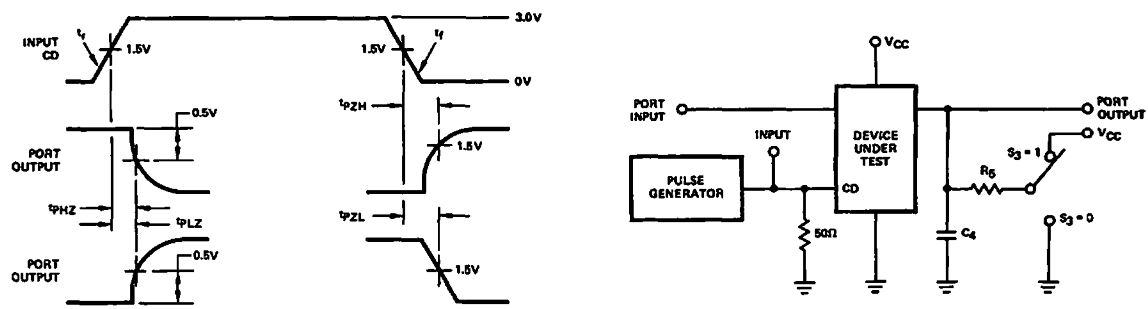
$t_r = t_f < 10ns$
10% to 90%

Note: C_2 and C_3 include test fixture capacitance.

LIC-513

Figure 2. Propagation Delay from T/$\bar{R}$ to A Port or B Port.

LIC-514



Note: C_4 includes test fixture capacitance.
Port input is in a fixed logical condition.

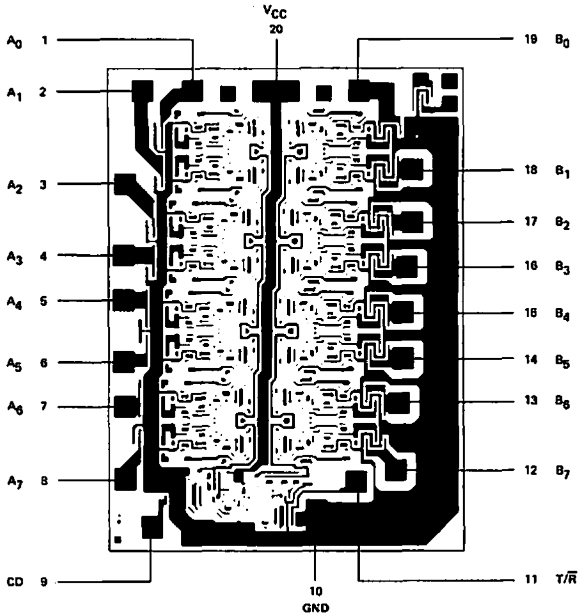
$t_r = t_f < 10ns$
10% to 90%

LIC-515

Figure 3. Propagation Delay from CD to A Port or B Port.

LIC-516

Metallization and Pad Layout



DIE SIZE 0.066" x 0.086"

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	DP7304BJ
Hermetic DIP	0°C to +70°C	DP8304BJ
Molded DIP	0°C to +70°C	DP8304BN
Dice	0°C to +70°C	AM8304BX

Am78/8820·Am78/8820A

Dual Differential Line Receivers

Distinctive Characteristics:
- Dual differential receiver pin-for-pin equivalent to the National 78/8820 and 78/8820A
- 500mV sensitivity at ±3V common mode
  1V sensitivity at ±15V common mode
- Single 5-volt supply
- Frequency response control, strobe and internal terminating resistor
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am78/8820 and Am78/8820A are dual differential line receivers designed to receive digital data from transmission lines and provide up to 15 volts of common mode rejection with a single 5-volt supply.

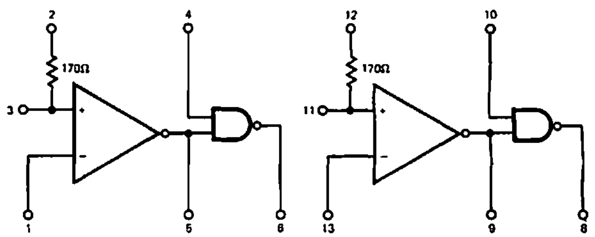
The device would normally be used in systems using twisted pair lines for connection, with each receiver having a terminating resistor included. The receivers respond to small differential signals and reject considerable amounts of common mode noise.

Each receiver has a strobe that enables the output and a response control that allows the time constant of the output circuit to be controlled by an external capacitor and give noise rejection of high frequency noise and short logic spikes.

Companion differential line drivers are the Am78/8830, Am78/8831 and Am78/8832.

LOGIC DIAGRAM

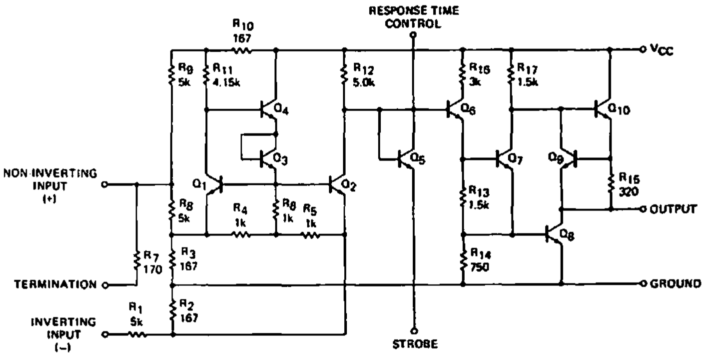
Receiver A　　Receiver B



V_{CC} = Pin 14
GND = Pin 7

LIC-517

CIRCUIT DIAGRAM



LIC-518

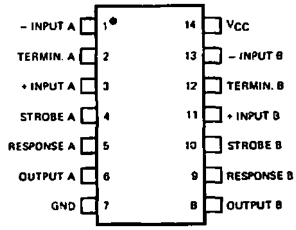
Note: Only one receiver shown.

ORDERING INFORMATION

Package Type	Temperature Range	Am78/8820 Order Number	Am78/8820A Order Number
Molded DIP	0°C to +75°C	DM8820N	DM8820AN
Hermetic DIP	0°C to +75°C	DM8820J	DM8820AJ
Dice	0°C to +75°C	AM8820X	AM8820AX
Hermetic DIP	−55°C to +125°C	DM7820J	DM7820AJ
Hermetic Flat Pak	−55°C to +125°C	DM7820W	DM7820AW
Dice	−55°C to +125°C	AM7820X	AM7820AX

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.　LIC-519

Am7820 • Am8820

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am8820A	$T_A = 0°C$ to $+75°C$	$V_{CC} = 5.0V \pm 5\%$	$V_{CM} = -15V$ to $+15V$
Am7820A	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	$V_{CM} = -15V$ to $+15V$

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} < 0.2mA$	2.5	4.0	5.5	Volts
V_{OL}	Output LOW Voltage	$I_{OL} < 3.5mA$	0		0.4	Volts
V_{TH}	Differential Threshold Voltage	$V_{CM} = 0V$		+0.06	+0.5	Volts
		$-15V < V_{CM} < +15V$		+0.06	+1.0	
		$V_{CM} = 0V$	−0.5	−0.08		
		$-15V < V_{CM} < +15V$	−1.0	−0.08		
I_{IH}	Strobe Input HIGH Current	$V_{STROBE} = 5.5V$		0.01	5.0	µA
I_{IL}	Strobe Input LOW Current	$V_{STROBE} = 0.4V$	−1.4	−1.0		mA
$I_{IN\ INV}$	Inverting Input Current	$V_{CM} = +15V$		+3.0	+4.2	mA
		$V_{CM} = 0V$	−0.5	0		
		$V_{CM} = -15V$	−4.2	−3.0		
$I_{IN\ NINV}$	Non-Inverting Input Current	$V_{CM} = +15V$		+5.0	+7.0	mA
		$V_{CM} = 0V$	−1.6	−1.0		
		$V_{CM} = -15V$	−9.8	−7.0		
I_{CC}	Power Supply Current (Each Receiver)	$V_{CM} = +15V$		+3.9	+7.0	mA
		$V_{CM} = 0V$		+6.5	+10.2	
		$V_{CM} = -15V$		+8.3	+15.0	
$R_{IN\ INV}$	Inverting Input Resistance		3.6	5.0		kΩ
$R_{IN\ NINV}$	Non-Inverting Input Resistance		1.8	2.5		kΩ
R_{TERM}	Input Terminating Resistor	$T_A = 25°C$	120	170	250	Ω

Notes: 1. For operating at elevated temperatures, the device must be derated based on a thermal resistance of 100°C/W and a maximum junction temperature of 150°C for the AM7820, or 150°C/W and 115°C maximum junction temperature for the AM8820.
2. Typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0V$ unless stated differently.

4

Switching Characteristics ($T_A = 25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{RESP}	Response Time	$C_{delay} = 0$		40		ns
t_{RESP}	Response Time	$C_{delay} = 100\ pF$		150		ns

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature		–65°C to +150°C
Temperature (Ambient) Under Bias		–55°C to +125°C
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous		–0.5V to +8.0V
DC Common Mode Voltage		–20V to +20V
DC Strobe Input Voltage		–0.5V to +8.0V
DC Data Input Voltage		–20V to +20V
Output Current, Into Outputs:	Am78/8820	25mA
	Am78/8820A	50mA
Power Dissipation (Note 1)		600mW

Am7820A • Am8820A

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am8820A $T_A = 0°C$ to $+75°C$ $V_{CC} = 5.0V \pm 5\%$ $V_{CM} = -15V$ to $+15V$
Am7820A $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ $V_{CM} = -15V$ to $+15V$

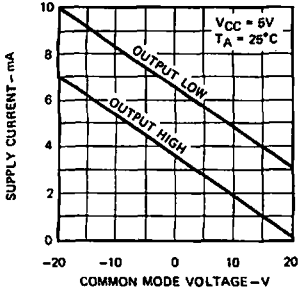
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{DIFF} = +1V$, $I_{OH} = -400\mu A$	2.5	4.0	5.5	Volts
V_{OL}	Output LOW Voltage	$V_{DIFF} = -1V$	0		0.4	Volts
V_{IH}	Strobe Input HIGH Level Voltage	$V_{DIFF} = -3V$ $V_{OUT} \leq 0.4V$, $I_{OUT} = 16mA$	2.1			Volts
V_{IL}	Strobe Input LOW Level Voltage	$V_{DIFF} = -3V$ $V_{OUT} \geq 2.5V$, $I_{OUT} = -400\mu A$			0.9	Volts
V_{TH}	Differential Threshold Voltage	$-3V \leq V_{CM} \leq +3V$, $I_{OUT} = -400\mu A$		+0.06	+0.5	Volts
		$-15V \leq V_{CM} \leq +15V$, $I_{OUT} = -400\mu A$		+0.06	+1.0	
		$-3V \leq V_{CM} \leq +3V$, $I_{OUT} = 16mA$	–0.5	–0.08		
		$-15V \leq V_{CM} \leq +15V$, $I_{OUT} = 16mA$	–1.0	–0.08		
I_{IH}	Strobe Input HIGH Current	$V_{STROBE} = 5.5V$, $V_{DIFF} = +3V$		0.01	5.0	µA
I_{IL}	Strobe Input LOW Current	$V_{STROBE} = 0.4V$, $V_{DIFF} = -3V$	–1.4	–1.0		mA
$I_{IN\ INV}$	Inverting Input Current	$V_{CM} = +15V$		+3.0	+4.2	mA
		$V_{CM} = 0V$	–0.5	0		
		$V_{CM} = -15V$	–4.2	–3.0		
$I_{IN\ NINV}$	Non-Inverting Input Current	$V_{CM} = +15V$		+5.0	+7.0	mA
		$V_{CM} = 0V$	–1.6	–1.0		
		$V_{CM} = -15V$	–9.8	–7.0		
I_{SC}	Output Short Circuit Current	$V_{OUT} = 0V$, $V_{STROBE} = 0V$, $V_{CC} = 5.5V$	–6.7	–4.5	–2.8	mA
I_{CC}	Power Supply Current (Each Receiver)	$V_{CM} = +15V$, $V_{DIFF} = -1V$		+3.9	+6.0	mA
		$V_{CM} = 0V$, $V_{DIFF} = -0.5V$		+6.5	+10.2	
		$V_{CM} = -15V$, $V_{DIFF} = -1V$		+9.2	+14.0	
$R_{IN\ INV}$	Inverting Input Resistance		3.6	5.0		kΩ
$R_{IN\ NINV}$	Non-Inverting Input Resistance		1.8	2.5		kΩ
R_{TERM}	Input Terminating Resistor	$T_A = 25°C$	120	170	250	Ω

Notes: 1. For operating at elevated temperatures, the device must be derated based on a thermal resistance of 100°C/W and a maximum junction temperature of 160°C for the AM7820A, or 150°C/W and 115°C maximum junction temperature for the AM8820A.
2. Typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0V$ unless stated differently.

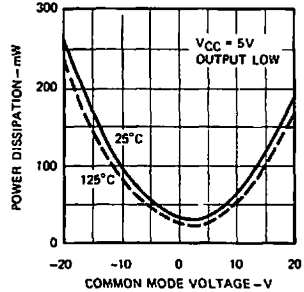
Switching Characteristics ($T_A = 25°C$)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL}	Differential Input to Output LOW	$V_{CC} = 5.0V$ See Switching Waveforms		25	45	ns
t_{PLH}	Differential Input to Output HIGH			22	40	ns
t_{PHL}	Strobe Input to Output LOW			16	25	ns
t_{PLH}	Strobe Input to Output HIGH			15	30	ns

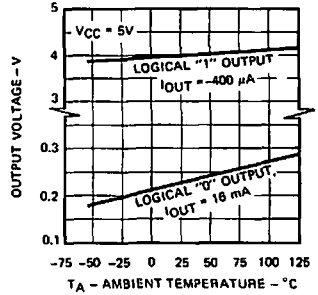
Power Supply Current (Each Receiver)



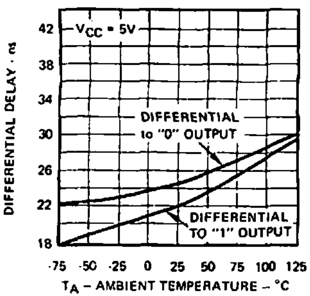
Internal Power Dissipation (Each Receiver)



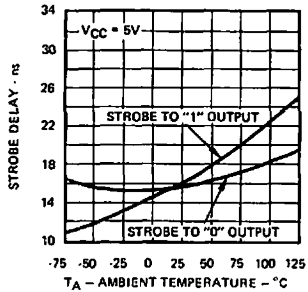
Output Voltage Levels



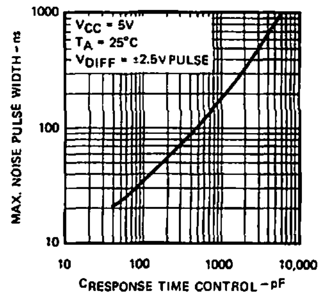
Differential Input Delays



Strobe Delays



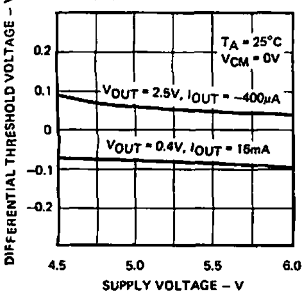
Noise Rejection



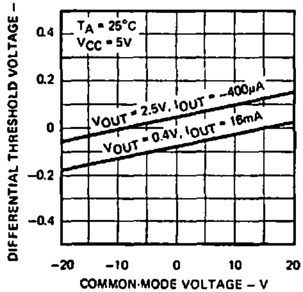
LIC-520

TYPICAL PERFORMANCE CHARACTERISTICS

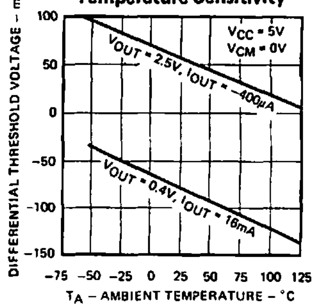
Supply Voltage Sensitivity



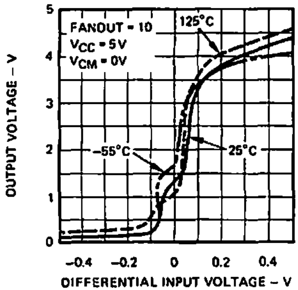
Common-Mode Voltage Sensitivity



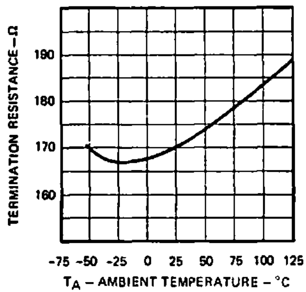
Temperature Sensitivity



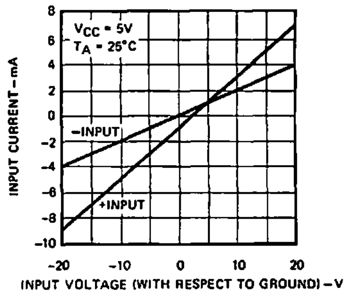
Transfer Function



Termination Resistance

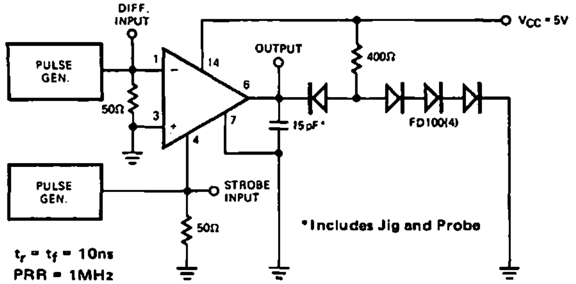


Input Characteristics

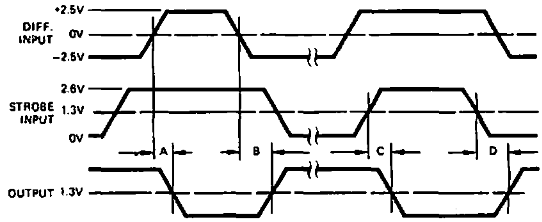


4

AC TEST CIRCUIT AND WAVEFORMS



LIC-521

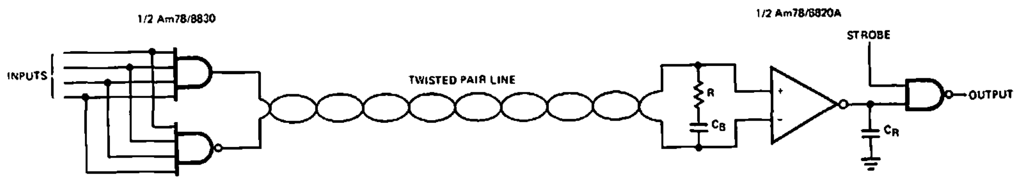


A = Differential Input to "0" Output
B = Differential Input to "1" Output
C = Strobe Input to "0" Output
D = Strobe Input to "1" Output

LIC-522

TYPICAL APPLICATION

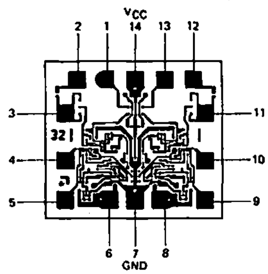
TYPICAL TWISTED PAIR DIFFERENTIAL COMMUNICATION SYSTEM



LIC-523

The Am78/8830 drives a twisted pair line which is terminated at the receiving end by an RC network. The R is approximately equal to the line impedance (170Ω) and is part of the Am78/8820A differential receiver. The C_B is a blocking capacitor which stops DC current flow, and for low duty cycles reduces power consumption. The value of this capacitor depends upon the data rate, C_B must be large compared to $\frac{1}{fd \cdot R}$ where fd is the data rate. The capacitor C_R is used to control the response time of the receiver and limit high frequency noise. $C_R \sim 4 \times 10^3 \frac{1}{fn}$ where C is in pF and fn is the lowest noise frequency expected in MHz.

Metallization and Pad Layout



DIE SIZE 0.045" X 0.050"

Am78/8830

Dual Differential Line Driver

Distinctive Characteristics

- *Single 5-volt power supply*
- Input diodes for prevention of line ringing
- Low output skew between NAND and AND propagation delays.
- Clamped outputs for reduction in positive and negative voltage transients.
- 100% reliability assurance testing in compliance with MIL-STD-883.

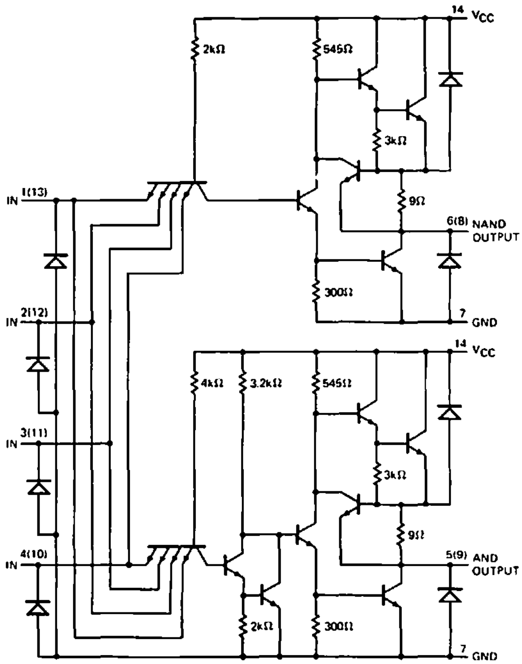
FUNCTIONAL DESCRIPTION

The Am78/8830 is a dual differential line driver suitable for driving differential lines with characteristic impedances in the range 50Ω to 500Ω.

Each driver consists of a 4-input AND gate in parallel with a 4-input NAND gate. The inputs to the gates are clamped to reduce the effect of line transients. The differential outputs are balanced and have approximately the same delay so as to minimize skew problems, and have high drive capability at both the LOW and HIGH logic levels.

The device is ideal for driving differential transmission lines, and forms a very noise insensitive balanced digital communication system with excellent common mode noise rejection when used in conjunction with the Am78/8820A dual differential receiver.

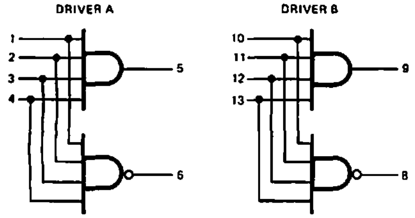
CIRCUIT DIAGRAM



Note: Only one driver shown

LIC-525

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

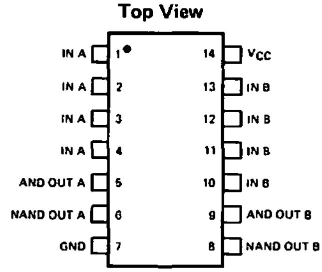
LIC-524

Am78/8830 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	DM8830N
Ceramic DIP	0°C to +75°C	DM8830J
Hermetic DIP	–55°C to +125°C	DM7830J
Hermetic Flat Pak	–55°C to +125°C	DM7830W
Dice	0°C to +75°C	AM8830X
Dice	–55°C to +125°C	AM7830X

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation

LIC-526

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to $+V_{CC}$ max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	100mA
DC Input Current	−30mA to +5.0mA
Output Short Circuit Duration at 125°C	1sec

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am8830 T_A = 0°C to +75°C V_{CC} = 5.0V ±5%
Am7830 T_A = −55°C to +125°C V_{CC} = 5.0V ±10%

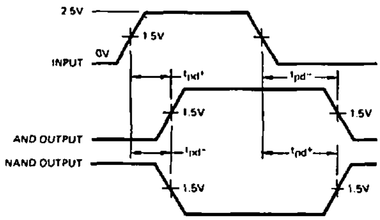
Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = 0.8V	I_{OH} = −40mA	1.8	2.9		Volts
			I_{OH} = −0.8mA	2.4	3.3		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = 0.8V	I_{OL} = 40mA		0.22	0.5	Volts
			I_{OL} = 32mA		0.2	0.4	
V_{IH}	Input HIGH Level Voltage	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level Voltage	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V			−3.0	−4.8	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				120	µA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				2.0	mA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = 5.0V, V_{OUT} = 0.0V		−40	−100	−120	mA
I_{CC}	Power Supply Current*	V_{CC} = MAX. (Each Driver)			11	18	mA

Note 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
Note 2. Limits for T_A = +125°C only.

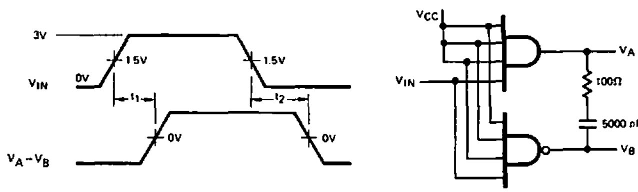
Switching Characteristics (T_A = 25°C)

Parameters	Description	Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Delay from Inputs to Output of AND Gate	V_{CC} = 5.0V, C_L = 15pF See Figure 1		8	12	ns
t_{PHL}				11	18	ns
t_{PLH}	Delay from Inputs to Output of NAND gate			8	12	ns
t_{PHL}				5	8	ns
t_1	Differential Delay	V_{CC} = 5.0V, C_L = 5000pF R_L = 100Ω, See Figure 2		12	16	ns
t_2				12	16	ns

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUIT



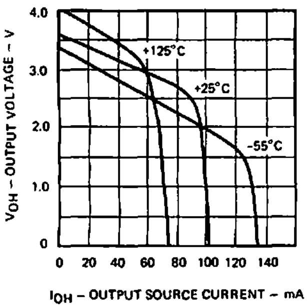
LIC-527 **Figure 1.**



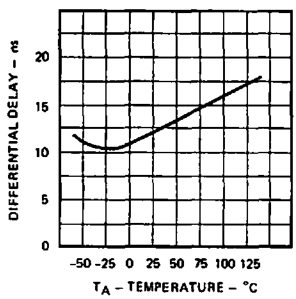
LIC-528 **Figure 2.** LIC-529

TYPICAL ELECTRICAL CHARACTERISTICS

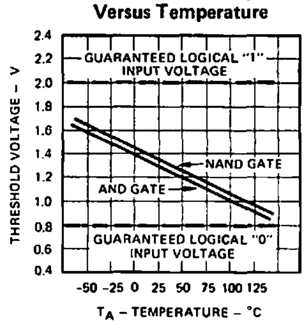
Output High Voltage Versus Output Current



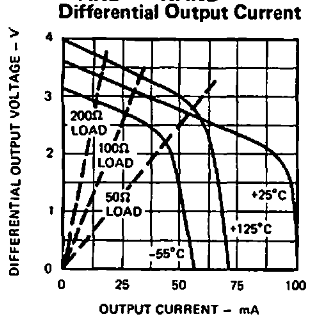
Differential Delay Versus Temperature



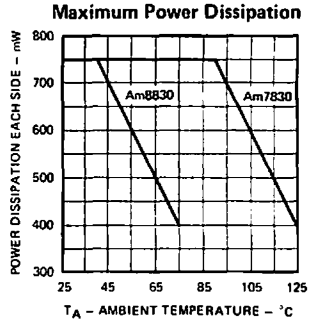
Threshold Voltage Versus Temperature



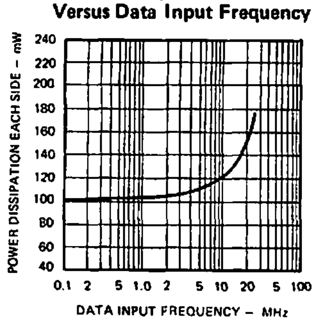
Differential Output Voltage $V_{AND} - V_{NAND}$ Versus Differential Output Current



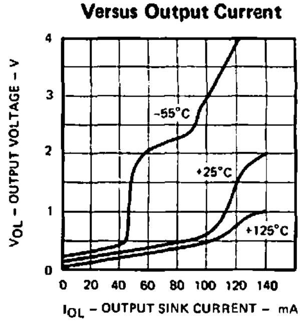
Maximum Power Dissipation



Power Dissipation (No Load) Versus Data Input Frequency

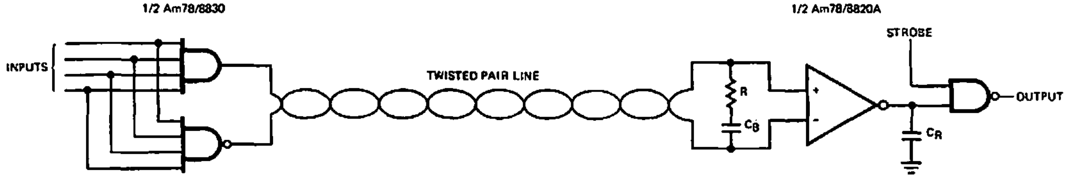


Output Low Voltage Versus Output Current



LIC-530

APPLICATIONS

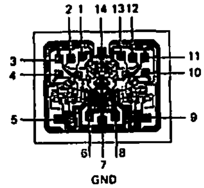


LIC-531

TYPICAL TWISTED PAIR DIFFERENTIAL COMMUNICATION SYSTEM

The Am78/8830 drives a twisted pair line which is terminated at the receiving end by an RC network. The R is approximately equal to the line impedance (170Ω) and is part of the Am78/8820A differential receiver. The C_B is a blocking capacitor which stops DC current flow, and for low duty cycles reduces power consumption. The value of this capacitor depends upon the data rate, C_B must be large compared to $\frac{1}{fd \cdot R}$ where fd is the data rate. The capacitor C_R is used to control the response time of the receiver and limit high frequency noise. $C_R \sim 4 \times 10^3 \frac{1}{fn}$ where C is in pF and fn is the lowest noise frequency expected in MHz.

Metallization and Pad Layout



DIE SIZE 0.050" x 0.063"

Am78/8831·Am78/8832

Three-State Line Driver

Distinctive Characteristics

- Three-State Line Drivers pin-for-pin equivalent to the *DM78/8831* and DM78/8832
- Mode control for quad single-ended or dual differential operation
- *Common* bus operation
- High-drive capability
- 40mA sink and source current
- Series 54/74 compatible
- 13ns typical propagation delay
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

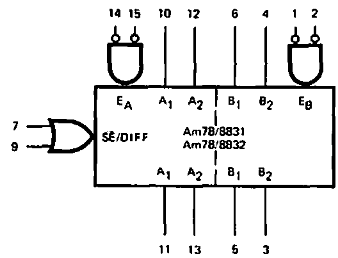
The Am78/8831 and Am78/8832 line drivers can be used either as a quad single-ended driver or as a dual differential driver. Each driver has a three-state output making the device particularly suitable for party-line operation where several drivers are directly connected to the same bus. The Am78/8832 does not have the V_{CC} clamp diodes found on the Am74/8831.

When used for single-ended operation the two differential/single-ended control inputs are held LOW. The device then operates as four independent non-inverting drivers. For differential working at least one differential/single-ended control input is held HIGH. The A-channel inputs are connected together and the B-channel inputs are connected together. Signal inputs will then pass non-inverted to the A_2 and B_2 outputs and inverted on the A_1 and B_1 outputs.

For party-line operation outputs of different channels are tied together, and outputs of all channels except one are forced into the third high impedance state by having at least one of the channel disable inputs HIGH. The channel that is enabled has both channel disable inputs LOW, and the low-output impedance of this output at both logic levels controls the level of the bus, provides good capacitance drive and insures good waveform integrity.

The channel which is enabled can conveniently be selected by a decoding matrix using Am9301 1-of-10 or Am9311 1-of-16 active LOW output decoders. The high drive capability at both logic levels enables drivers to drive a low impedance line and still supply the inverse leakage current of several disabled drivers.

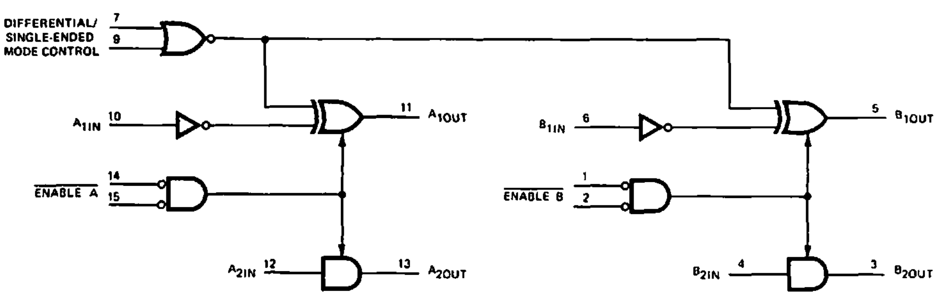
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LIC-532

LOGIC DIAGRAM

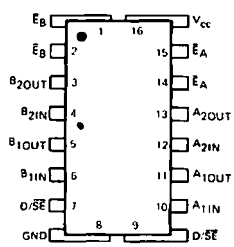


LIC-533

ORDERING INFORMATION

Package Type	Temperature Range	Am78/8831 Order Number	Am78/8832 Order Number
Molded DIP	0°C to +75°C	DM8831N	DM8832N
Hermetic DIP	0°C to +75°C	DM8831J	DM8832J
Dice	0°C to +75°C	AM8831X	AM8832X
Hermetic DIP	−55°C to +125°C	DM7831J	DM7832J
Hermetic Flat Pak	−55°C to +125°C	DM7831W	DM7832W
Dice	−55°C to +125°C	AM7831X	AM8832X

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-534

4

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	–0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	–0.5 V to $+V_{CC}$ max
DC Input Voltage	–0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	–30 mA to +5.0 mA
Time that 2 Bus-Connected Devices May Be in Opposite Low Impedance States Simultaneously	∞

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am8831, Am8832	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am7831, Am7832	T_A = –55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –40 mA	1.8	2.8		Volts
			Am7831, 32 I_{OH} = –2 mA Am8831, 32 I_{OH} = –5.2 mA	2.4	3.1		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 40 mA		0.29	0.5	Volts
			I_{OL} = 32 mA		0.2	0.4	
V_{IH}	Input HIGH Level Voltage	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level Voltage	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_L	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			–1.0	–1.6	mA
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			6.0	40	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{LK}	Output Leakage Current	V_{CC} = MAX., $\overline{E}$ = 2.4 V, V_{OUT} = 2.4 V			5	40	μA
		V_{CC} = MAX., $\overline{E}$ = 2.4 V, V_{OUT} = 0.4 V			–5	–40	
V_I	Input Clamp Diode Voltage	V_{CC} = 5.0 V, I_I = –12 mA, T_A = 25°C				–1.5	Volts
V_O	Output Clamp Diode Voltage	V_{CC} = 5.0 V, I_I = 12 mA, T_A = 25°C Am78/8831 Only				V_{CC} + 1.5V	Volts
V_O	Output Substrate Diode Voltage	V_{CC} = 5.0 V, I_I = –12 mA, T_A = 25°C				–1.5	Volts
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V, T_A = MAX.		–40		–120	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			57	90	mA

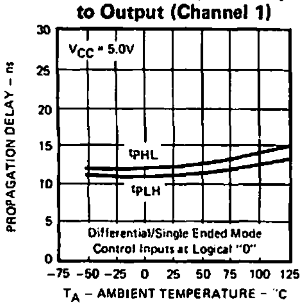
Notes: 1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. Only one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°)

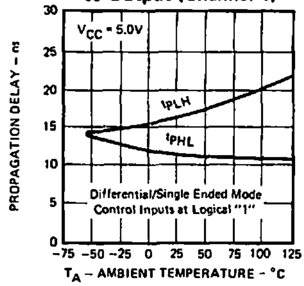
Parameters	Description	Min.	Typ.	Max.	Units
t_{PLH}	Delay from Inputs A_1, A_2, B_1, B_2 and Single-Ended/ Diff. Control to Output		13	25	ns
t_{PHL}			13	25	ns
t_{HZ}	Delay from Output Enable to Output		6	12	ns
t_{LZ}			14	22	ns
t_{ZH}	Delay from Output Enable to Output		14	22	ns
t_{ZL}			18	27	ns

TYPICAL PERFORMANCE CHARACTERISTICS

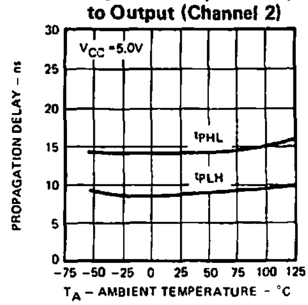
Propagation Delay from Input to Output (Channel 1)



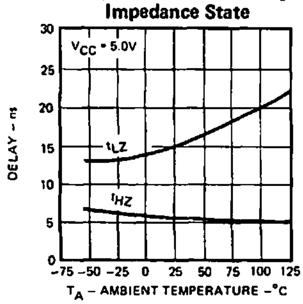
Propagation Delay from Input to Output (Channel 1)



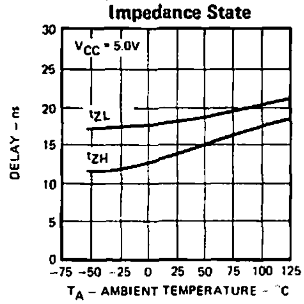
Propagation Delay from Input to Output (Channel 2)



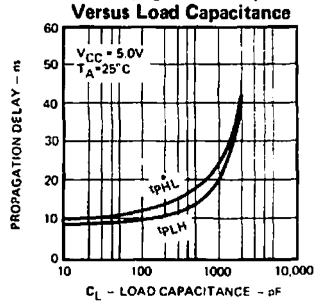
Delay from Disable to High Impedance State



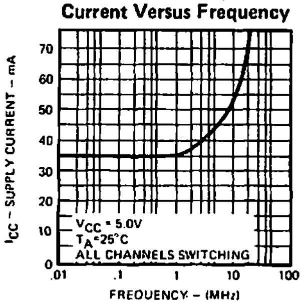
Delay from Disable to Low Impedance State



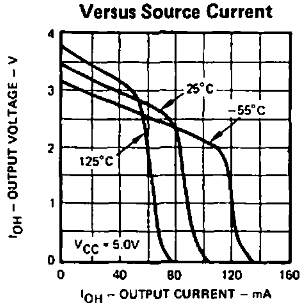
Propagation Delay Versus Load Capacitance



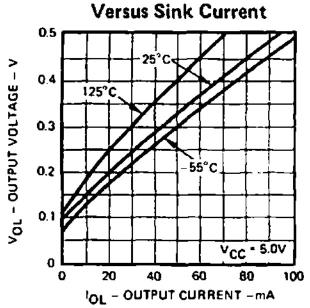
Total Supply Current Versus Frequency



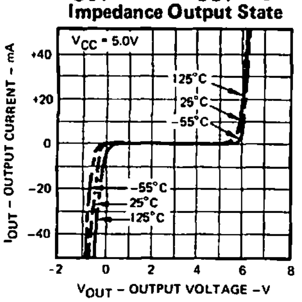
Logical "1" Output Voltage Versus Source Current



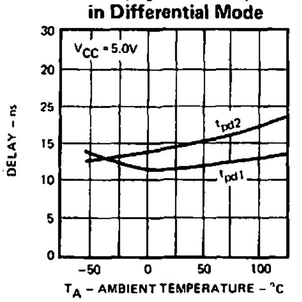
Logical "0" Output Voltage Versus Sink Current

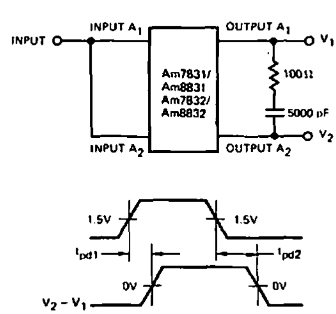


I_{OUT} Versus V_{OUT} High Impedance Output State



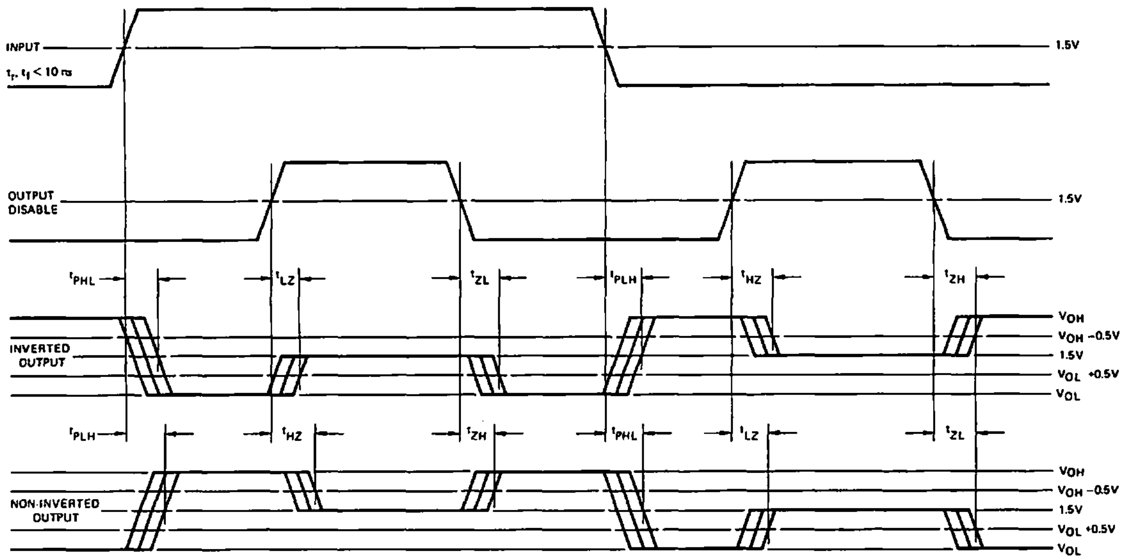
Propagation Delay in Differential Mode





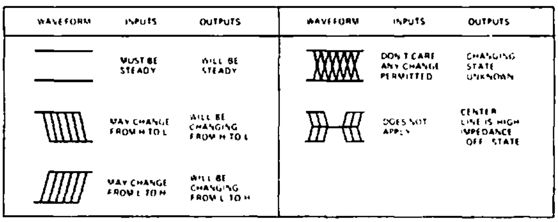
LIC-535

SWITCHING TIME WAVEFORMS AND TEST CIRCUIT



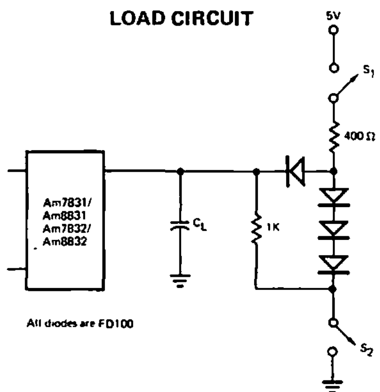
NOTE: V_{OL} and V_{OH} refer to actual voltages on output LOW and HIGH states.

KEY TO TIMING DIAGRAM



LIC-536

LOAD CIRCUIT



All diodes are FD100

	Switch S_1	Switch S_2	C_L
t_{PLH}	closed	closed	50 pF
t_{PHL}	closed	closed	50 pF
t_{HZ}	closed	closed	* 5 pF
t_{LZ}	closed	closed	* 5 pF
t_{ZL}	closed	open	50 pF
t_{ZH}	open	closed	50 pF

* Jig Capacitance

LIC-537

TRUTH TABLE
(Shown for A Channels Only)

SINGLE-ENDED/ DIFF CONTROL		A ENABLE		IN A_1	OUT A_1	IN A_2	OUT A_2
L	L	L	L	A_1	A_1	A_2	A_2
H	X	L	L	A_1	$\overline{A}_1$	A_2	A_2
X	H	L	L	A_1	$\overline{A}_1$	A_2	A_2
X	X	H	X	X	F	X	F
X	X	X	H	X	F	X	F

H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
F = Floating Output

TABLE I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400	1	1
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

TABLE III

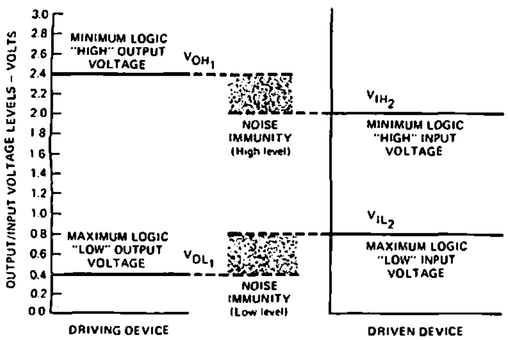
LOADING RULES (In Unit Loads)

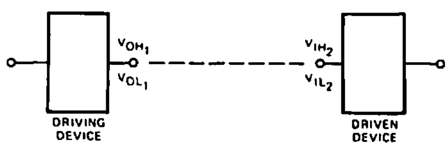
Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{\text{Enable B}}$	1	1	–	–
Enable B	2	1	–	–
B_2 Out	3	–	1000	25
B_2 In	4	1	–	–
B_1 Out	5	–	1000	25
B_1 In	6	1	–	–
$\overline{\text{SE}}$/Diff	7	1	–	–
GND	8	–	–	–
$\overline{\text{SE}}$/Diff	9	1	–	–
A_1 In	10	1	–	–
A_1 Out	11	–	1000	25
A_2 In	12	1	–	–
A_2 Out	13	–	1000	25
$\overline{\text{Enable A}}$	14	1	–	–
Enable A	15	1	–	–
V_{CC}	16	–	–	–

TABLE II

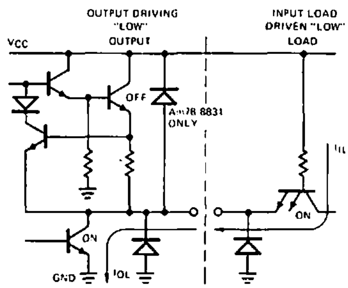
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions – LOW & HIGH

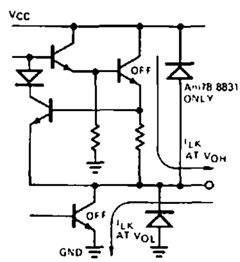




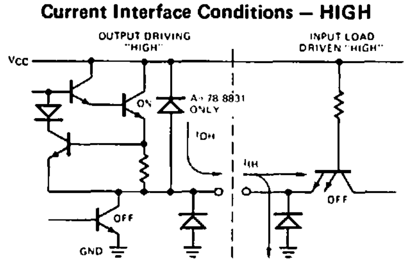
Current Interface Conditions – LOW



Current Interface Conditions – FLOATING

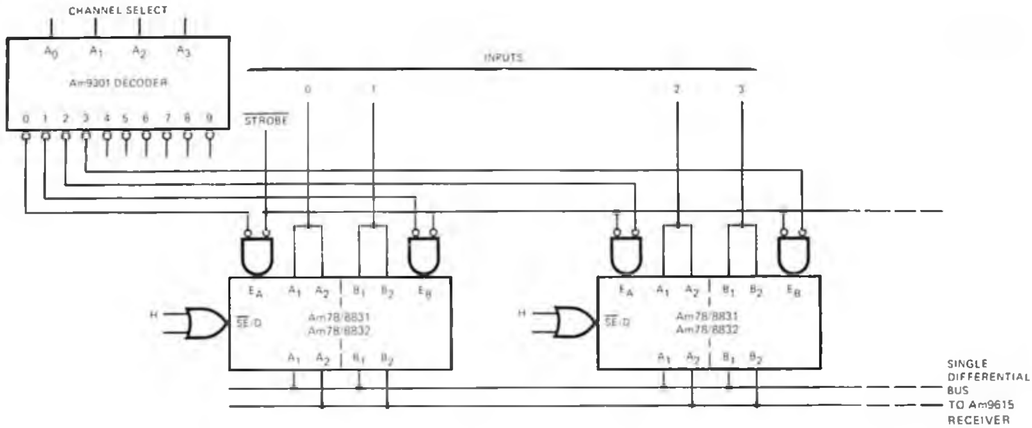


Current Interface Conditions – HIGH



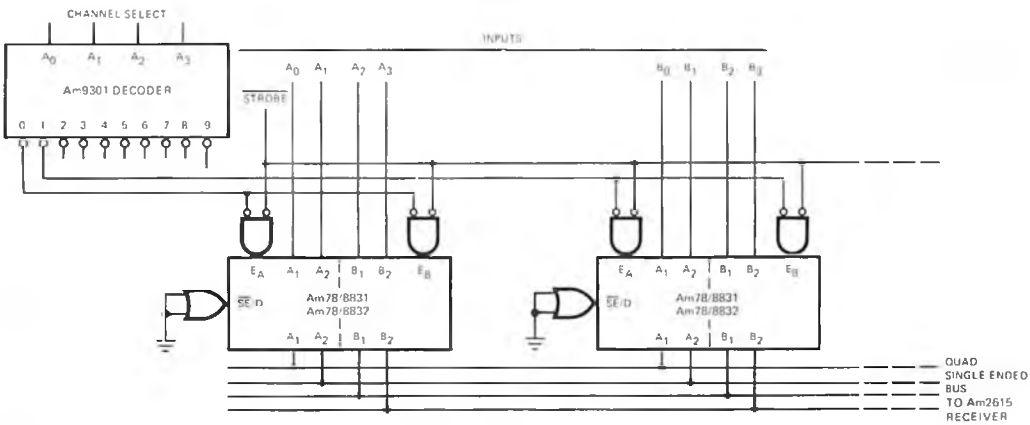
LIC-538

APPLICATIONS



LIC-539

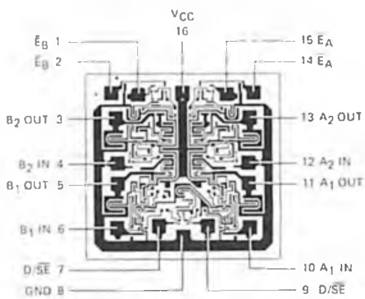
PARTY LINE DIFFERENTIAL OPERATION



LIC-540

PARTY LINE SINGLE-ENDED OPERATION

Metallization and Pad Layout



DIE SIZE 0.057" X 0.058"

Am7838 • Am8838

Quad Unified Bus Transceiver

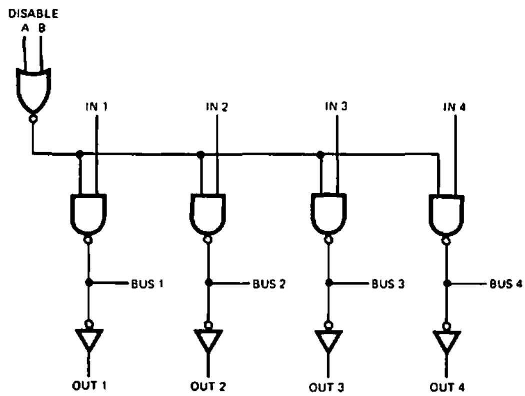
DISTINCTIVE CHARACTERISTICS

- 4 totally separate driver/receiver pairs per package.
- 1V typical receiver input hysteresis
- Receiver hysteresis independent of receiver output load
- Guaranteed minimum bus noise immunity of 1.3V, 2V typ.
- Temperature insensitive receiver thresholds track bus logic levels
- 20μA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High-Speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs
- Advanced Schottky processing

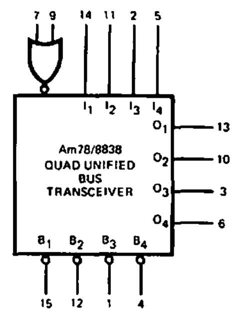
FUNCTIONAL DESCRIPTION

The Am7838 • Am8838 are quad high-speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be a 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate hysteresis to greatly enhance bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously. Receiver performance is optimized for systems with bus rise and fall times ⩽ 1.0μs/V.

LOGIC DIAGRAM AND LOGIC SYMBOL



LIC-541



V_{CC} = PIN 16
GND = PIN 8

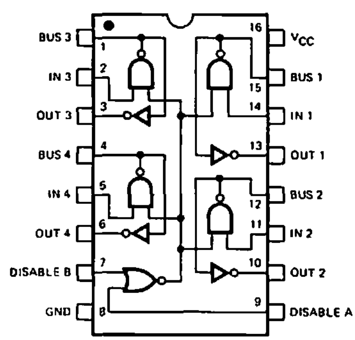
LIC-542

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	DS7838J
Hermetic DIP	0°C to +70°C	DS8838J
Molded DIP	0°C to +70°C	DS8838N

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

LIC-543

MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage	7.0V
Input and Output Voltage	5.5V
Power Dissipation	600mW
Operating Temperature Range	
Am7838	−55°C to +125°C
Am8838	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise specified:

Am7838 (MIL)	T_A = −55°C to +125°C	V_{CC}MIN = 4.50V	V_{CC}MAX = 5.50V
Am8838 (COM'L)	T_A = 0°C to +70°C	V_{CC}MIN = 4.75V	V_{CC}MAX = 5.25V

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
Driver and Disable Inputs							
V_{IH}	Logical "1" Input Voltage			2.0			Volts
V_{IL}	Logical "0" Input Voltage					0.8	Volts
I_I	Logical "1" Input Current	V_{IN} = 5.5V				1.0	mA
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V				40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V				−1.6	mA
V_{CL}	Input Diode Clamp Voltage	I_{DIS} = −12mA, I_{IN} = −12mA, I_{BUS} = −12mA, T_A = 25°C			−1.0	−1.5	Volts
Driver Output/Receiver Input							
V_{OLB}	Low Level Bus Voltage	V_{DIS} = 0.8V, V_{IN} = 2.0V, I_{BUS} = 50mA			0.4	0.7	Volts
I_{IHB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4.0V, V_{CC} = V_{MAX}.			20	100	μA
I_{ILB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4.0V, V_{CC} = 0V			2.0	100	μA
V_{IH}	High Level Receiver Threshold	V_{IND} = 0.8V, V_{OL} = 16mA	Am7838	1.65	2.25	2.65	Volts
			Am8838	1.80	2.25	2.50	
V_{IL}	Low Level Receiver Threshold	V_{IND} = 0.8V, V_{OH} = −400μA	Am7838	0.97	1.30	1.63	Volts
			Am8838	1.05	1.30	1.55	
Receiver Output							
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 0.5V, I_{OH} = −400μA		2.4			Volts
V_{OL}	Logical "0" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 4.0V, I_{OL} = 16mA			0.25	0.4	Volts
I_{OS}	Output Short Circuit Current	V_{DIS} = 0.8V, V_{IN} = 0.8V, V_{BUS} = 0.5V, V_{OS} = 0V, V_{CC} = V_{MAX}. (Note 3)		−18		−55	mA
I_{CC}	Supply Current	V_{DIS} = 0V, V_{IN} = 2.0V, (Per Package)			50	70	mA

AC CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C unless otherwise specified)

				Min.	Typ.	Max.	Units
t_{pd}	Propagation Delays	Disable to Bus "1"	(Note 4)		19	30	ns
		Disable to Bus "0"	(Note 4)		15	23	ns
		Driver Input to Bus "1"	(Note 4)		17	25	ns
		Driver Input to Bus "0"	(Note 4)		9.0	15	ns
		Bus to Logical "1" Receiver Output	(Note 5)		20	30	ns
		Bus to Logical "0" Receiver Output	(Note 6)		18	30	ns

Notes:
1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max. or min. on absolute value basis.
3. Only one output at a time should be shorted.
4. 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground, C_{LOAD} = 15pF total. Measured from V_{IN} = 1.5V to V_{BUS} = 1.5V, V_{IN} = 0V to 3.0V pulse.
5. Fan-out of 10 load, C_{LOAD} = 15pF total. Measured from V_{IN} = 1.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3.0V pulse.
6. Fan-out of 10 load, C_{LOAD} = 15pF total. Measured from V_{IN} = 2.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3.0V pulse.

Am8T26

Schottky Three-State Quad Bus Driver/Receiver

Distinctive Characteristics

- Advanced Schottky technology
- 40mA driver sink current
- Three-state outputs on driver and receiver
- PNP inputs
- 20ns max. driver propagation delay
- 18ns max. receiver propagation delay
- 100% reliability assurance testing in compliance with MIL-STD-883

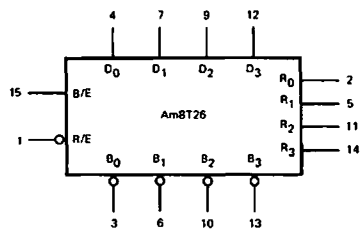
FUNCTIONAL DESCRIPTION

The Am8T26 is a high speed bus transceiver consisting of four bus drivers with three-state outputs and four bus receivers, also with three-state outputs. Each driver output is internally connected to a receiver input. Both the drivers and receivers have PNP inputs.

One buffered common "bus enable" input is connected to the four drivers and another buffered common "receiver enable" input is connected to the receivers. A LOW on the bus enable (B/E) input forces the four driver outputs to the high-impedance state. A HIGH on the bus enable allows input data to be transferred onto the data bus.

A HIGH on the receiver enable (R/E) input forces the four receiver outputs to the high-impedance state while a LOW on the receiver enable input allows the received data to be transferred to the output. The complementary design of the bus enable and receiver enable inputs allows these control inputs to be connected together externally such that a single transmit/receive function is derived.

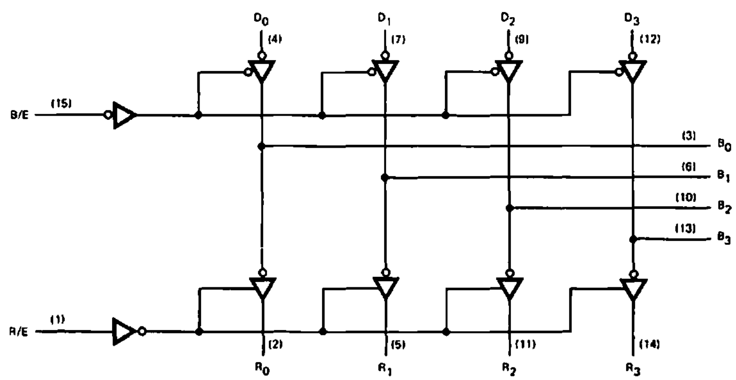
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LIC-544

LOGIC DIAGRAM



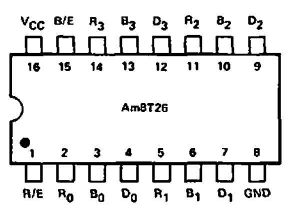
LIC-545

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	N8T26B
Hermetic DIP	0°C to +75°C	N8T26F
Dice	0°C to +75°C	AM8T26XC
Hermetic DIP	−55°C to +125°C	S8T26F
Dice	−55°C to +125°C	AM8T26XM

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

LIC-546

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to $+V_{CC}$ max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

N8T26 T_A = 0°C to +75°C V_{CC} = 5.0V ±5%
S8T26 T_A = −55°C to +125°C V_{CC} = 5.0V ±10%

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Driver Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −10mA V_{IN} = V_{IH} or V_{IL}		2.6	3.1		Volts
V_{OL}	Driver Output LOW Voltage	V_{CC} = MIN., I_{OL} = 40mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −2mA, COM'L	2.6	3.1		Volts
			I_{OH} = −1mA, MIL	2.4			
V_{OL}	Receiver Output LOW Voltage	V_{CC} = MIN., I_{OL} = −16mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	COM'L			0.85	Volts
			MIL			0.80	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −5mA				−1.0	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−0.2	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.25V				25	μA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V	Driver	−50		−150	mA
			Receiver	−30		−75	
I_{CC}	Power Supply Current	V_{CC} = MAX.				87	mA
I_O	Bus Leakage Current with Driver Off	V_{CC} = MAX., V_{BUS} = 2.6V V_{IN} = V_{IH} or V_{IL}				100	μA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Driver Input to Bus	Figure 1		16	20	ns
t_{PHL}				16	20	
t_{PLH}	Bus to Receiver Output	Figure 2		13	18	ns
t_{PHL}				6	10	
t_{ZL}	Driver Enable to Bus	Figure 3		29	38	ns
t_{LZ}				35	43	
t_{ZL}	Receiver Enable to Receiver Output	Figure 4		20	30	ns
t_{LZ}				10	17	

DEFINITION OF FUNCTIONAL TERMS

D_0, D_1, D_2, D_3 The four driver inputs.

B_0, B_1, B_2, B_3 The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the driver inputs is non-inverted.

B/E Bus enable input. When the bus enable input is LOW, the four driver outputs are in the high-impedance state.

R/E Receiver enable input. When the receiver enable input is HIGH, the four receiver outputs are in the high-impedance state.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	LOW Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
R/E	1	1/8	–	–
R_0	2	–	50	10
B_0	3	1/16	250	25
D_0	4	1/8	–	–
R_1	5	–	50	10
B_1	6	1/16	250	25
D_1	7	1/8	–	–
GND	8	–	–	–
D_2	9	1/8	–	–
B_2	10	1/16	250	25
R_2	11	–	50	10
D_3	12	1/8	–	–
B_3	13	1/16	250	25
R_3	14	–	50	10
B/E	15	1/8	–	–
V_{CC}	16	–	–	–

A TTL Unit Load is defined as –1.6mA measured at 0.4V LOW and 40μA measured at 2.4V HIGH.

4

DRIVER FUNCTION TABLE

INPUTS		OUTPUT
B/E	D_i	B_i
L	X	Z
H	L	H
H	H	L

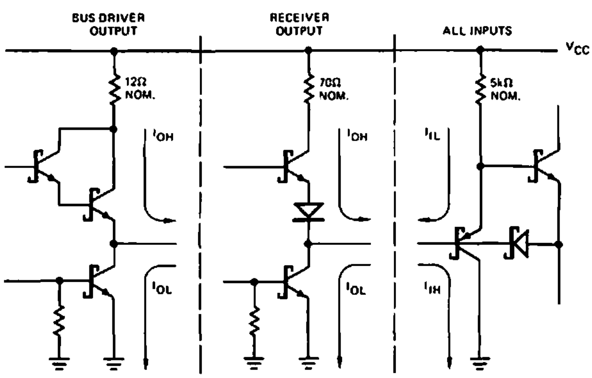
L = LOW　X = Don't Care
H = HIGH　Z = High Impedance
i = 0, 1, 2, or 3

RECEIVER FUNCTION TABLE

INPUTS		OUTPUT
R/E	B_i	R_i
H	X	Z
L	L	H
L	H	L

L = LOW　X = Don't Care
H = HIGH　Z = High Impedance
i = 0, 1, 2, or 3

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

LIC-547

AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY (Data In to Bus)

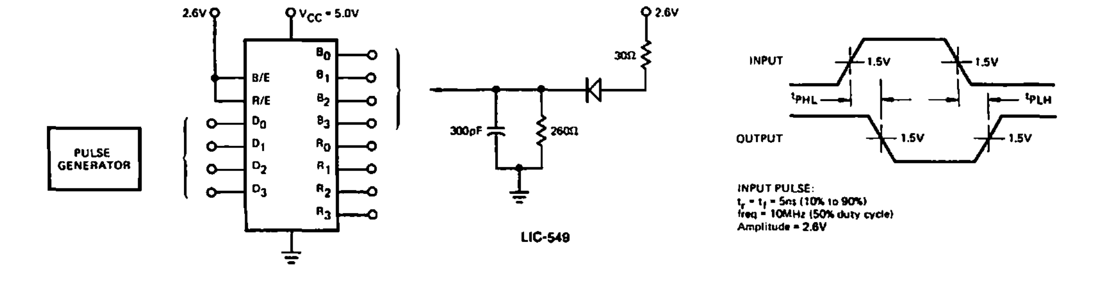


Figure 1

PROPAGATION DELAY (Bus to Receiver Out)

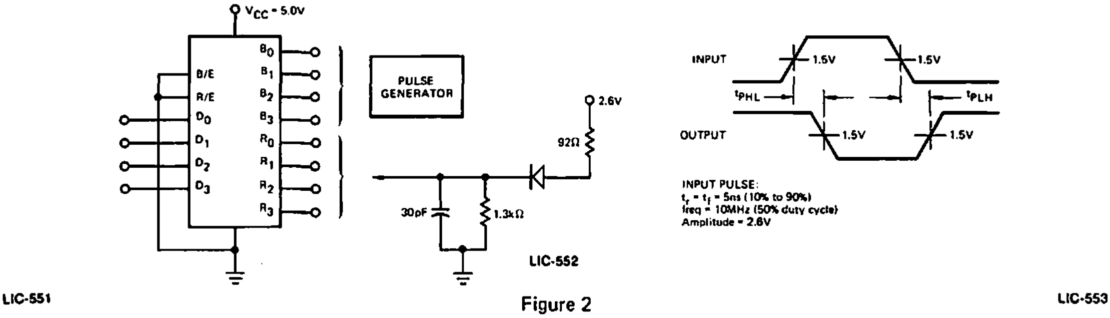


Figure 2

PROPAGATION DELAY (Bus Enable to Bus Output)

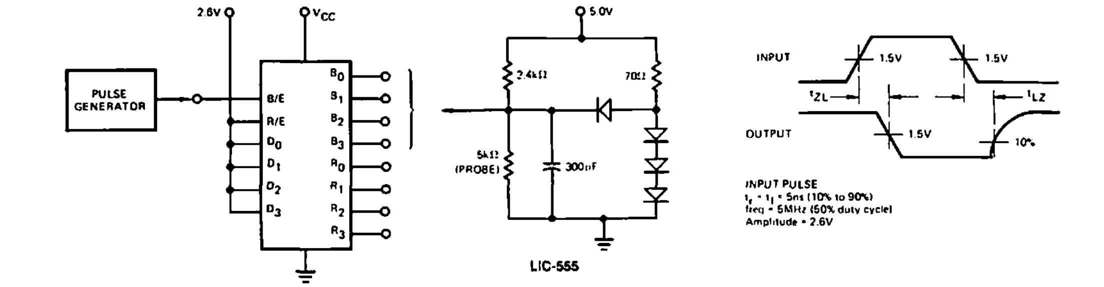


Figure 3

PROPAGATION DELAY (Receive Enable to Receive Output)

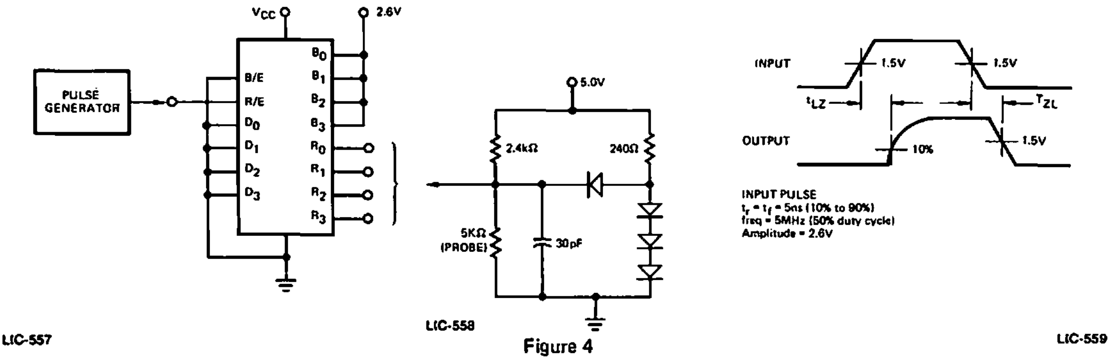
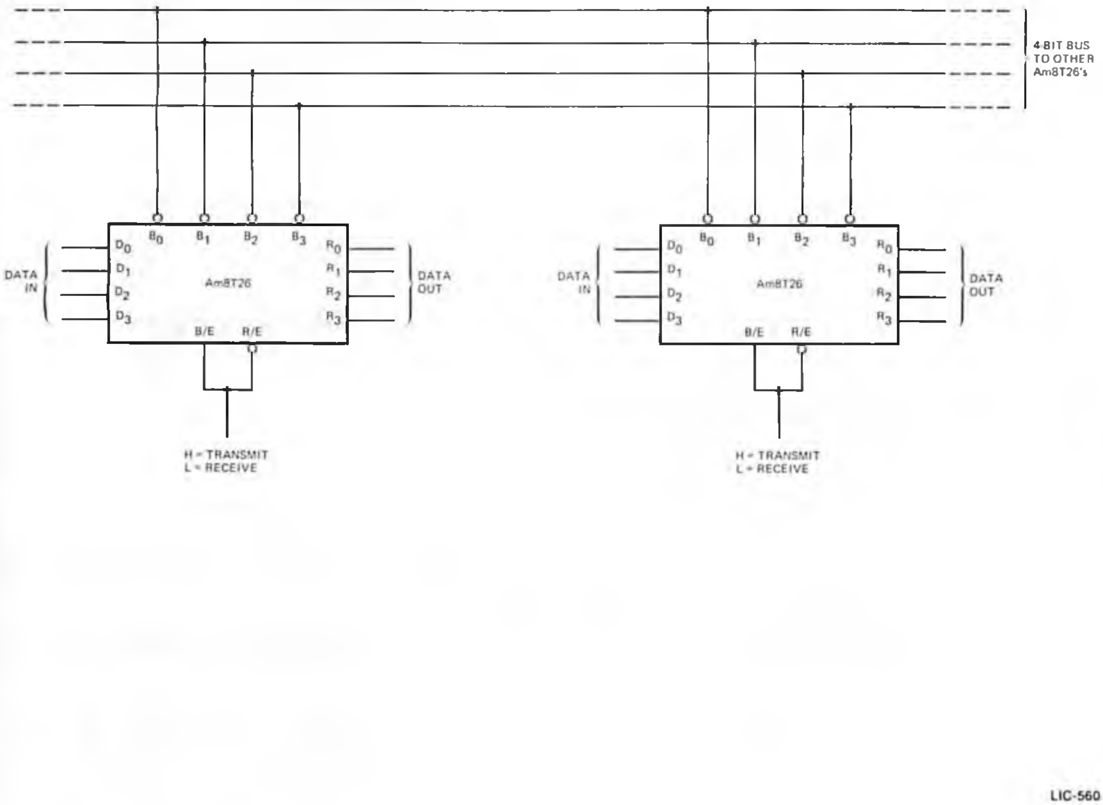
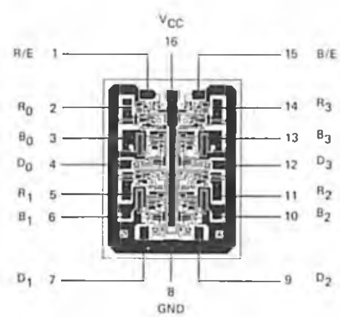


Figure 4

APPLICATION



Metallization and Pad Layout



DIE SIZE 0.063" X 0.082"

Am8T26A·Am8T28

Schottky Three-State Quad Bus Driver/Receiver

Distinctive Characteristics

- Advanced Schottky technology
- 48mA driver sink current
- Three-state outputs on driver and reciever
- PNP inputs
- Am8T26A has inverting outputs
- Am8T28 has non-inverting outputs
- Driver propagation delay – 14ns max. for 8T26A; 17ns max. for 8T28
- Receiver propagation delay – 14ns max. for 8T26A; 17ns max. for 8T28
- 100% reliability assurance testing in compliance with MIL-STD-883

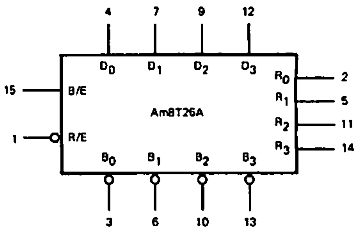
FUNCTIONAL DESCRIPTION

The Am8T26A/Am8T28 are high speed bus transceivers consisting of four bus drivers with three-state outputs and four bus receivers, also with three-state outputs. Each driver output is internally connected to a receiver input. Both the drivers and receivers have PNP inputs.

One buffered common "bus enable" input is connected to the four drivers and another buffered common "receiver enable" input is connected to the receivers. A LOW on the bus enable (B/E) input forces the four driver outputs to the high-impedance state. A HIGH on the bus enable allows input data to be transferred onto the data bus.

A HIGH on the receiver enable (R/E) input forces the four receiver outputs to the high-impedance state while a LOW on the receiver enable input allows the received data to be transferred to the output. The complementary design of the bus enable and receiver enable inputs allows these control inputs to be connected together externally such that a single transmit/receive function is derived.

LOGIC SYMBOL

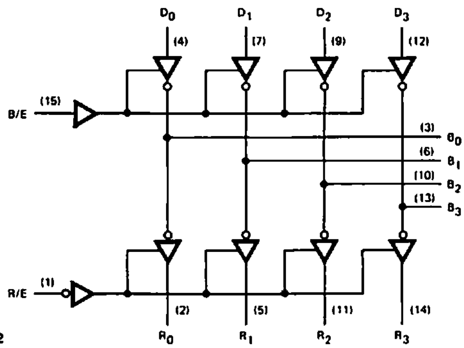


V_{CC} = Pin 16
GND = Pin 8

LIC-561

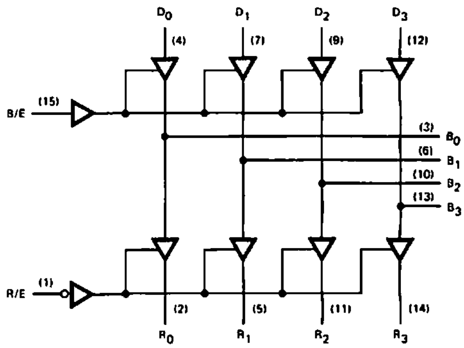
LOGIC DIAGRAMS

Am8T26A
Inverting Output (Three-State)



LIC-562

Am8T28
Non-Inverting Output (Three-State)

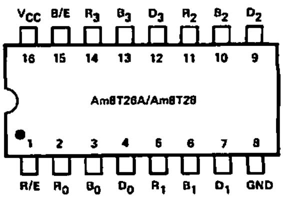


LIC-563

ORDERING INFORMATION

Package Type	Temperature Range	Am8T26A Order Number	Am8T28 Order Number
Molded DIP	0°C to +75°C	N8T26AB	N8T28B
Hermetic DIP	0°C to +75°C	N8T26AF	N8T28F
Dice	0°C to +75°C	AM8T26AXC	AM8T28XC
Hermetic DIP	–55°C to +125°C	S8T26AF	S8T28F
Dice	–55°C to +125°C	AM8T26AXM	AM8T28XM

CONNECTION DIAGRAM
(Top View)



Note: Pin 1 is marked for orientation.

LIC-564

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	–0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	–0.5V to $+V_{CC}$ max.
DC Input Voltage	–0.5V to +5.5V
DC Output Current, Into Outputs (Receiver)	30mA
DC Output Current, Into Outputs (BUS)	80mA
DC Input Current	–30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

N8T26A, N8T28 T_A = 0°C to +75°C(COM'L) MIN. = 4.75 V MAX. = 5.25 V

S8T26A, S8T28 T_A = –55°C to +125°C(MIL) MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
Driver						
I_{IL}	Low Level Input Current	V_{IN} = 0.4 V			–200	μA
I_{IL}	Low Level Input Current (Disabled)	V_{IN} = 0.4 V			–25	μA
I_{IH}	High Level Input Current (D_{IN}, D_E)	V_{IN} = V_{CC}MAX.			25	μA
V_{OL}	Low Level Output Voltage	I_{OUT} = 48mA (Note 5)			0.5	Volts
V_{OH}	High Level Output Voltage	I_{OUT} = –10mA, V_{CC} = V_{CC}MIN. (Note 6)	2.4			Volts
I_{OS}	Short Circuit Output Current	V_{OUT} = 0 V, V_{CC} = V_{CC}MAX. (Note 4)	–50		–150	mA
Receiver						
I_{IL}	Low Level Input Current	V_{IN} = 0.4 V			–200	μA
I_{IH}	High Level Input Current (R_E)	V_{IN} = V_{CC}MAX.			25	μA
V_{OL}	Low Level Output Voltage	I_{OUT} = 20mA (Note 5)			0.5	Volts
V_{OH}	High Level Output Voltage	I_{OUT} = –100μA, V_{CC} = 5.0 V	3.5			Volts
		I_{OUT} = –2.0mA (Note 6)	2.4			
I_{OS}	Short Circuit Output Current	V_{OUT} = 0 V, V_{CC} = V_{CC}MAX.	–30		–75	mA
Both Driver and Receiver						
V_{TL}	Low Level Input Threshold Voltage		0.85			Volts
V_{TH}	High Level Input Threshold Voltage				2.0	Volts
I_O	Low Level Output Off Leakage Current	V_{OUT} = 0.5 V			–100	μA
	High Level Output Off Leakage Current	V_{OUT} = 2.4 V			100	μA
V_I	Input Clamp Voltage	I_{IN} = –12mA			–1.0	Volts
PWR/ I_{CC}	Power/Current Consumption Am8T26A	V_{CC} = V_{CC}MAX.			457/87	mW/mA
	Power/Current Consumption Am8T28	V_{CC} = V_{CC}MAX.			578/110	

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0 V)

Parameters	Description	Test Conditions	Am8T26A Min.	Am8T26A Typ.	Am8T26A Max.	Am8T28 Min.	Am8T28 Typ.	Am8T28 Max.	Units
t_{PLH}	Driver Input to Bus	Figure 1		10	14		13	17	ns
t_{PHL}				10	14		13	17	
t_{PLH}	Bus to Receiver Output	Figure 2		9.0	14		12	17	ns
t_{PHL}				6.0	14		9.0	17	
t_{ZL}	Driver Enable to Bus	Figure 3		19	25		21	28	ns
t_{LZ}				15	20		18	23	
t_{ZL}	Receiver Enable to Receiver Output	Figure 4		15	20		18	23	ns
t_{LZ}				10	15		13	18	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual inout currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Output sink current is supplied through a resistor to V_{CC}.
6. Measurements apply to each output and the associated data input independently.

DEFINITION OF FUNCTIONAL TERMS

D_0, D_1, D_2, D_3 The four driver inputs.

B_0, B_1, B_2, B_3 The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the driver inputs is non-inverted.

B/E Bus enable input. When the bus enable input is LOW, the four driver outputs are in the high-impedance state.

R/E Receiver enable input. When the receiver enable input is HIGH, the four receiver outputs are in the high-impedance state.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	LOW Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
R/E	1	1/8	–	–
R_0	2	–	50	10
B_0	3	1/16	250	25
D_0	4	1/8	–	–
R_1	5	–	50	10
B_1	6	1/16	250	25
D_1	7	1/8	–	–
GND	8	–	–	–
D_2	9	1/8	–	–
B_2	10	1/16	250	25
R_2	11	–	50	10
D_3	12	1/8	–	–
B_3	13	1/16	250	25
R_3	14	–	50	10
B/E	15	1/8	–	–
V_{CC}	16	–	–	–

A TTL Unit Load is defined as –1.6mA measured at 0.4V LOW and 40μA measured at 2.4V HIGH.

DRIVER FUNCTION TABLE

INPUTS		Am8T26A OUTPUT	Am8T28 OUTPUT
B/E	D_i	B_i	B_i
L	X	Z	Z
H	L	H	L
H	H	L	H

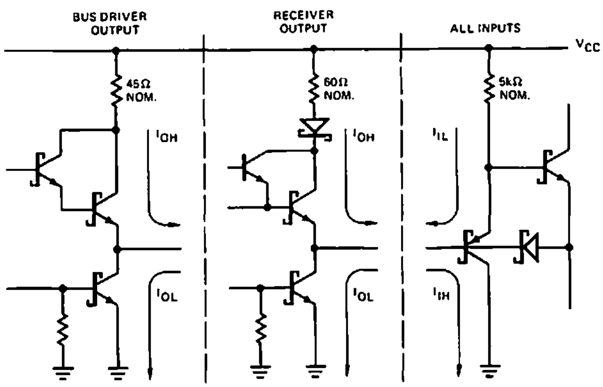
L = LOW X = Don't Care
H = HIGH Z = High Impedance
i = 0, 1, 2, or 3

RECEIVER FUNCTION TABLE

INPUTS		Am8T26A OUTPUT	Am8T28 OUTPUT
R/E	B_i	R_i	R_i
H	X	Z	Z
L	L	H	L
L	H	L	H

L = LOW X = Don't Care
H = HIGH Z = High Impedance
i = 0, 1, 2, or 3

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

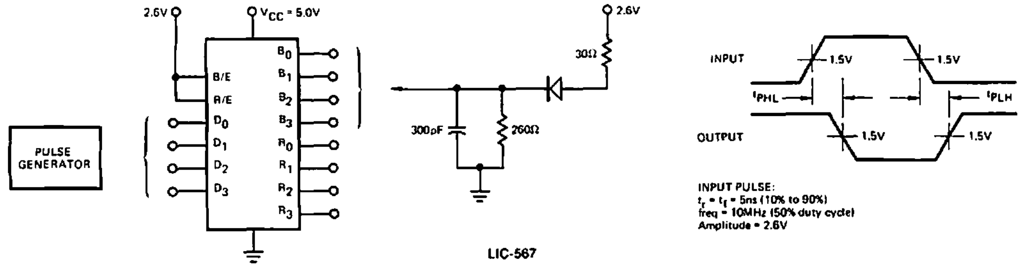


Note: Actual current flow direction shown.

LIC-565

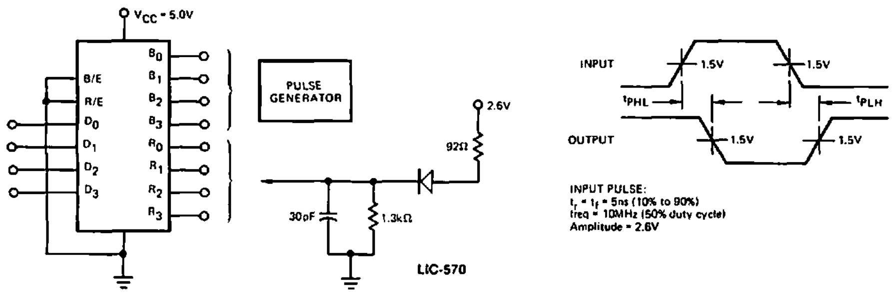
AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY (Data In to Bus)



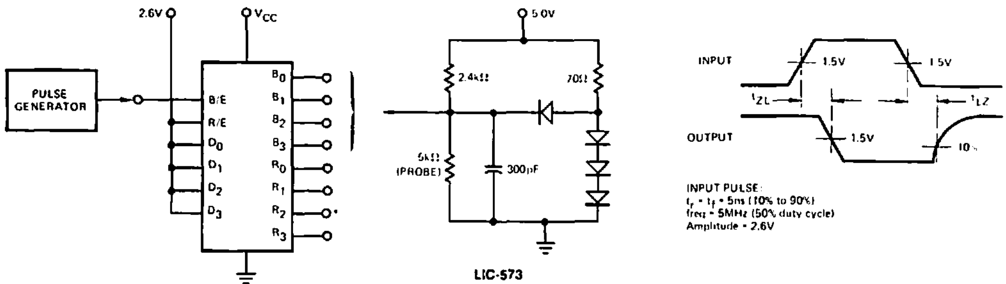
LIC-566 Figure 1 LIC-568

PROPAGATION DELAY (Bus to Receiver Out)



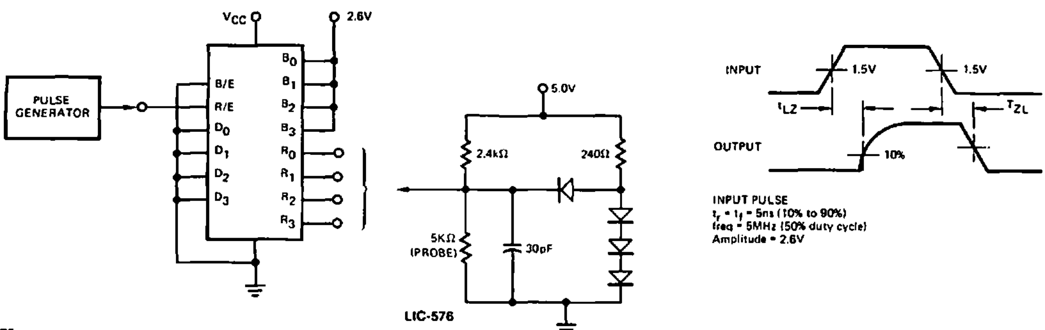
LIC-569 Figure 2 LIC-571

PROPAGATION DELAY (Bus Enable to Bus Output)



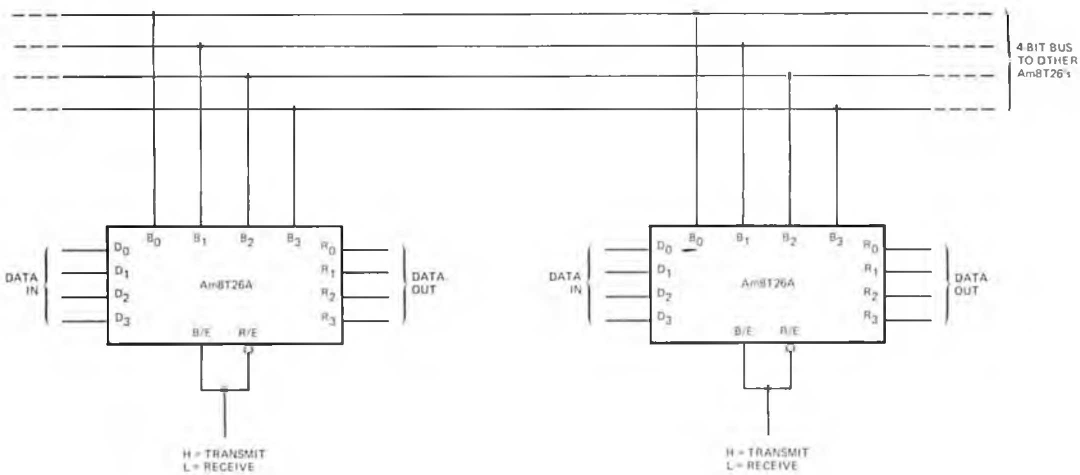
LIC-572 Figure 3 LIC-574

PROPAGATION DELAY (Receive Enable to Receive Output)



LIC-575 Figure 4 LIC-577

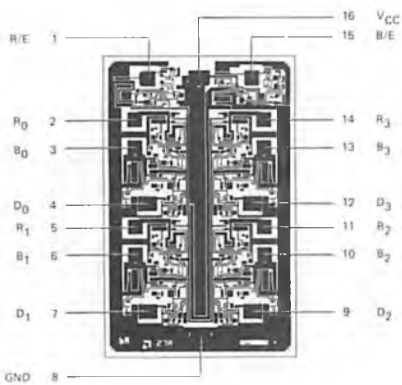
APPLICATION



LIC-578

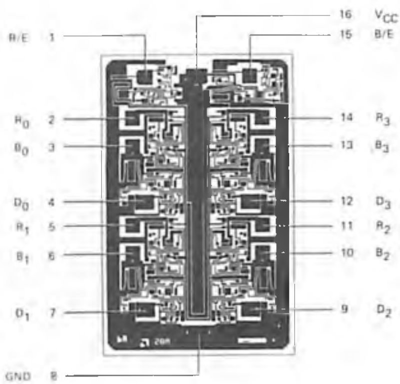
Metallization and Pad Layouts

Am8T26A



DIE SIZE 0.058" X 0.091"

Am8T28



DIE SIZE 0.058" X 0.091"

Am9614

Dual Differential Line Driver

Distinctive Characteristics

- Dual differential line driver with complementary outputs
- Single 5-volt supply
- DTL, TTL compatible
- Short-circuit protected outputs
- Able to drive 50Ω terminated transmission lines
- 100% reliability assurance testing in compliance with MIL-STD-883

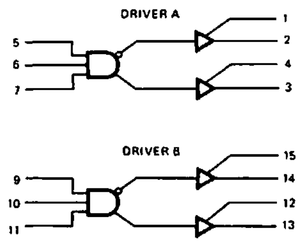
FUNCTIONAL DESCRIPTION

The Am9614 is a DTL, TTL compatible line driver operating off a single 5V supply.

The Am9614 is designed to drive either differential or single-ended, back-matched or terminated transmission lines. The device has the active pull-down and active pull-up circuits split and brought out to adjacent pins. This allows multiplex operation (wire-AND) at the driving end in either the single-ended mode via the uncommitted collector or in the differential mode by use of the active pull-ups on one side and the uncommitted collectors on the other. The complementary outputs of the Am9614 give great application flexibility.

The Am9614 has short-circuit protected active pull-ups, and incorporates input clamp diodes to reduce the effect of line transients, and can drive into 50Ω terminated transmission lines.

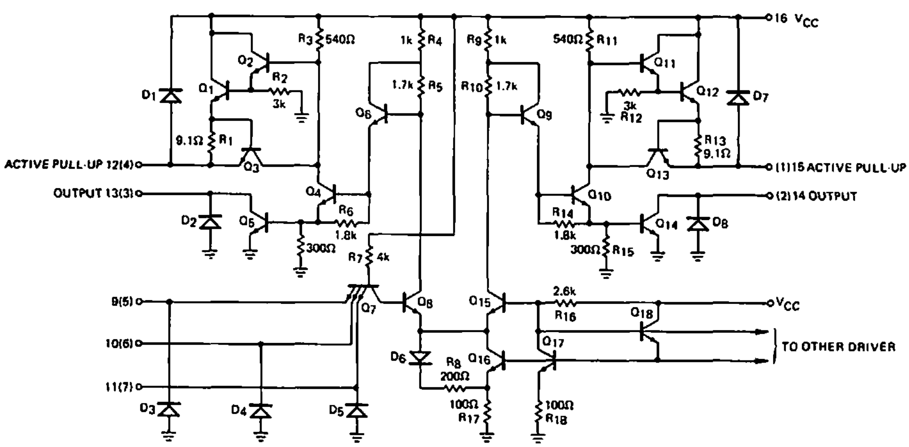
LOGIC DIAGRAMS



V_{CC} = Pin 16
GND = Pin 8

LIC-579

CIRCUIT DIAGRAM (1/2 Am9614)



Notes: 1. Circuit shown for one driver only.
2. Pin numbers in parenthesis refer to the other driver.

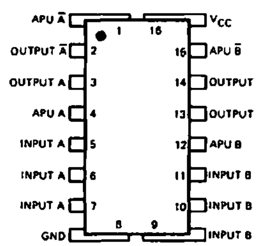
LIC-580

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	9614DM
Flat Pak	−55°C to +125°C	9614FM
Dice	−55°C to +125°C	AM9614XM
Hermetic DIP	0°C to +70°C	9614DC
Molded DIP	0°C to +70°C	9614PC
Dice	0°C to +70°C	AM9614XC

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

LIC-581

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to $+V_{CC}$ max
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Ouputs	200mA
DC Input Current	Note 1

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

9614XM (MIL)	T_A = −55°C to +125°C	V_{CC}MIN. = 4.50V	V_{CC}MAX. = 5.50V
9614XC (COM'L)	T_A = 0°C to +70°C	V_{CC}MIN. = 4.75V	V_{CC}MAX. = 5.25V

DC Characteristics (Note 2)

Parameters	Description	Test Conditions		T_A MIN. Min.	T_A MIN. Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_A MAX. Min.	T_A MAX. Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −10mA		2.4		2.4	3.2		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 40mA	MIL		0.4		0.2	0.4		0.4	Volts
			COM'L		0.45		0.2	0.45		0.45	
V_{IH}	Input HIGH Voltage	V_{CC} = MIN.	MIL	2.0		1.7	1.5		1.4		Volts
			COM'L	1.9		1.8	1.5		1.6		
V_{IL}	Input LOW Voltage	V_{CC} = MAX.	MIL		0.8		1.3	0.9		0.8	Volts
			COM'L		0.85		1.3	0.85		0.85	
I_F	Input Load Current	V_{CC} = MAX.	V_F = 0.4V, MIL		−1.6		−1.1	−1.1		−1.6	mA
			V_F = 0.45V, COM'L		−1.6		−1.0	−1.6		−1.6	
I_R	Reverse Input Current	V_{CC} = MAX. V_R = 4.5V			60			60		60	μA
I_{SC}	Short Circuit Current	V_{CC} = MAX., V_O = 0V				−40	−90	−120			mA
I_{PD}	Power Supply Current	V_{CC} = MAX., Inputs = 0V			48.7		33	48.7		48.7	mA
		V_{CC} = 7.0V, Inputs = 0V	COM'L				46	70			
			MIL				46	65.7			
I_{CEX}	Reverse Output Current	V_{CC} = MAX	V_{CEX} = 12V, MIL		100		10	100		200	μA
			V_{CEX} = 5.25V, COM'L		100		10	100		200	
V_{OLC}	Output Low Clamp Voltage	V_{CC} = MAX., I_{OLC} = −40mA					−0.8	−1.5			Volts
V_{IC}	Input Clamp Voltage	V_{CC} = MIN., I_{IC} = −12mA					−1.0	−1.5			Volts

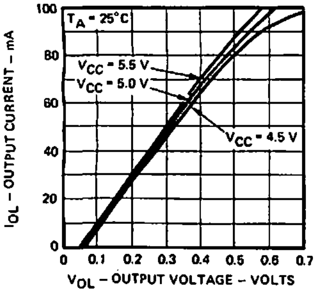
Switching Characteristics (T_A = 25°C unless otherwise specified)

Parameters	Description	Test Conditions	9614XM Min.	9614XM Typ.	9614XM Max.	9614XC Min.	9614XC Typ.	9614XC Max.	Units
t_{pd+}	Turn Off Delay	V_{CC} = 5.0V, C_L = 30pF, V_M = 1.5V, Refer to Fig. 1		14	20		14	30	ns
t_{pd-}	Turn On Delay			18	20		18	30	ns

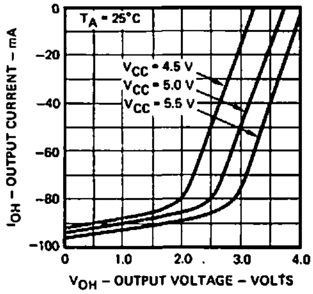
Notes: 1. Maximum current defined by DC input voltage.
2. For conditions shown as MIN. or MAX. use the appropriate value specified under electrical characteristics for the applicable device type or grade.

TYPICAL ELECTRICAL CHARACTERISTICS

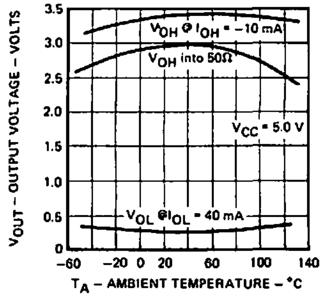
Output Low Current Versus Output Low Voltage



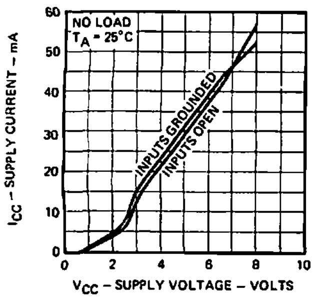
Output High Current Versus Output High Voltage



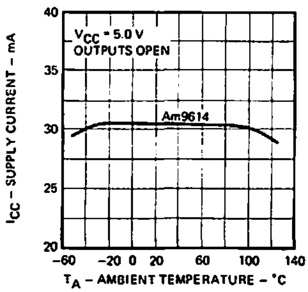
Logic Levels Versus Ambient Temperature



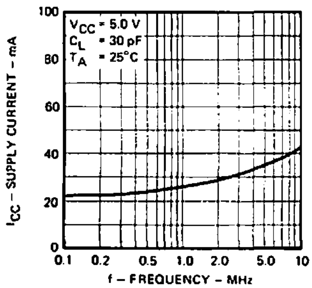
Supply Current Versus Supply Voltage



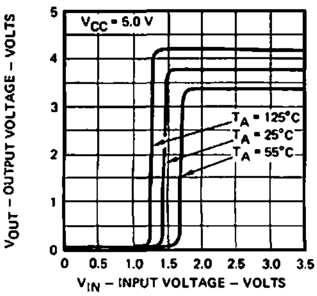
Supply Current Versus Temperature



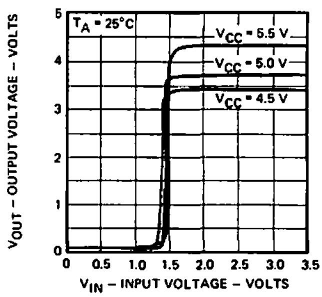
Supply Current Versus Operating Frequency



Transfer Characteristics Versus Temperature



Transfer Characteristics Versus Supply Voltage



LIC-582

USERS NOTES

DIFFERENTIAL LINES. The Am9614 dual differential line driver can be used with the Am9615 dual differential line receiver to form an interconnection system which can tolerate extremely noisy environments and interconnect equipments where there is a ±15V difference in voltage level of the equipment grounds. Two wires are used for each channel to form a balanced transmission line. This method of sending data between equipments offers extremely high protection from common mode noise and also gives excellent DC noise margins.

MATCHING. Transmission lines can be matched in a number of ways. The most widely used method is to terminate the line at the receiving end in its characteristic impedance. This impedance is connected across the input terminals of the receiver. A 130Ω resistor is included at the + input of each receiver for matching twisted pairs and this resistor, or if the characteristic impedance is not 130Ω, a discrete resistor, is connected between the two receiver inputs. This method of matching causes a DC component in the signal. Power is dissipated in the resistor and the signal is attenuated. The DC component can be effectively removed by connecting a large capacitor in series with the terminating resistor.

The transmission line can also be terminated through the receiver power supply by placing equal value resistors from the + input of the receiver to V_{CC} and from the – input to ground. This method again has the disadvantage that a DC signal component exists, attenuation occurs, and power is dissipated in the terminating resistors but it does allow multiplexed operation in the balanced differential mode.

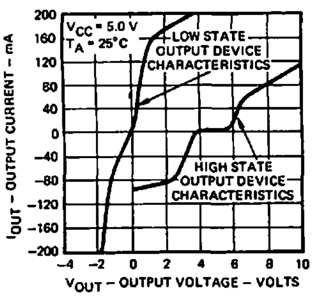
An alternate method to matching at the receiver is to back match at the driver. A resistor is placed in series with the line so that the signal from the driver which is reflected at the high input impedance of the receiver is absorbed at the driver. This method does not have a DC component and therefore no attenuation occurs and power is not dissipated in the resistor. For balanced differential driving a resistor is required in series with each line. The table below shows the value of each matching resistor required for lines of different characteristic impedance.

MULTIPLEXING. When operating in the balanced differential mode the Am9614 driver can be OR tied with other devices to allow multiplexed operation. The open collector NAND outputs are connected together and the active pull-up AND outputs are connected together. Selection of the active driver can be made by two of the three logic inputs on the driver. Multiplexed operation can only be performed with the lines terminated to the appropriate voltage level at the driver so that this method has a DC component and power is dissipated in the terminating resistors.

TYPICAL DC CHARACTERISTICS
FOR MATCHING TO TRANSMISSION LINE

BACK MATCHING TABLE

Z_O	R_M (ohms) Differential
50	12
75	24
92	33
100	36
130	54
300	140
600	290

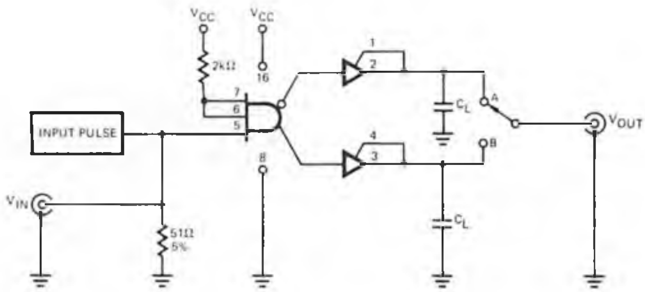


LIC-583

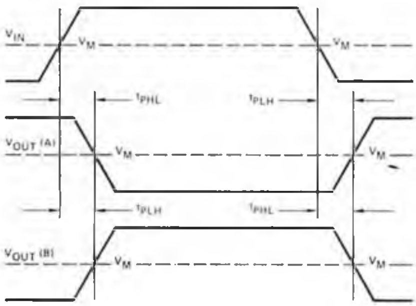
LOADING RULES

Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
APU A	1	—	166	—
Output A	2	—	—	25
Output A	3	—	—	25
APU A	4	—	166	—
Input A	5	1	—	—
Input A	6	1	—	—
Input A	7	1	—	—
GND	8	—	—	—
Input B	9	1	—	—
Input B	10	1	—	—
Input B	11	1	—	—
APU B	12	—	166	—
Output B	13	—	—	25
Output B	14	—	—	25
APU B	15	—	166	—
V_{CC}	16	—	—	—

SWITCHING CIRCUITS AND WAVEFORMS



LIC-584

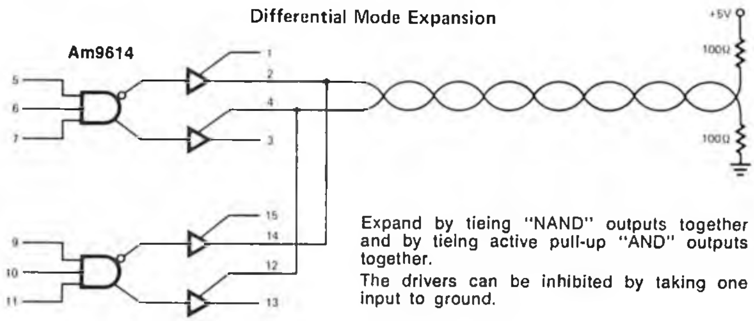


INPUT PULSE
Frequency = 500 kHz
Amplitude = 3.0 ±0.1 V
Pulse Width = 110 ±10 ns
$t_r = t_f \leq 5.0$ ns

LIC-585

APPLICATION

Differential Mode Expansion

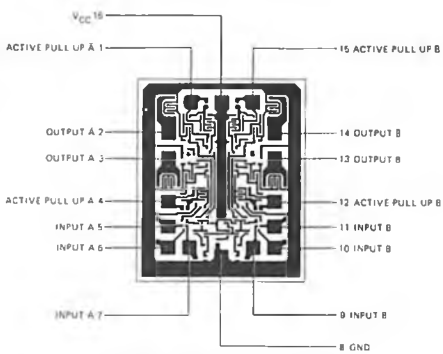


Expand by tieing "NAND" outputs together and by tieing active pull-up "AND" outputs together.

The drivers can be inhibited by taking one input to ground.

LIC-586

Metallization and Pad Layout



DIE SIZE 0.052" X 0.063"

Am9616

Triple EIA RS-232C/MIL-STD-188C Line Driver

Distinctive Characteristics

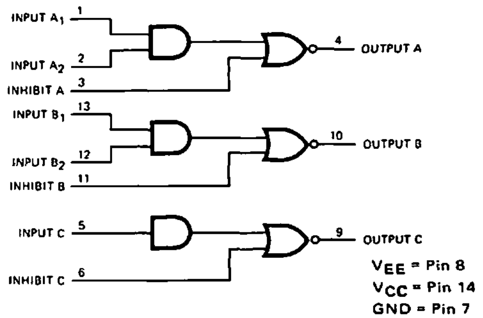
- Conforms to EIA RS-232C and CCITT V.24 specifications and/or MIL-STD-188C
- Short circuit protected output
- Internal slew rate limiting
- Supply independent output swing
- 100% reliability assurance testing in compliance with MIL-STD-883
- TTL/DTL compatible input

FUNCTIONAL DESCRIPTION

The Am9616 is a triple line driver specifically designed to meet the EIA RS-232C and CCITT V.24 and/or MIL-STD-188C electrical interface requirements. Each driver accepts DTL/TTL logic levels and converts them to EIA/CCITT levels for data transmission between equipment. The output slew rate of each driver is internally limited, but can be lowered by an external capacitor. All outputs are short circuit protected, and protected against fault conditions specified in RS-232C. A HIGH logic level on the inhibit input forces the driver output to V_{OL} or mark state.

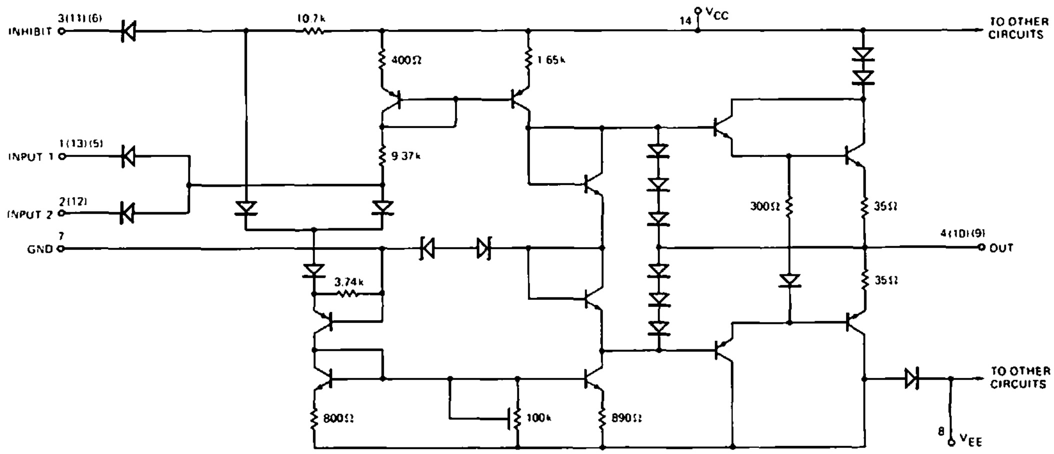
The Am9616EXC and Am9616XM meets the requirements of MIL-STD-188C and EIA RS-232C. The Am9616XC conforms to the requirements of EIA RS-232C.

LOGIC SYMBOL



LIC-587

CIRCUIT DIAGRAM
(One Driver Shown)

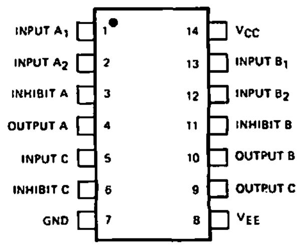


LIC-588

Am9616 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	9616DM
Dice	−55°C to +125°C	AM9616XM
Hermetic DIP	0°C to +75°C	9616EDC
Hermetic DIP	0°C to +75°C	9616DC
Molded DIP	0°C to +75°C	9616EPC
Molded DIP	0°C to +75°C	9616PC
Dice	0°C to +75°C	AM9616XC

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-589

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +75°C
Supply Voltage to Ground Potential	
V_{CC}	+15 V
V_{EE}	−15 V
DC Voltage Applied to Outputs	±15 V
DC Input Voltage	−1.5 V to +6 V
Lead Temperature (Soldering, 30 sec.)	300°C

Am9616XM AND Am9616EXC
RS232-C AND MIL-STD-188C

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:
Am9616XM (MIL) $T_A = -55°C$ to $+125°C$
Am9616EXC (COM'L) $T_A = 0°C$ to $+70°C$
$V_{CC} = +12V \pm 10\%$, $V_{EE} = -12V \pm 10\%$, $R_L = 3k\Omega$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage			5.0	6.0	7.0	Volts
V_{OL}	Output LOW Voltage			−7.0	−6.0	−5.0	Volts
	Ripple Rejection	Power Supply Ripple = $2.4V_{p-p}$, f = 400Hz			0.25		% of V_{OUT}
V_{OH} to V_{OL}	Output HIGH Voltage to Output LOW Voltage, Magnitude Matching Error					±10	%
R_{OUT}	Output Resistance, Power On	$R_L = 6k\Omega$, $\Delta I_L = 10mA$			75		Ω
I_{SC+}	Positive Output Short Circuit Current				22	100	mA
I_{SC-}	Negative Output Short Circuit Current			−100	−22		mA
V_{IH}	Input HIGH Voltage			2.0			Volts
V_{IL}	Input LOW Voltage					0.8	Volts
I_{IH}	Input HIGH Current	$V_{IN} = 2.4V$				40	µA
		$V_{IN} = 5.5V$				1.0	mA
I_{IL}	Input LOW Current	$V_{IN} = 0.4V$		−1.6			mA
R_{OUT}	Output Resistance, Power Off	$-2.0V < V_{OUT} < +2.0V$ All Inputs and Supply Pins Grounded		300			Ω
I_+	Positive Supply Current	$T_A = +25°C$	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 0.8V$		15	22	mA
			$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0V$		7.5	13	
I_-	Negative Supply Current	$T_A = +25°C$	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 0.8V$		0	−1	mA
			$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0V$		−15	−22	

AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE OF T_A = 0°C TO 70°C (Note 2)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
	Positive Slew Rate	$0pF < C_L < 2500pF$ $R_L > 3k\Omega$	4.0	15	30	V/µs
	Negative Slew Rate	$0pF < C_L < 2500pF$ $R_L > 3k\Omega$	−30	−15	−4.0	V/µs
t_{PLH}	Propagation Delay Time	No Load		320		ns
t_{PHL}	Propagation Delay Time	No Load		320		ns

Notes: 1. Typical values are at $V_{CC} = 12V$, $V_{EE} = -12V$, $T_A = 25°C$.
2. An external capacitor may be needed to meet signal wave shaping requirements of MIL-STD-188C at the applicable modulation rate.

ELECTRICAL CHARACTERISTICS

Am9616XC
EIA RS-232-C

The Following Conditions Apply Unless Otherwise Noted:
T_A = 0°C to +75°C, V_{CC} = +12V ± 10%, V_{EE} = −12V ± 10%, R_L = 3kΩ

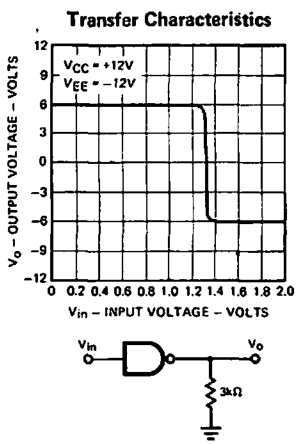
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

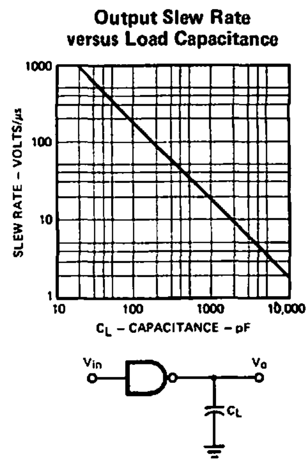
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{IN_1} or V_{IN_2} = $V_{INHIBIT}$ = 0.8 V	+5.0	+6.0	+7.0	Volts
V_{OL}	Output LOW Voltage	V_{IN_1} = V_{IN_2} = $V_{INHIBIT}$ = 2.0 V	−7.0	−6.0	−5.0	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage			0.8	Volts
I_{IL}	Input LOW Current	V_{IN_1} = V_{IN_2} = 0.4 V or $V_{INHIBIT}$ = 0.4 V		−1.2	−1.6	mA
I_{IH}	Input HIGH Current	V_{IN_1} = V_{IN_2} = 2.4 V or $V_{INHIBIT}$ = 2.4 V			40	μA
I_{SC}	Output Short Circuit Current (Positive)	R_L = 0Ω, V_{IN_1} or V_{IN_2} = $V_{INHIBIT}$ = 0.8 V	−8	−17	−30	mA
I_{SE}	Output Short Circuit Current (Negative)	R_L = 0Ω, V_{IN_1} or V_{IN_2} = $V_{INHIBIT}$ = 2.0 V	+8	+17	+30	mA
I_{CC}	Total Positive Supply Current	V_{IN_1} = V_{IN_2} = $V_{INHIBIT}$ = 0.8 V		15	22	mA
		V_{IN_1} = V_{IN_2} = $V_{INHIBIT}$ = 2.0 V		7.5	13	
I_{EE}	Total Negative Supply Current	V_{IN_1} = V_{IN_2} = $V_{INHIBIT}$ = 0.8 V		0	−1	mA
		V_{IN_1} = V_{IN_2} = $V_{INHIBIT}$ = 2.0 V		−15	−22	

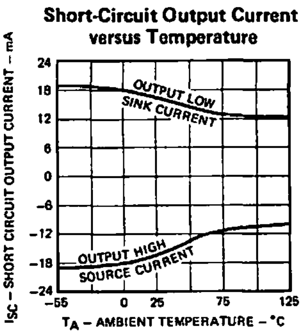
AC CHARACTERISTICS

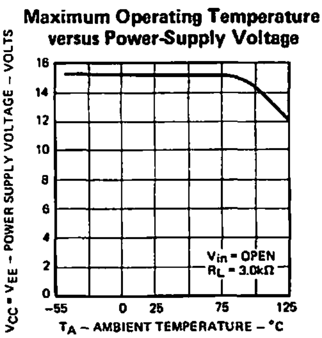
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Delay from Input LOW to Output HIGH	C_L = 15 pF, R_L = ∞		320	650	ns
t_{PHL}	Delay from Input HIGH to Output LOW			320	650	ns
	Positive Slew Rate	0 pF < C_L < 2500 pF, R_L > 3 kΩ	4.0	15	30	V/μs
	Negative Slew Rate		−30	−15	−4.0	V/μs

TYPICAL CHARACTERISTICS



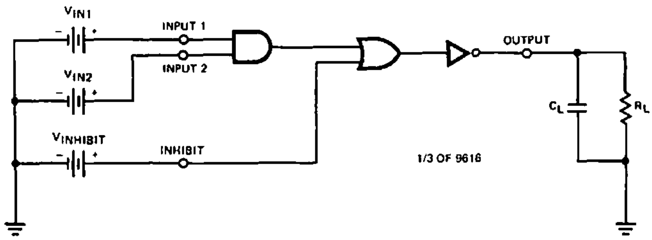






LIC-590

SWITCHING TEST CIRCUIT

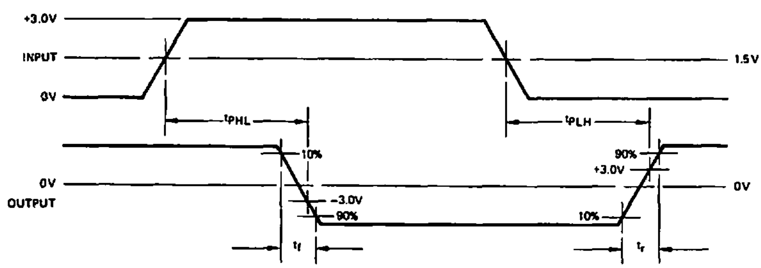


Note: Omit V_{IN2} for channel "C".

LIC-591

4

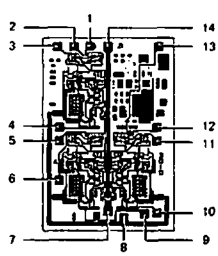
VOLTAGE WAVEFORMS



Pulse Generator Rise Time = 10 ± 5 ns.

LIC-592

Metallization and Pad Layout



DIE SIZE 0.069" X 0.103"

Am9617

RS-232C Line Reeeiver

Distinctive Characteristics

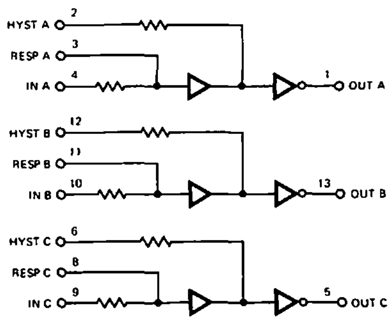
- Compatible with EIA RS-232C and CCITT V24 specifications.
- Input signal range ±30 volts
- Available in commercial and military temperature range
- Variable hysteresis
- 100% reliability assurance testing in compliance with MIL-STD-883
- Includes response control input and built-in hysteresis.

FUNCTIONAL DESCRIPTION

The Am9617 is a triple line receiver that meets both the CCITT TV24 and EIA RS-232C specifications. Each receiver has single data input that can accept signal swings of up to ±30V. The output of each receiver is TTL/DTL compatible, and includes a 2kΩ resistor pull-up to V_{CC}. Each receiver has a hysteresis input so that the hysteresis can be controlled by means of a series resistor between the HYST input and a response control input RESP.

Because of this hysteresis in switching thresholds, the device can receive signals with superimposed noise or with slow rise and fall times without generating oscillations on the output. The threshold levels may be offset by a constant voltage by applying a DC bias to the response control input. A capacitor added to the response control input will reduce the frequency response of the receiver for applications in the presence of high frequency noise spikes. The companion line driver is the Am9616.

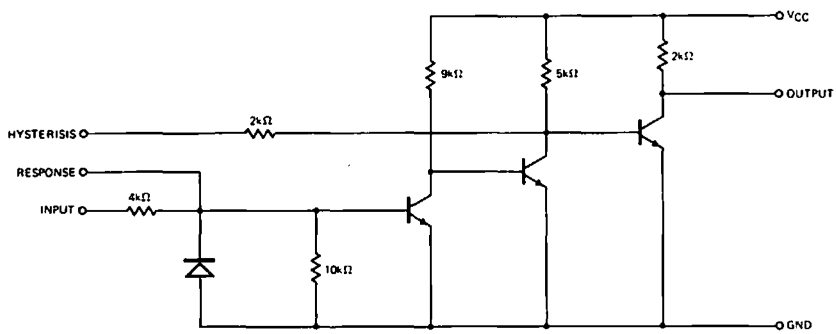
LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LIC-593

CIRCUIT DIAGRAM
(One Receiver)

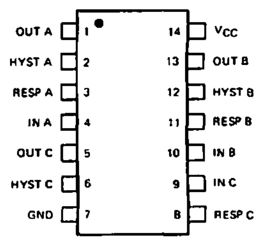


LIC-594

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	–55°C to +125°C	9617DM
Hermetic DIP	0°C to +75°C	9617DC
Molded DIP	0°C to +75°C	9617PC
Dice	–55°C to +125°C	AM9617XM
Dice	0°C to +75°C	AM9617XC

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

LIC-595

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +175°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous	–0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	–0.5 V to $+V_{CC}$ max.
Input Signal Range	–30 V to +30 V
Output Current, Into Outputs	30 mA
DC Input Current	Defined by Input Voltage Limits

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

Am9617XM (MIL) T_A = –55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

Am9617XC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V

Response Control Pin Open Unless Otherwise Specified

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
R_{IN}	Input Resistance	V_{IN} = ± 25V		3.0	4.0	7.0	kΩ
V_{IN}	Open Circuit Input Voltage				0.2	2.0	Volts
V_{OH}	Output HIGH Voltage	I_{OH} = –0.2mA, V_{CC} = Min. V_{IN} = –3.0V, 0V or Open Circuit		2.4	3.0		Volts
V_{OL}	Output LOW Voltage	I_{OL} = 8mA, V_{CC} = Min. V_{IN} = +3.0V			0.3	0.4	Volts
V_{IH}	Input HIGH Level Threshold	V_{OL} = 0.45V, V_{CC} = 5.0V Resp-Hyst Connected	–55°C	2.3		3.1	Volts
			0°C	1.9		2.5	
			25°C	1.75	2.0	2.25	
			75°C	1.45		1.90	
			125°C	1.20		1.65	
V_{IL}	Input LOW Level Threshold	V_{OH} = 2.5V, V_{CC} = 5.0V Resp-Hyst Connected	–55°C	0.85		1.65	Volts
			0°C	0.75		1.40	
			25°C	0.75	0.95	1.25	
			75°C	0.60		1.10	
			125°C	0.50		0.95	
V_{IO}	Open Loop Input Threshold		25°C	0.4	1.0	1.2	Volts
				0.4		1.4	
I_{IL}	Input LOW Current	V_{IN} = –25V	25°C	–3.6		–8.0	mA
						–8.3	
I_{IH}	Input HIGH Current	V_{IN} = +25V	25°C	3.6		8.0	mA
						8.3	
I_{SC}	Output Short Circuit Current	V_{IN} = 0.0V, V_{OUT} = 0.0V			2.5		mA
I_{CC}	Power Supply Current	V_{IN} = 5.0V, V_{CC} = Max.			12	18	mA

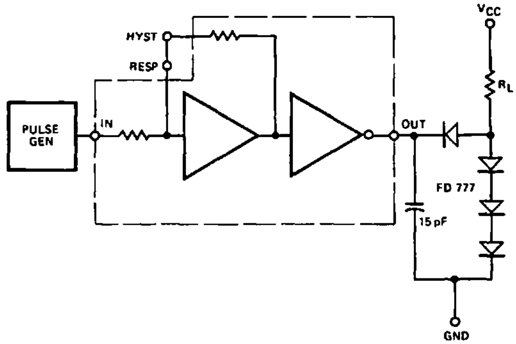
Notes: 1. Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

2. The input threshold margin for the device is greater than the voltage computed as the $V_{T+} - V_{T-}$ value. For the minimum value see the input threshold margin versus temperature graph.

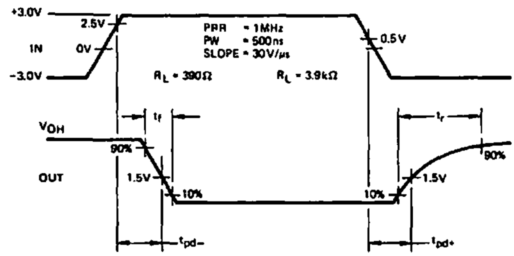
Switching Characteristics (T_A = 25°C, response control pin open, C_L = 15 pF)

Parameters	Definition	Test Conditions	Min.	Typ.	Max.	Units
t_{pd+}	Delay from Input LOW to Output HIGH	R_L = 3.9 kΩ		25	85	ns
t_{pd-}	Delay from Input HIGH to Output LOW	R_L = 390 Ω		25	50	ns
t_r	Output Rise Time (10% to 90%)	R_L = 3.9 kΩ		120	175	ns
t_f	Output Fall Time (90% to 10%)	R_L = 390 Ω		15	40	ns

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



LIC-596

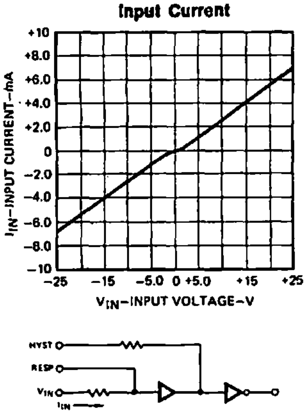


Note: Wiring capacitance should be minimized between Outputs, Hysterisis and Response Pins.

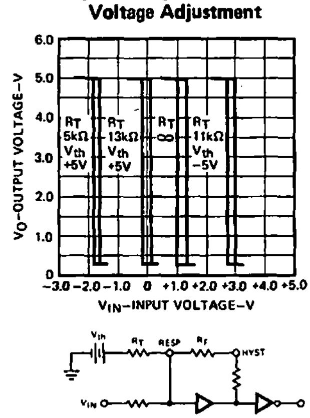
LIC-597

TYPICAL CHARACTERISTICS

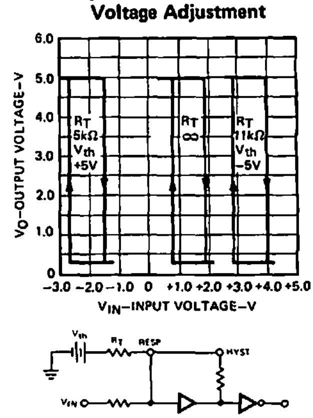
Input Current



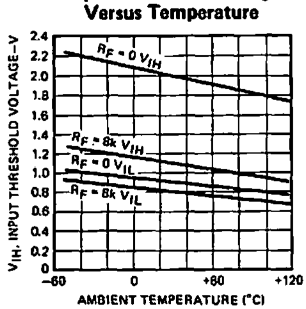
RF = 8k Input Threshold Voltage Adjustment



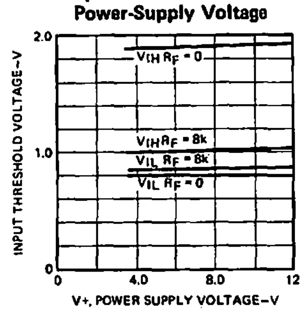
RF = 0 Input Threshold Voltage Adjustment



Input Threshold Voltage Versus Temperature

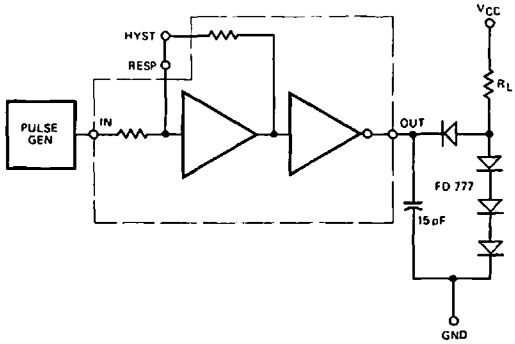


Input Threshold Versus Power-Supply Voltage

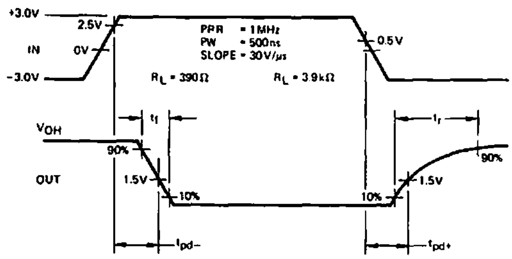


LIC-598

SWITCHING TIME TEST CIRCUIT & WAVEFORMS



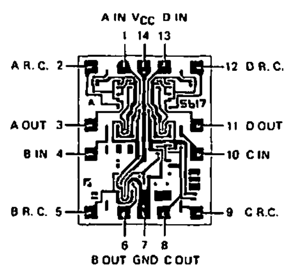
LIC-599



NOTE: Wiring capacitance should be minimized between Outputs, Hysterisis and Response Pins.

LIC-600

Metallization and Pad Layout



MOS Memory and Microprocessor Interface – Section V

Am0026/Am0026C

5MHz Two-Phase MOS Clock Driver

Distinctive Characteristics

- 20 ns rise and fall times with 1000 pF load
- 20 V output voltage swing
- ±1.5 amps output current drive
- High speed 5 to 10 MHz depending on load
- 100% reliability assurance testing in compliance with MIL-STD-883

5

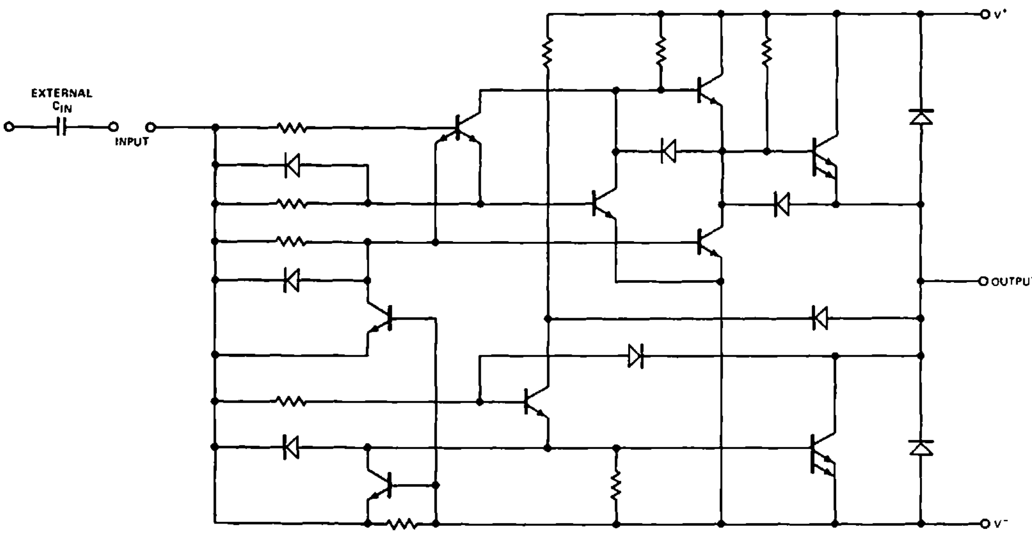
FUNCTIONAL DESCRIPTION

The Am0026 is a dual high speed MOS clock driver and interface circuit. The device is particularly suitable for driving two phase MOS circuits and can provide high speed operation even when driving into high capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. The output pulse width of the device is determined by the input pulse width.

The Am0026 can operate with a variety of MOS circuits. A popular application is a two-phase clock timer for driving long silicon gate shift registers such as the Am1402/3/4 series. A single clock driver is able to drive 10k bits at 5MHz. The device can also be used with standard dynamic MOS RAMS such as the 1103 to provide address and precharge drive for memories up to 8k by 16-bits.

The device is available in an 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, a one and one-half watt TO-8 package, and a 14-pin ceramic package.

SCHEMATIC DIAGRAM
(One Driver Shown)

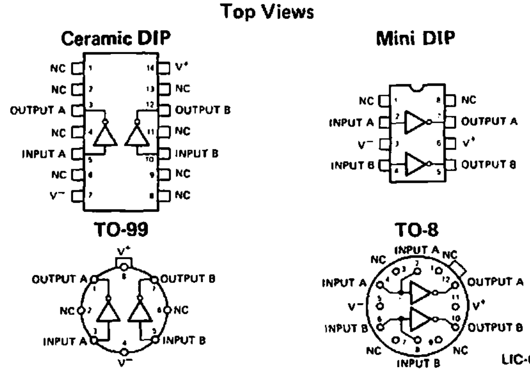


LIC-601

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
TO-99	0°C to 70°C	MH0026CH
Mini-DIP	0°C to 70°C	MH0026CN
TO-8	0°C to 70°C	MH0026CG
Ceramic DIP	0°C to 70°C	MMH0026CL
Dice	0°C to 70°C	AM0026XC
TO-99	–55°C to +125°C	MH0026H
TO-8	–55°C to +125°C	MH0026G
Ceramic DIP	–55°C to +125°C	MMH0026L
Dice	–55°C to +125°C	AM0026XM

CONNECTION DIAGRAMS
Top Views



LIC-602

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
$V^+ - V^-$ Differential Voltage	22 V
Input Current	100 mA
Input Voltage ($V_{IN} - V^-$)	5.5 V
Peak Output Current	1.5 A
Power Dissipation	See curves

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am0026C T_A = 0°C to 85°C (COM Range) $V^+ - V^-$ = 10 V to 20 V
Am0026 T_A = −55°C to +125°C (MIL Range) Unless Otherwise Specified

Parameter	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Logical "0")	V^+ = +5.0 V, V^- = −12.0 V, V_{IN} = −11.6 V	4.0	4.3		Volts
		$V_{IN} - V^-$ = 0.4 V	V^+ −1.0	V^+ −0.7		
V_{OL}	Output LOW Voltage (Logical "I")	V^+ = +5.0 V, V^- = −12.0 V, V_{IN} = −9.5 V		−11.5	−11.0	Volts
		$V_{IN} - V^-$ = 2.5 V		V^- +0.5	V^- +1.0	
V_{IH}	Input HIGH Level	V_{OUT} = V^- +1.0 V	2.5	1.5		Volts
V_{IL}	Input LOW Level	V_{OUT} = V^+ −1.0 V		0.6	0.4	Volts
I_{IL}	Input LOW Current	$V_{IN} - V^-$ = 0 V, V_{OUT} = V^+ −1.0 V		−0.005	−10	µA
I_{IH}	Input HIGH Current	$V_{IN} - V^-$ = 2.5 V, V_{OUT} = V^- +1.0 V		10	15	mA
$I_{CC\ ON}$	"ON" Supply Current	$V^+ - V^-$ = 20 V, $V_{IN} - V^-$ = 2.5 V		30	40	mA
$I_{CC\ OFF}$	"OFF" Supply Current	$V^+ - V^-$ = 20 V, $V_{IN} - V^-$ = 0.0 V	COM'L	10	100	µA
			MIL	50	500	

Notes: 1. These specifications apply for $V^+ - V^-$ = 10 V to 20 V, C_L = 1000 pF, over the temperature range −55°C to +125°C for the Am0026 and 0°C to +85°C for the Am0026C.
2. All typical values for T_A = 25°C.

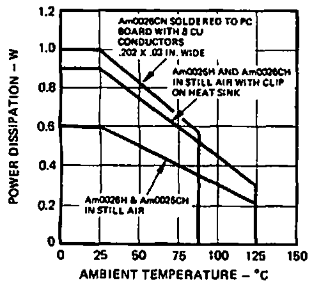
Switching Characteristics (Notes 1 and 2 Above)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL}	Turn On Delay		5.0	7.5	12	ns
t_{PLH}	Turn Off Delay		5.0	12	15	ns
t_r	Rise Time (Note 3)	$V^+ - V^-$ = 17 V, C_L = 250 pF		12		ns
		$V^+ - V^-$ = 17 V, C_L = 500 pF		15	18	
		$V^+ - V^-$ = 17 V, C_L = 1000 pF		20	35	
t_f	Fall Time (Note 3)	$V^+ - V^-$ = 17 V, C_L = 250 pF		10		ns
		$V^+ - V^-$ = 17 V, C_L = 500 pF		12	16	
		$V^+ - V^-$ = 17 V, C_L = 1000 pF		17	25	

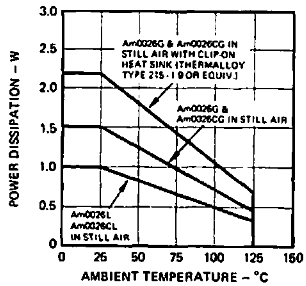
Note: 3. Rise and fall times are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall. See switching time waveforms.

TYPICAL PERFORMANCE CHARACTERISTICS

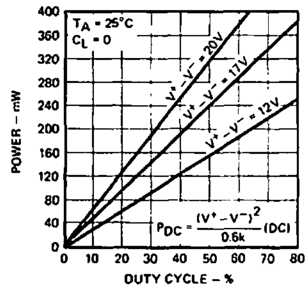
Power Ratings TO-5 & 8-Pin DIP



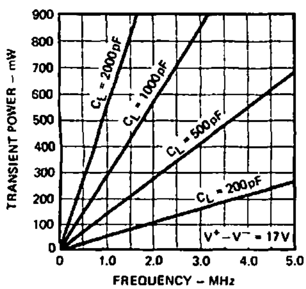
Power Rating TO-8 & 14-Pin DIP



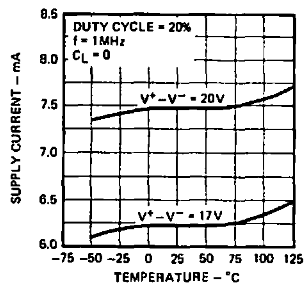
DC Power (P_{DC}) Versus Duty Cycle



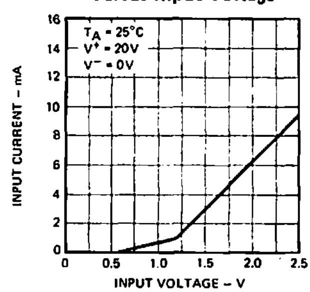
Transient Power (P_{AC}) Versus Frequency



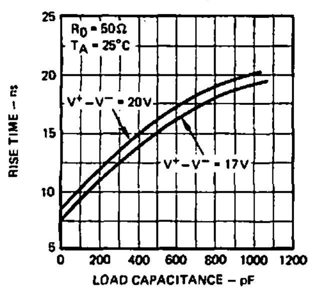
Supply Current Versus Temperature



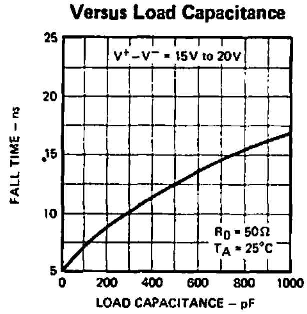
Input Current Versus Input Voltage



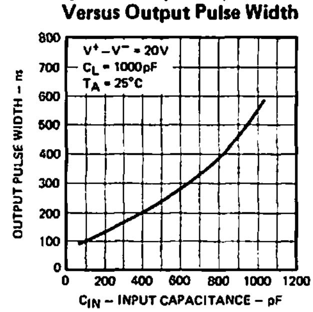
Rise Time Versus Load Capacitance



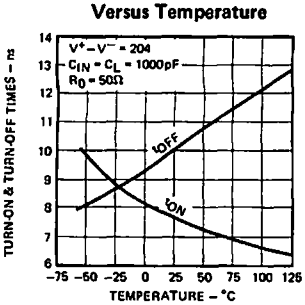
Fall Time Versus Load Capacitance



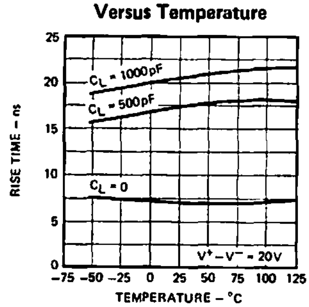
Optimum Input Capacitance Versus Output Pulse Width



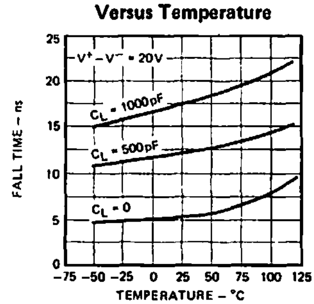
Turn-On & Turn-Off Time Versus Temperature



Rise Time Versus Temperature



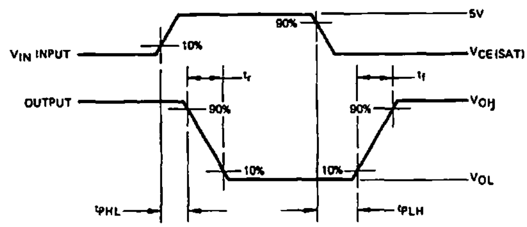
Fall Time Versus Temperature



LIC-603

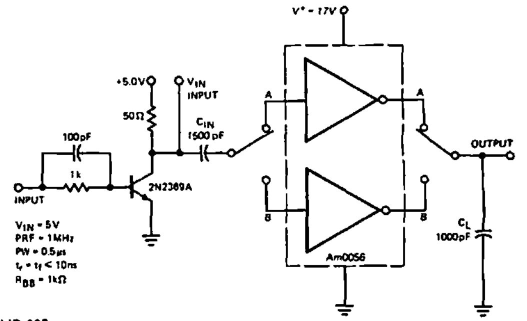
5

SWITCHING TIME WAVEFORMS



LIC-604

AC TEST CIRCUIT



LIC-605

APPLICATION INFORMATION

POWER DISSIPATION

The total average power dissipation of the Am0026 is the sum of the DC power and AC transient power. This total must be less than the given package power rating.

$$P_{DISS} = P_{AC} + P_{DC} \leq P_{MAX}.$$

With the device dissipating only 2 mW when the output is at a HIGH voltage (MOS logic "0"), the dominant factor in average DC power is the duty cycle or fraction of the time the output is at a LOW voltage level (MOS logic "1"). For the shift register driving where the duty cycle is less than 25%, P_{DC} is usually negligible. For RAM address line driver applications P_{DC} dominates since duty cycle can exceed 50%.

DC Power per driver:

DC power is given by,

$$P_{DC} = (V^+ - V^-) \times I_{S(LOW)} \times \text{Duty Cycle}$$

where $I_{S(LOW)}$ is $I_{SUPPLY(ON)}$ at $(V^+ - V^-)$

$$I_{SUPPLY(ON)} \text{ is } 40\,\text{mA} \times \frac{(V^+ - V^-)}{20\,V} \text{ worst case}$$

$$\text{or } 30\,\text{mA} \times \frac{(V^+ - V^-)}{20\,V} \text{ typically}$$

AC transient power per driver:

AC transient power is given by,

$$P_{AC} = (V^+ - V^-)^2 \times C_L \cdot x\, f \times 10^{-3} \text{ in mW}$$

where f = frequency of operation in MHz and C_L = load capacitance including all strays and wiring in pF.

PACKAGE SELECTION

Power ratings are based on a maximum junction rating of 175°C. The following guidelines are suggested for package selection. Graphs shown in the Performance Curves illustrate derating for various operating temperatures.

TO-5 ("H") Package: Rated at 600 mW in still air (derate at 4.0 mW/°C above 25°C) and rated at 900 mW with clip-on heat sink (derate at 6.0 mW/°C above 25°C). This popular hermetic package is recommended for small systems. Low cost (about 10¢) clip-on-heat sink increases driving power dissipation capability by 50%.

8-pin ("N") Molded Mini-DIP: Rated at 600 mW still air (derate at 4.0 mW/°C above 25°C) and rated at 1.0 watt soldered to PC board (derate at 6.6 mW/°C). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600 mW when mounted in a socket and not one watt until it is soldered down.)

$$C_L\,(\text{max.}) = \frac{10^3}{n}\,\frac{(P_{max.}\,Req - 10^3 n\,(V^+ - V^-)^2\,\text{Duty Cycle})}{Req\,(V^+ - V^-)^2 \times f}$$

where n is the number of drivers used in the package.

$P_{max.}$ is the package power rating in milliwatts for given package, heat sink, and maximum ambient temperature.

Req is the equivalent resistance $(V^+ - V^-)/I_{S(LOW)} = 500\Omega$ (worst case over temperature or 600 Ω (typically).

Duty cycle is the fraction of the time that the output signal is in the LOW state.

f is the input signal frequency in MHz.

$C_{L(max.)}$ is the maximum load capacitance per driver in picofarads which can be driven without exceeding device power limits.

When used as a non-overlapping two phase driver with each side operating at the same frequency and duty cycle, and with $(V^+ - V^-)$ -17 V, the above equation simplifies to

$$C_L = \frac{10^3}{f}\left[\frac{P_{max.}}{578} - \text{Duty Cycle}\right]$$

Table I gives maximum drive capability for various system conditions using the above equation.

PULSE WIDTH CONTROL

The Am0026 is intended for applications in which the input pulse width sets the output pulse width; i.e., the output pulse width is logically controlled by the input pulse. The output pulse width is given by:

$$(PW)_{OUT} = (PW)_{IN} + t_f = PW_{IN} + 25\,\text{ns}$$

Two external input coupling capacitors are required to perform the level translation between TTL/DTL and MOS logic levels. Selection of the capacitor size is determined by the desired output pulse width. Minimum delay and optimum performance is attained when the voltage at the input of the Am0026 discharges to just above the devices threshold (about 1.5 V). If the input is allowed to discharge below the threshold, t_r and t_f will be degraded. The graph in the Performance Curves shows optimum values for C_{IN} versus desired output pulse width. The value for C_{IN} may be roughly predicted by:

$$C_{IN} = (2 \times 10^{-3})\ (PW)_{OUT}$$

For an output pulse width of 500 ns, the optimum value for C_{IN} is:

$$C_{IN} = (2 \times 10^{-3})\ (500 \times 10^{-9}) = 1000\,\text{pF}$$

RISE AND FALL TIME CONSIDERATIONS (Note 3)

The Am0026's peak output current is limited to 1.5 A. The peak current limitation restricts the maximum load capacitance which the device is capable of driving and is given by:

$$I = C_L \frac{dv}{dt} \leqslant 1.5\,A$$

The rise time, t_r, for various loads may be predicted by:

$$t_r = (\Delta V) \quad (250 \times 10^{-12} + C_L)$$

Where: ΔV = the change in voltage across C_L

$$\cong V^+ - V^-$$

C_L = The load capacitance

for $V^+ - V^- = 20V$, $C_L = 1000pF$, t_r is:

$$t_r \cong (20\,V) \quad (250 \times 10^{-12} + 1000 \times 10^{-12})$$

$$= 25\,ns$$

For small values of C_L, the equation above predicts optimistic values for t_r. The graph in the performance curves shows typical rise times for various load capacitances.

The output fall time (see Graph) may be predicted by:

$$t_f \cong 2.2\,R\left(C_S + \frac{C_L}{h_{FE} + 1}\right)$$

CLOCK OVERSHOOT

The output waveform of the Am0026 can overshoot. The overshoot is due to finite inductance of the clock lines. It occurs on the negative going edge when Q_7 saturates, and on the positive edge when Q_3 turns OFF as the output goes through $V^+ - V_{be}$. The problem can be eliminated by placing a small series resistor in the output of the Am0026. The critical valve for $R_S = 2\sqrt{L/C_L}$ where L is the self-inductance of the clock line. In practice, determination of a value for L is rather difficult. However, R_S is readily determined emperically, and values typically range between 10 and 51Ω. R_S does reduce rise and fall times as given by:

$$t_r = t_r \cong 2.2 R_S\, C_L$$

CLOCK LINE CROSS TALK

At the system level, voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice-versa) during the transition of ϕ_1 to MOS logic "1". The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Transistors Q_3 and Q_4 on the ϕ_2 side of the Am0026 are essentially "OFF" when ϕ_2 is in the MOS logic "0" state since only micro-amperes are drawn from the device. When the spike is coupled to ϕ_2, the output has to drop at least $2\,V_{BE}$ before Q_3 and Q_4 come on and pull the output back to V^+. A simple method for eliminating or minimizing this effect is to add bleed resistors between the Am0026 outputs and ground causing a current of a few milliamps to flow in Q_4. When a spike is coupled to the clock line Q_4 is already "ON" with a finite h_{fe}. The spike is quickly clamped by Q_4. Values for R depend on layout and the number of registers being driven and vary typically between 2 k and 10 kΩ.

POWER SUPPLY DECOUPLING

Adequate power supply decoupling is necessary for satisfactory operation. Decoupling of V^+ to V^- supply lines with at least 0.1 μF noninductive capacitors as close as possible to each Am0026 is strongly recommended. This decoupling is necessary because otherwise 1.5 ampere currents flow during logic transition in order to rapidly charge clock lines.

5

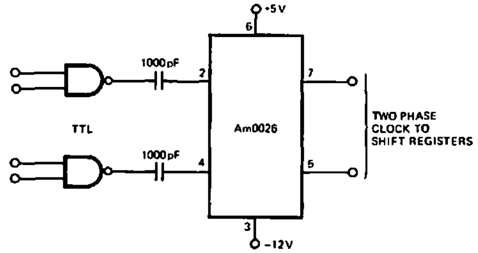
TABLE I – WORST CASE MAXIMUM DRIVE CAPABILITY FOR Am0026*

Package Type		TO-8 with Heat Sink		TO-8 Free Air		Mini-DIP Soldered Down		TO-5 and Mini-DIP Free Air		14-Pin DIP Soldered Down
Max. Operating Frequency	Duty Cycle \ Max. Ambient Temp.	60°C	85°C	60°C	85°C	60°C	85°C	60°C	85°C	70°C
100kHz	5%	30k	24k	19k	15k	13k	10k	7.5k	5.1k	11k
500kHz	10%	6.5k	5.1k	4.1k	3.2k	2.5k	1.9k	1.4k	1.1k	2k
1MHz	20%	2.9k	2.2k	1.8k	1.4k	1.1k	840	600	420	860
2MHz	25%	1.4k	1.1k	850	650	540	400	280	190	390
5MHz	25%	620	470	380	290	220	160	110	75	165
10MHz	25%	280	220	170	130	110	79	55	37	90

*Note: Values in pF and assume both sides in use as non-overlapping 2 phase driver; each side operating at same frequency and duty cycle with $(V^+ - V^-) = 17\,V$.

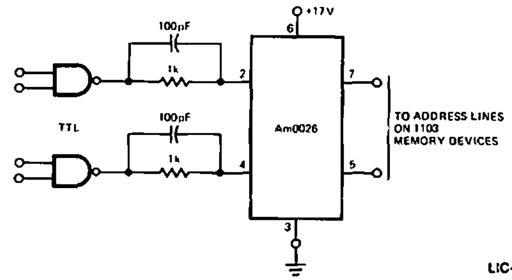
TYPICAL APPLICATIONS

AC Coupled MOS Clock Driver



LIC-606

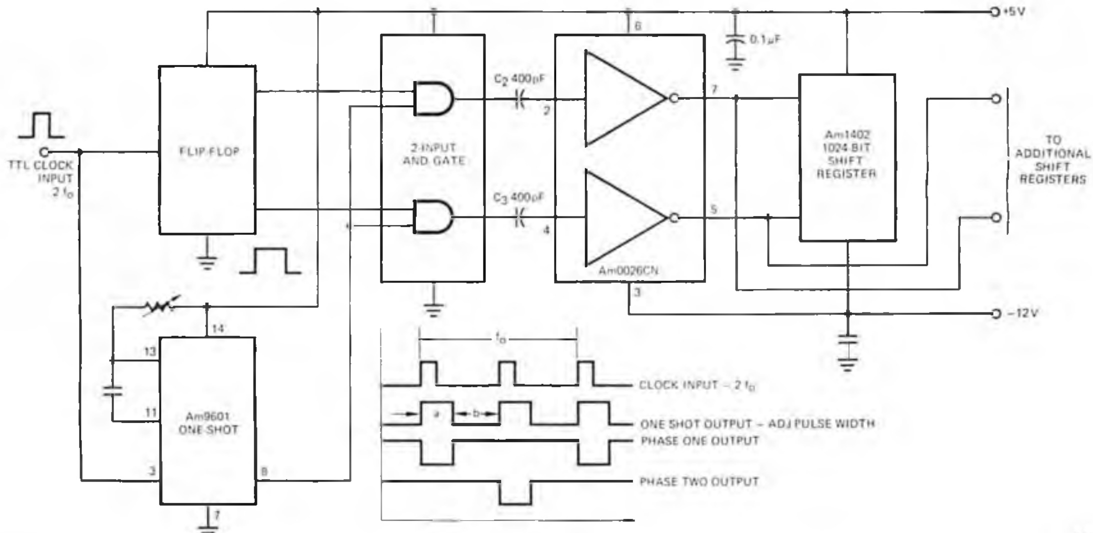
DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)



LIC-607

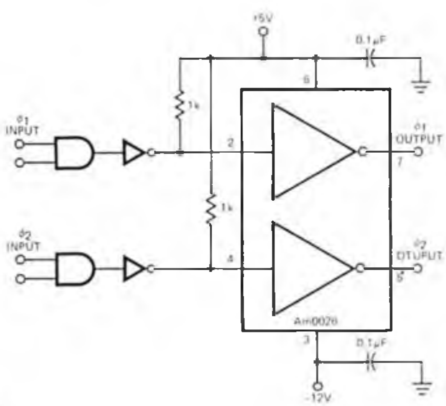
TYPICAL APPLICATIONS (Cont.)

Logically Controlled AC Coupled Clock Driver



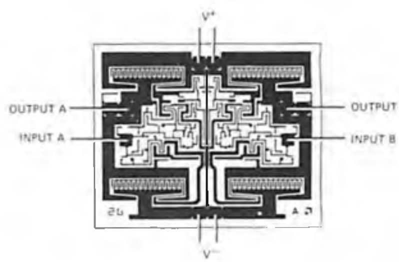
LIC-608

DC Coupled MOS Clock Driver



LIC-609

Metallization and Pad Layout



DIE SIZE 0.063" X 0.078"

Am0056 • Am0056C

5MHz Two-Phase MOS Clock Driver

5

Distinctive Characteristics

- 20ns rise and fall times with 1000pF load
- 20V output voltage swing
- ±1.5 amps outnut current drive
- High speed 5 to 10MHz depending on load
- 100% reliability assurance testing in compliance with MIL-STD-883
- Improved V_{OH} compared with Am0026

FUNCTIONAL DESCRIPTION

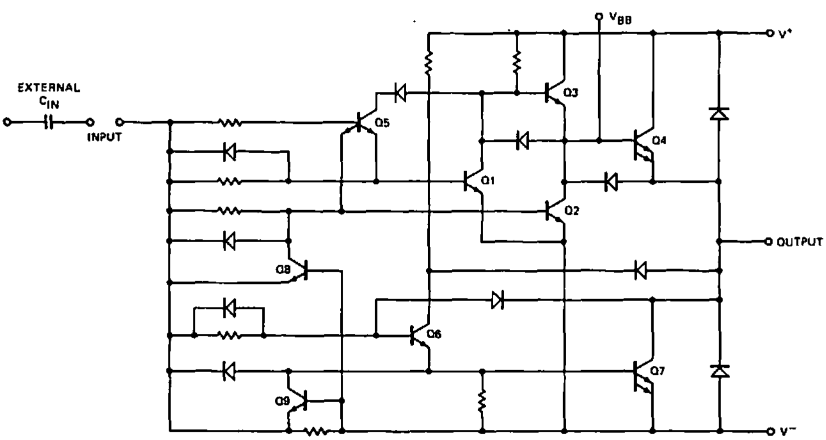
The Am0056 is a dual high speed MOS clock driver and interface circuit. The device is particularly suitable for driving two phase MOS circuits and can provide high speed operation even when driving into high capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. The output pulse width of the device is determined by the input pulse width.

The Am0056 can operate with a variety of MOS circuits. A popular application is a two-phase clock timer for driving long silicon gate shift registers such as the Am1402/3/4 series. A single clock driver is able to drive 10k bits at 5MHz. The device can also be used with standard dynamic MOS RAMS such as the 1103 to provide address and precharge drive for memories up to 8k by 16-bits.

The device is available in a TO-99, one watt copper lead frame 8-pin mini-DIP, a one and one-half watt TO-8 package, and a ceramic DIP.

The V_{BB} terminal is intended to be connected through a series resistor to a supply higher than V^+. This connection will enable the output to pull-up to V^+–0.1V. Under no conditions should the V_{BB} terminal be connected directly to a positive supply as the device will be damaged when the driver switches LOW.

SCHEMATIC DIAGRAM (One Driver Shown)



LIC-610

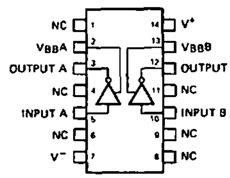
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
TO-99	0°C to 70°C	DS0056CH
Mini-DIP	0°C to 70°C	DS0056CN
Ceramic DIP	0°C to 70°C	DS0056CJ
Dice	0°C to 70°C	AM0056XC
TO-99	–55°C to +125°C	DS0056H
Ceramic DIP	–55°C to +125°C	DS0056J
Dice	–55°C to +125°C	AM0056XM

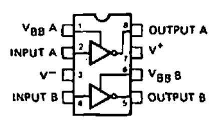
CONNECTION DIAGRAMS

Top Views

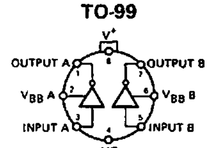
Ceramic DIP



Mini DIP



TO-99



LIC-611

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
$V^+ - V^-$ Differential Voltage	22V
Input Current	100mA
Input Voltage ($V_{IN} - V^-$)	5.5V
Peak Output Current	1.5A
Power Dissipation	See curves
V_{BB} Voltage	V^+ +5.0V
Current Into V_{BB}	50mA
Operating Temperature–Am0056	−55°C to +125°C
Am0056C	0°C to 70°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Logical "0" Output Voltage)	$V_{IN} - V^- = 0.4V$, V_{BB} Open Circuit ($R_{BB} = \infty$)	$V^+ -2.5$	$V^+ -1.4$		Volts
		$V_{IN} - V^- = 0.4V$, $R_{BB} = 1k\Omega$; V_{BB} $V_B \geq V^+ +1.0V$	$V^+ -0.3$	$V^+ -0.1$		
V_{OL}	Output LOW Voltage (Logical "1" Output Voltage)	$V_{IN} - V^- = 2.4V$		$V^- +0.7$	$V^- +1.0$	Volts
V_{IH}	Input HIGH Level	$V_{OUT} = V^- +1.0V$	2.0	1.5		Volts
V_{IL}	Input LOW Level	$V_{OUT} = V^+ -1.0V$		0.6	0.4	Volts
I_{IL}	Input LOW Current	$V_{IN} - V^- = 0V$, $V_{OUT} = V^+ -1.0V$		−0.005	−10	μA
I_{IH}	Input HIGH Current	$V_{IN} - V^- = 2.4V$, $V_{OUT} = V^- +1.0V$		10	15	mA
$I_{CC\,ON}$	"ON" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.4V$		15	30	mA
$I_{CC\,OFF}$	"OFF" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0.0V$ — COM'L		10	100	μA
		$V^+ - V^- = 20V$, $V_{IN} - V^- = 0.0V$ — MIL		50	500	
I_{BB}	"ON" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.4V$, $V_{BB} = V^+ +3.0V$, $R_{BB} = 1k\Omega$		22		mA

Notes: 1. These specifications apply for $V^+ - V^- = 10V$ to $20V$, $C_L = 1000pF$, over the temperature range −55°C to +125°C for the Am0056 and 0°C to +70°C for the Am0056C.
2. All typical values for $T_A = 25°C$.

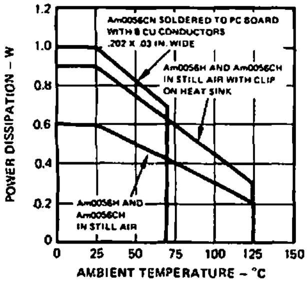
SWITCHING CHARACTERISTICS (Notes 1 and 2 Above)

Parameters	Description	Test Conditions		Min.	Typ.	Max.	Units
t_{PHL}	Turn ON Delay			5.0	8.0	12	ns
t_{PLH}	Turn OFF Delay			5.0	12	15	ns
t_r	Rise Time (Note 3)	$V^+ - V^- = 17V$,	$C_L = 500pF$		15	18	ns
			$C_L = 1000pF$		20	35	
t_f	Fall Time (Note 3)	$V^+ - V^- = 17V$,	$C_L = 500pF$		12	16	ns
			$C_L = 1000pF$		17	25	

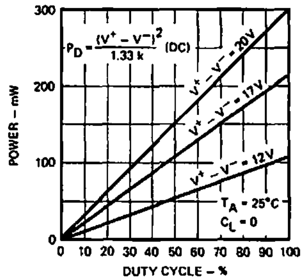
Note: 3. Rise and fall times are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall. See switching time waveforms.

TYPICAL PERFORMANCE CURVES

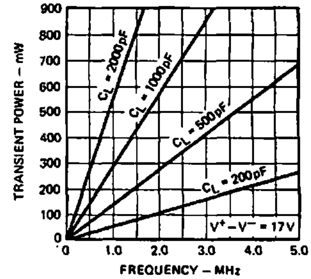
Power Ratings TO-5 & 8-Pin DIP



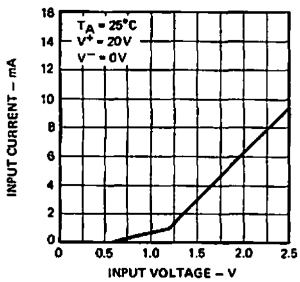
DC Power (P_{DC}) Versus Duty Cycle (DC)



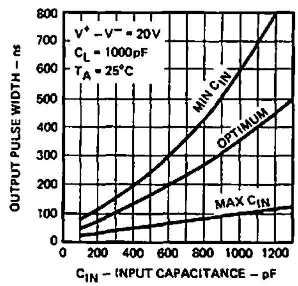
Transient Power (P_{AC}) Versus Frequency



Input Current Versus Input Voltage

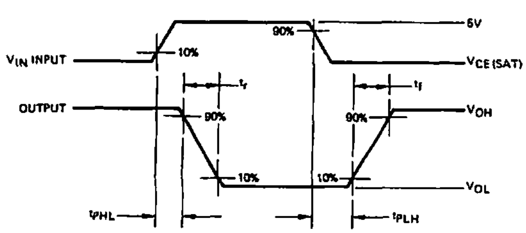


Optimum Input Capacitance Versus Output Pulse Width



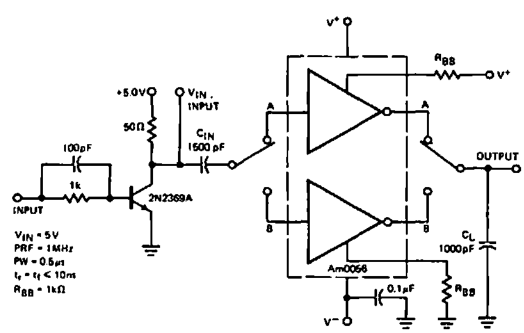
LIC-612

SWITCHING TIME WAVEFORMS



LIC-613

AC TEST CIRCUIT



LIC-614

APPLICATION INFORMATION

POWER DISSIPATION

The total average power dissipation of the Am0056 is the sum of the DC power and AC transient power. This total must be less than the given package power rating.

$$P_{DISS} = P_{AC} + P_{DC} \leqslant P_{MAX}.$$

With the device dissipating only 10 mW when the output is at a HIGH voltage (MOS logic "0"), the dominant factor in average DC power is the duty cycle or fraction of the time the output is at a LOW voltage level (MOS logic "1"). For the shift register driving where the duty cycle is less than 25%, P_{DC} is usually negligible. For RAM address line driver applications P_{DC} dominates since duty cycle can exceed 50%.

DC Power per Driver

DC power is given by,

$$P_{DC} = (V^+ - V^-) \times I_{S\,(LOW)} \times \text{Duty Cycle}$$

where $I_{S\,(LOW)}$ is $I_{SUPPLY(ON)}$ at $(V^+ - V^-)$

$$I_{SUPPLY(ON)} \text{ is } 30\text{mA} \times \frac{(V^+ - V^-)}{20\,V} \text{ worst case}$$

$$\text{or } 15\text{mA} \times \frac{(V^+ - V^-)}{20\,V} \text{ typically}$$

AC Transient Power per Driver

AC transient power is given by,

$$P_{AC} = (V^+ - V^-)^2 \times C_L \times f \times 10^{-3} \text{ in mW}$$

where f = frequency of operation in MHz and C_L = load capacitance including all strays and wiring in pF.

PACKAGE SELECTION

Power ratings are based on a maximum junction rating of 175°C. The following guidelines are suggested for package selection. Graphs shown in the Performance Curves illustrate derating for various operating temperatures.

TO-99 ("H") Package: Rated at 600 mW in still air (derate at 4.0 mW/°C above 25°C) and rated at 900 mW with clip-on heat sink (derate at 6.0 mW/°C above 25°C). This popular hermetic package is recommended for small systems. Low cost (about 10¢) clip-on-heat sink increases driving power dissipation capability by 50%.

8-pin ("N") Molded Mini-DIP: Rated at 600 mW still air (derate at 4.0 mW/°C above 25°C) and rated at 1.0 watt soldered to PC board (derate at 6.6 mW/°C). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600 mW when mounted in a socket and not one watt until it is soldered down.)

TO-8 ("G") Package: Rated at 1.5 watts still air (derate at 10mW/°C above 25°C) and 2.3 watts with clip on heat sink (Wakefield type 215-1.9 or equivalent – derate at 15mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

MAXIMUM LOAD CONSIDERATIONS

The maximum capacitive load that the Am0056 can drive is determined by:

The AC power consumed $= nVs^2\ C_L f \times 10^{-3}$ mW

The DC power consumed $= \dfrac{nVs^2}{Req}\ \rho \times 10^3$ mW

The package power rating for a given package, heatsink, and maximum ambient temperature = Pmax mW

Combining these expressions:

$$Pmax = \frac{nVs^2\ \rho \times 10^3}{Req} + nVs^2\, C_L f \times 10^{-3}$$

from which the maximum capacitive load:

$$C_{L(max)} = \frac{10^3}{n} \cdot \frac{(Pmax\ Req - nVs^2\rho \times 10^3)}{Vs^2 f\ Req}$$

Where n = number of drivers employed in the package
Vs = total supply voltage $(V^+ - V^-)$ across device
ρ = duty cycle = time in output LOW state/ time in output LOW + time in output HIGH

Req = $(V^+ - V^-)/I_{CC}$ ON = 1000 Ω worst case or 1300 Ω TYP

C_L = load capacitance per driver in pF

f = input signal frequency in MHz

When used as a non-overlapping, two-phase driver with each side operating at the same frequency and duty cycle and with V_s = 17 V, the above equation reduces to:

$$C_{L(max)} = \frac{10^3}{f}\left(\frac{Pmax}{578} - \rho\right)$$

Table 1 gives maximum drive capability using above equation.

PULSE WIDTH CONTROL

The Am0056 is intended for applications in which the input pulse width sets the output pulse width; i.e., the output pulse width is logically controlled by the input pulse. The output pulse width is given by:

$$(PW)_{OUT} = (PW)_{IN} + t_f = PW_{IN} + 17\,\text{ns}$$

Two external input coupling capacitors are required to perform the level translation between TTL/DTL and MOS logic levels. Selection of the capacitor size is determined by the desired output pulse width. Minimum delay and optimum performance is attained when the voltage at the input of the Am0056 discharges to just above the devices threshold (about 1.5 V). If the input is allowed to discharge below the threshold, t_r and t_f will be degraded. The graph in the Performance Curves shows optimum values for C_{IN} versus desired output pulse width. The value for C_{IN} may be roughly predicted by:

$$C_{IN}\ (3 \times 10^{-3})\ (PW)_{OUT}$$

For an output pulse width of 500 ns, the optimum value for C_{IN} is:

$$C_{IN} = (3 \times 10^{-3})\ (500 \times 10^{-9}) = 1500\text{pF}$$

RISE AND FALL TIME CONSIDERATIONS (Note 3)

The Am0056's peak output current is limited to 1.5 A. The peak current limitation restricts the maximum load capacitance which the device is capable of driving and is given by:

$$I = C_L \frac{dv}{dt} \leqslant 1.5\,A$$

The rise time, t_r, for various loads may be predicted by:

$$t_r = (\Delta V) \quad (250 \times 10^{-12} + C_L)$$

Where: ΔV = the change in voltage across C_L

$$\cong V^+ - V^-$$

C_L = The load capacitance

for $V^+ - V^- = 20V$, $C_L = 1000pF$, t_r is:

$$t_r \cong (20\,V) \quad (250 \times 10^{-12} + 1000 \times 10^{-12})$$
$$= 25\,ns$$

For small values of C_L, the equation above predicts optimistic values for t_r.

The output fall time may be predicted by:

$$t_f \cong 2.2\,R\left(C_S + \frac{C_L}{h_{FE}+1}\right)$$

CLOCK OVERSHOOT

The output waveform of the Am0056 can overshoot. The overshoot is due to finite inductance of the clock lines. It occurs on the negative going edge when Q_7 saturates, and on the positive edge when Q_3 turns OFF as the output goes through $V^+ - V_{be}$. The problem can be eliminated by placing a small series resistor in the output of the Am0056. The critical value for $R_S = 2\sqrt{L/C_L}$ where L is the self-inductance of the clock line. In practice, determination of a value for L is rather difficult. However, R_S is readily determined emperically, and values typically range between 10 and 51Ω. R_S does reduce rise and fall times as given by:

$$t_r = t_f \cong 2.2 R_S\, C_L$$

CLOCK LINE CROSS TALK

At the system level, voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice-versa) during the transition of ϕ_1 to MOS logic "1". The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Transistors Q_3 and Q_4 on the ϕ_2 side of the Am0056 are essentially "OFF" when ϕ_2 is in the MOS logic "0" state since only micro-amperes are drawn from the device. When the spike is coupled to ϕ_2, the output will drop until Q_4 becomes active. A simple method for eliminating or minimizing this effect is to add bleed resistors between the Am0056 outputs and ground causing a current of a few milliamps to flow in Q_4. When a spike is coupled to the clock line Q_4 is already "ON" with a finite h_{fe}. The spike is quickly clamped by Q_4. Values for R depend on layout and the number of registers being driven and vary typically between 2k and 10kΩ.

POWER SUPPLY DECOUPLING

Adequate power supply decoupling is necessary for satisfactory operation. Decoupling of V^+ and V^- supply lines with at least 0.1 µF noninductive capacitors as close as possible to each Am0056 is strongly recommended. This decoupling is necessary because of the 1.5 ampere currents which flow during logic transition when charging clock lines.

5

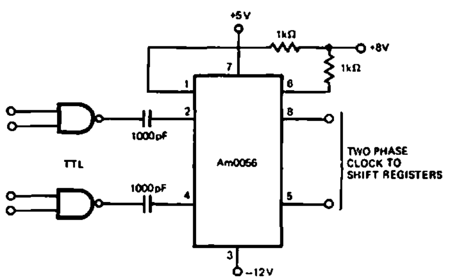
TABLE I – WORST CASE MAXIMUM DRIVE CAPABILITY FOR Am0056*

Package Type			TO-8 with Heat Sink		TO-8 Free Air		Mini-DIP Soldered Down		TO-5 and Mini-DIP Free Air		14-Pin DIP Soldered Down
Max. Operating Frequency	Duty Cycle	P_{Max} mW	1775	1400	1150	900	769	604	460	360	665
		Ambient Temp.	60°C	85°C	60°C	85°C	60°C	85°C	60°C	85°C	70°C
100kHz	5%		30k	24k	19k	15k	13k	10k	7.5k	5.1k	11k
500kHz	10%		6.0k	4.6k	3.8k	2.9k	2.5k	1.9k	1.4k	1.0k	2k
1MHz	20%		2.9k	2.2k	1.8k	1.4k	1.1k	840	600	420	860
2MHz	25%		1.4k	1.1k	870	650	540	400	270	190	390
5MHz	25%		560	440	350	260	220	160	110	75	165
10MHz	25%		280	220	170	130	110	80	55	37	90

*Note: Values in pF and assume both sides in use as non-overlapping 2 phase driver; each side operating at same frequency and duty cycle with $(V^+ - V^-) = 17V$.

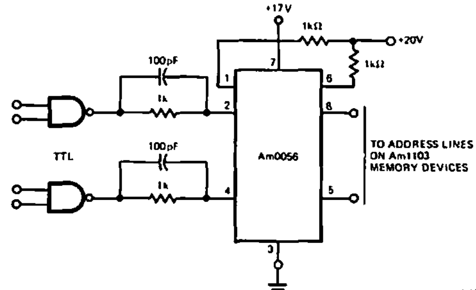
TYPICAL APPLICATIONS

AC Coupled MOS Clock Driver



LIC-615

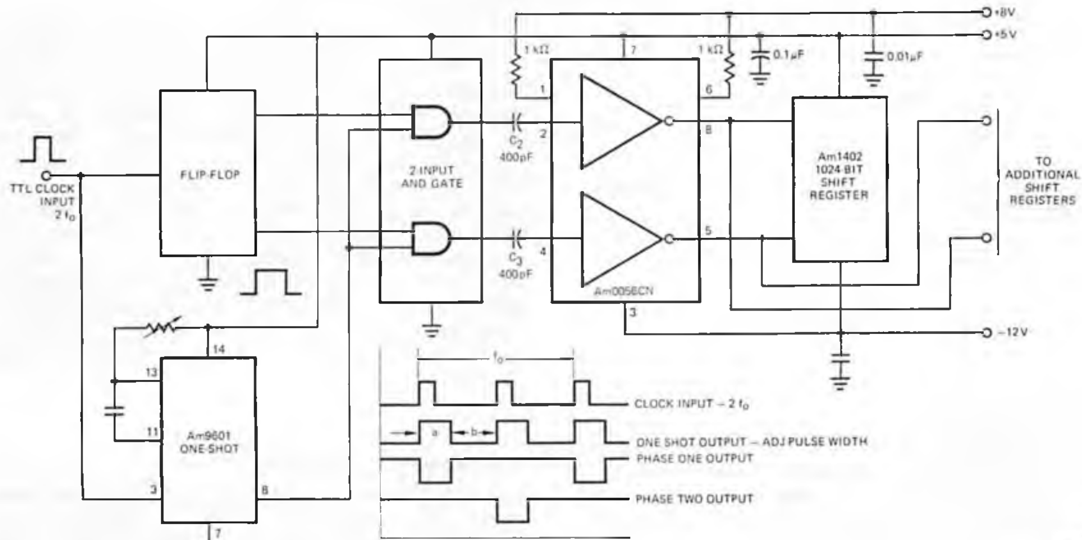
DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)



LIC-616

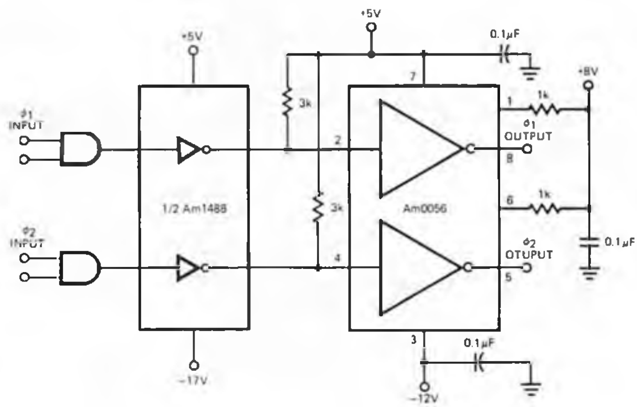
TYPICAL APPLICATIONS (Cont.)

Logically Controlled AC Coupled Clock Driver



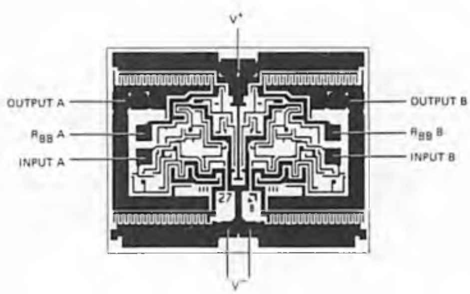
LIC-617

DC Coupled MOS Clock Driver



LIC-618

Metallization and Pad Layout



DIE SIZE 0.056" X 0.074"

Am8224

Clock Generator and Driver for 8080A Compatible Microprocessors

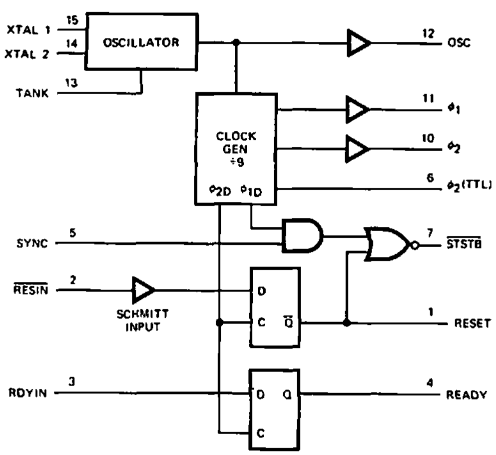
Distinctive Characteristics

- Single chip clock generator/driver for 8080A compatible CPU
- Power-up reset for CPU
- Ready synchronizing flip-flop
- Status strobe signal
- *Oscillator* output for external system timing
- Am8224-4 version available for use with 1µsec instruction cycle of Am9080A-4
- Available for operation over both commercial and military temperature ranges
- Crystal controlled for stable system operation
- Reduces system package count
- Advanced Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am8224 is a single chip Clock Generator/Driver for the Am9080A and 8080A CPU. It contains a crystal-controlled oscillator, a "divide by nine" counter, two high-level drivers and several auxiliary logic functions, including a power-up reset, status strobe and synchronization of ready. Also provided are TTL compatible oscillator and ϕ_2 outputs for external system timing. The Am8224 provides the designer with a significant reduction of packages used to generate clocks and timing for the Am9080A or 8080A for both commercial and military temperature range applications. A high speed version, the Am8224-4, is available for use with the high speed Am9080A-4.

LOGIC DIAGRAM



LIC-619

ORDERING INFORMATION

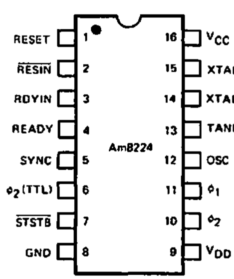
Package Type	Temperature Range	Order Number
Hermetic DIP	–55°C to +125°C	AM8224DM
Hermetic DIP	0°C to +70°C	D8224
Molded DIP	0°C to +70°C	AM8224PC
Dice	0°C to +70°C	AM8224XC
Hermetic DIP	0°C to +70°C	AM8224-4DC*

*For use with Am9080A-4 with clock period between 250ns and 320ns.

PIN DEFINITION

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	CONNECTIONS FOR CRYSTAL
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
ϕ_2(TTL)	ϕ_2 CLK (TTL LEVEL)
V_{CC}	+5.0V
V_{DD}	+12V
GND	0V
$\overline{\text{RESIN}}$	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
$\overline{\text{STSTB}}$	STATUS STB (ACTIVE LOW)
ϕ_1	Am9080A/8080A CLOCKS
ϕ_2	Am9080A/8080A CLOCKS

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation. LIC-620

5

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential	
V_{CC}	7.5V
V_{DD}	15V
Maximum Output Current ϕ_1 and ϕ_2 (Note 1)	100mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am8224XC, Am8224-4XC (COM'L)	T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	V_{DD} = 12V ± 5%
Am8224XC (MIL)	T_A = –55°C to +125°C	V_{CC} = 5.0V ± 10%	V_{DD} = 12V ± 10%

Parameters	Description	Test Conditions		Min.	Typ. (Note 2)	Max.	Units
I_F	Input Current Loading	V_F = 0.45V				–0.25	mA
I_R	Input Leakage Current	V_R = 5.25V				10	μA
V_C	Input Forward Clamp Voltage	I_C = –5.0mA	COM'L			–1.0	Volts
			MIL			–1.2	
V_{IL}	Input LOW Voltage	V_{CC} = 5.0V				0.8	Volts
V_{IH}	Input HIGH Voltage	Reset input	COM'L	2.6	2.2		Volts
			MIL	2.8	2.2		
		All other inputs		2.0			
V_{IH}-V_{IL}	$\overline{RESIN}$ Input Hysteresis	V_{CC} = 5.0V		0.25	0.5		Volts
V_{OL}	Output LOW Voltage	(ϕ_1, ϕ_2), Ready, Reset, $\overline{STSTB}$ I_{OL} = 2.5mA				0.45	Volts
		All other inputs I_{OL} = 15mA				0.45	
V_{OH}	Output HIGH Voltage	ϕ_1, ϕ_2: I_{OH} = –100μA	COM'L	9.4	11		Volts
			MIL	V_{DD} –1.6V	V_{DD} –1.0V		
		READY, RESET: I_{OH} = –100μA	COM'L	3.6	4.0		
			MIL	3.35	4.0		
		All other outputs; I_{OH} = –1.0mA		2.4	3.0		
I_{SC}	Output Short Circuit Current (All Low Voltage Outputs Only)	V_O = 0V V_{CC} = 5.0V		–10		–60	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 3)			70	115	mA
I_{DD}	Power Supply Current	V_{DD} = MAX.			5.0	12	mA

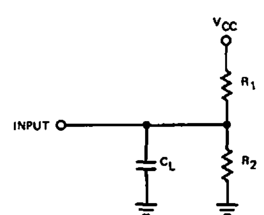
Notes: 1. Caution: ϕ_1 and ϕ_2 outputs do not have short circuit protection.
2. Typical limits are at V_{CC} = 5.0V, V_{DD} = 12V, 25°C ambient and maximum loading.
3. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

CRYSTAL REQUIREMENTS

Tolerance: .005% at 0°C - 70°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Min): 4mW

*With frequency in excess of 18MHz use 3rd overtone XTALs and tank circuit.

TEST CIRCUIT



LIC-621

AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am8224XM Min.	Am8224XM Typ.	Am8224XM Max.	Am8224XC Min.	Am8224XC Typ.	Am8224XC Max.	Am8224-4XC (Note 2) Min.	Am8224-4XC (Note 2) Typ.	Am8224-4XC (Note 2) Max.	Units
$t_{\phi 1}$	ϕ_1 Pulse Width	C_L = 20pF to 50pF	$\frac{2t_{CY}}{9}$ −23ns			$\frac{2t_{CY}}{9}$ −20ns			45			ns
$t_{\phi 2}$	ϕ_2 Pulse Width		$\frac{5t_{CY}}{9}$ −35ns			$\frac{5t_{CY}}{9}$ −35ns			110			
t_{D1}	ϕ_1 to ϕ_2 Delay		0			0			0			
t_{D2}	ϕ_2 to ϕ_1 Delay		$\frac{2t_{CY}}{9}$ −17ns			$\frac{2t_{CY}}{9}$ −14n.			35			
t_{D3}	ϕ_1 to ϕ_2 Delay		$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}$ +22ns	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}$ +20ns	55		76	
t_r	ϕ_1 and ϕ_2 Rise Time				20			20			20	
t_f	ϕ_1 and ϕ_2 Fall Time				20			20			20	
$t_{D\phi 2}$	ϕ_2 to ϕ_2(TTL) Delay	ϕ_2(TTL), C_L = 30pF, R_1 = 300Ω, R_2 = 600Ω	−5.0		15	−5.0		15	−5.0		15	ns
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\overline{STSTB}$, C_L = 15pF, R_1 = 2.0kΩ, R_2 = 4.0kΩ	$\frac{6t_{CY}}{9}$ −33ns		$\frac{6t_{CY}}{9}$	$\frac{6t_{CY}}{9}$ −30ns		$\frac{6t_{CY}}{9}$	137		167	ns
t_{PW}	$\overline{STSTB}$ Pulse Width		$\frac{t_{CY}}{9}$ −18ns			$\frac{t_{CY}}{9}$ −15ns			18			
t_{DRS}	RDYIN Set-up Time to Status Strobe		50ns − $\frac{4t_{CY}}{9}$			50ns − $\frac{4t_{CY}}{9}$			−61			
t_{DRH}	RDYIN Hold Time After STSTB		$\frac{4t_{CY}}{9}$			$\frac{4t_{CY}}{9}$			111			
t_{DR}	RDYIN or RESIN to ϕ_2 Delay	Ready and Reset C_L = 10pF, R_1 = 2.0kΩ, R_2 = 4.0kΩ	$\frac{4t_{CY}}{9}$ −25ns			$\frac{4t_{CY}}{9}$ −25ns			86			ns
t_{CLK}	CLK Period			$\frac{t_{CY}}{9}$			$\frac{t_{CY}}{9}$			28		
$f_{Max.}$	Maximum Oscillating Frequency		27			28.12			36			MHz
C_{in}	Input Capacitance	V_{CC} = 5.0V, V_{DD} = 12V, V_{BIAS} = 2.5V, f = 1.0MHz			8.0			8.0			8.0	pF

5

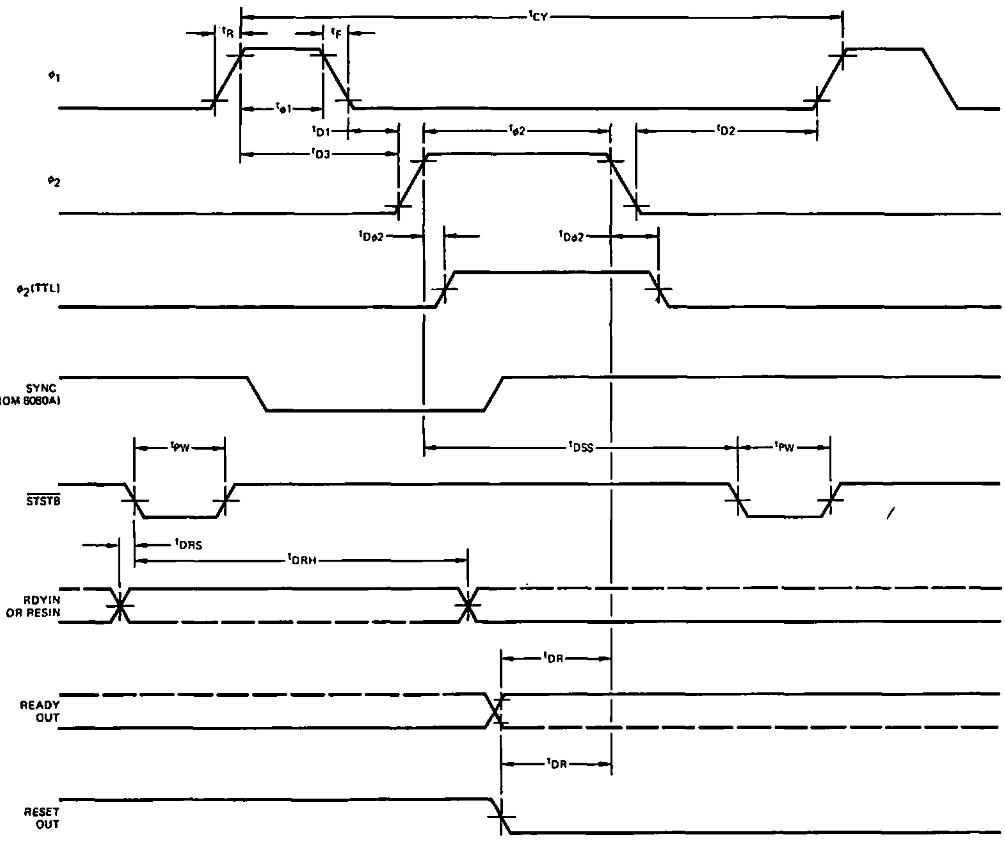
AC CHARACTERISTICS (For t_{CY} = 488.28ns)

T_A = 0°C to +70°C V_{CC} = +5.0V ±5% V_{DD} = +12V ±5%

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
$t_{\phi 1}$	ϕ_1 Pulse Width	ϕ_1 and ϕ_2 Loaded C_L = 20 to 50pF	89			ns
$t_{\phi 2}$	ϕ_2 Pulse Width		236			ns
t_{D1}	Delay ϕ_1 to ϕ_2		0			ns
t_{D2}	Delay ϕ_2 to ϕ_1		95			ns
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges		109		129	ns
t_r	Output Rise Time				20	ns
t_f	Output Fall Time				20	ns
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay		296		326	ns
$t_{D\phi 2}$	ϕ_2 to ϕ_2(TTL) Delay		−5.0		15	ns
t_{PW}	Status Strobe Pulse Width		40			ns
t_{DRS}	RDYIN Set-up Time to $\overline{STSTB}$	Ready and Reset Loaded C_L = 20 to 50pF R_1 = 2.0kΩ, R_2 = 4.0kΩ	−167			ns
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$		217			ns
t_{DR}	Ready or Reset to ϕ_2 Delay		192			ns
FREQ	Oscillator Frequency				18.432	MHz

Notes: 1. All measurements referenced to 1.5V unless specified otherwise.
2. Am8224-4 parameter limits are given for t_{CY} = 250ns or an oscillating frequency of 36MHz. Between 28.12MHz and 36MHz min. and max. limits should be ratioed between the calculated Am8224XC limits at 28.12MHz and the given 36MHz parameter limits.

SWITCHING WAVEFORMS



Voltage measurement points: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V
All other signals measured at 1.5V.

LIC-622

Oscillator

The oscillator circuit derives its basic operating frequency from an external, series resonant, fundamental mode crystal. Two inputs are provided for the crystal connections (XTAL1, XTAL2).

The selection of the external crystal frequency depends mainly on the speed at which the CPU is to be run. Basically, the oscillator operates at 9 times the desired processor speed.

The formula to determine the crystal frequency is:

$$f(XTAL) = \frac{1}{t_{CY}} \text{ times } 9$$

When using crystals above 10MHz a small amount of frequency "trimming" is necessary to produce the desired frequency. The addition of a selected capacitance (20pF – 30pF) in series with the crystal will accomplish this function.

Another input to the oscillator is TANK. This input allows the use overtone mode crystals. This type of crystal generally has a much lower output at its rated frequency and has a tendency to oscillate at its fundamental.

To avoid the unwanted oscillation and increase the desired frequency output it is necessary to provide a parallel tuned resonant circuit of low impedance. The external LC network is connected to the TANK input and is AC coupled. See typical application with Am8228 and Am9080A in Figure 2.

The formula for the LC network is:

$$F = \frac{1}{2\pi \sqrt{LC}}$$

The output of the oscillator is buffered and brought out on OSC (pin 12) so that other system timing signals can be derived from this stable, crystal-controlled source.

Clock Generator

The Clock Generator consists of a synchronous "divide by nine" counter and the associated decode gating to create the waveforms of the two clocks and auxiliary timing signals.

The waveforms generated by the decode gating follow a simple 2-5-2 digital pattern. See Figure 2. The clocks generated; ϕ_1 and ϕ_2, can best be thought of as consisting of "units" based on the oscillator frequency. Assume that one "unit" equals the period of the oscillator frequency. By multiplying the number of "units" that are contained in a pulse width or delay, times the period of the oscillator frequency, the approximate time in nanoseconds can be derived.

The outputs of the clock generator are connected to two high level drivers for direct interface to the CPU. A TTL level phase 2 is also brought out ϕ_2 (TTL) for external timing purposes. It is especially useful in DMA dependent activities. This signal is used to gate the requesting device onto the bus once the CPU issues the Hold Acknowledgement (HLDA).

Several other signals are also generated internally so that optimum timing of the auxiliary flip-flops and status strobe ($\overline{STSTB}$) is achieved.

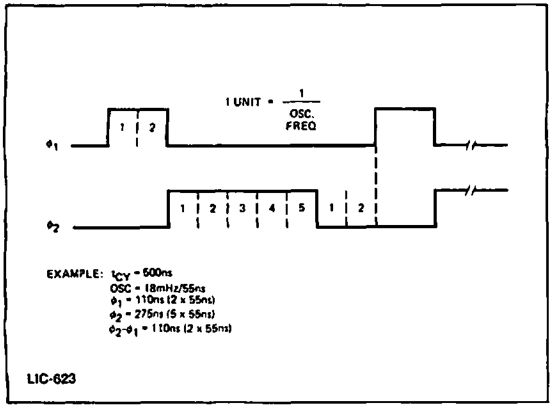


Figure 1. Clock Generator Waveforms.

$\overline{STSTB}$ (Status Strobe)

At the beginning of each machine cycle the CPU issues status information on its data bus. This information tells what type of action will take place during that machine cycle. By bringing in the SYNC signal from the CPU, and gating it with an internal timing signal (ϕ_{1A}), an active low strobe can be derived that occurs at the start of each machine cycle at the earliest possible moment that status data is stable on the bus. The $\overline{STSTB}$ signal connects directly to the Am8228 System Controller.

The power-on Reset also generates $\overline{STSTB}$, but of course, for a longer period of time. This feature allows the Am8228 to be automatically reset without additional pins devoted for this function.

Power-On Reset and Ready Flip-Flops

A common function in microcomputer systems is the generation of an automatic system reset and start-up upon initial power-on. The Am8224 has a built-in feature to accomplish this feature.

An external RC network is connected to the $\overline{RESIN}$ input. The slow transition of the power supply rise is sensed by an internal Schmitt Trigger. This circuit converts the slow transition into a clean, fast edge when its input level reaches a predetermined value. The output of the Schmitt Trigger is connected to a "D" type flip-flop that is clocked with ϕ_{2D} (an internal timing signal). The flip-flop is synchronously reset and an active high level that complies with the microprocessor input spec is generated. For manual switch type system Reset circuits, an active low switch closing can be connected to the RESIN input in addition to the power-on RC network.

The READY input to the CPU has certain timing specifications such as "set-up and hold" thus, an external synchronizing flip-flop is required. The Am8224 has this feature built-in. The RDYIN input presents the asynchronous "wait request" to the "D" type flip-flop. By clocking the flip-flop with ϕ_{2D}, a synchronized READY signal at the correct input level, can be connected directly to the CPU.

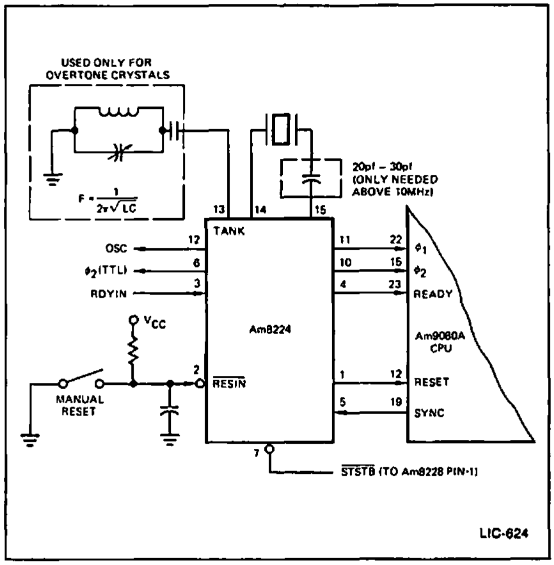


Figure 2. Typical Application with Am8224 and Am9080A.

APPLICATION PRECAUTIONS WHEN USING Am8224 UP TO 36MHz

Usage with Third Harmonic Crystal or Am9080A-4

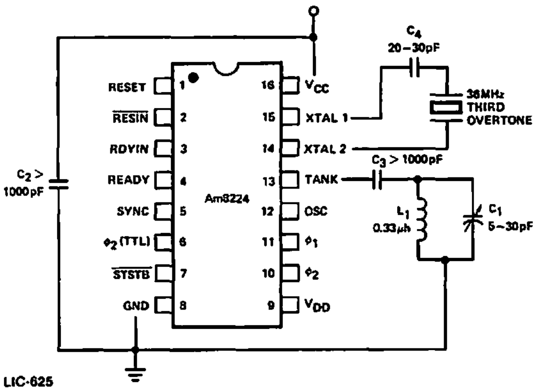
The use of the Am8224 with a third harmonic crystal requires a minor modification to the external circuitry associated with the Am8224. The changes are as follows:

- Series capacitor in conjunction with the xtal
- Adding a tuned circuit in the "tank" lead
- Tuning of circuit to proper frequency

It is necessary to maintain the crystal activity to a proper level if an xtal controlled circuit is to operate properly. A 20-30pfd capacitor placed in series will help achieve this level in third overtone crystal, while helping to suppress the fundamental mode. The Am8224 has an auxiliary port provided to allow for a tuned circuit. This tuned circuit eliminates the tendency of the circuit to oscillate at the crystal's fundamental. The tank or tuned circuit must have the following properties:

1. It must be parallel resonant at the crystal frequency (third order).
2. The off resonance impedance must be low enough to spoil the AC gain of the Am8224.
3. The circuit must be DC decoupled (or returned to V_{CC}) at a low impedance (substantially below 100Ω).

All frequency determining components must be in close proximity to the Am8224. Insert crystal and tune tank for best waveform at Pin 12 (OSC). If counter is available, adjust for match of crystal marking. The circuit in Figure 3 will accomplish the above result for the 36MHz range.



LIC-625

Figure 3.

C_1 = E.F. Johnson
275-0430-005
5-30pF Trimmer or Equiv.

L_1 = J.W. Miller Inductor
9230-08

V_{CC} Ground

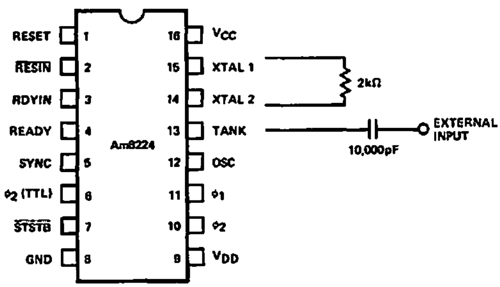
Due to the nature of our device (fast switching, higher voltage) it is necessary to provide a bypass capacitor from V_{CC} to ground in the immediate proximity of the Am8224. This insures proper operation of the device while reducing noise spiking on adjacent circuits.

Resin Bypass

The use of a high impedance capacitor for timing R-C, and/or timing components remotely located from the Am8224 device may cause a disturbance to occur during the linear transition region. The capacitor for this function should be of the ceramic type and a value of 1000pF or greater.

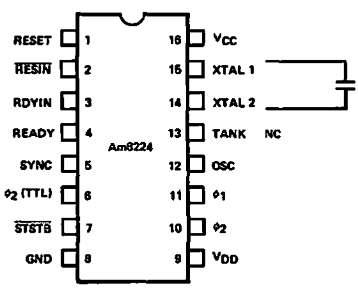
This can be cured by placing a >1000pfd ceramic capacitor from Resin (Pin 2) to Ground (Pin 8) in the immediate proximity of the device. This will allow the timing R-C to be placed at will.

APPLICATIONS



LIC-626

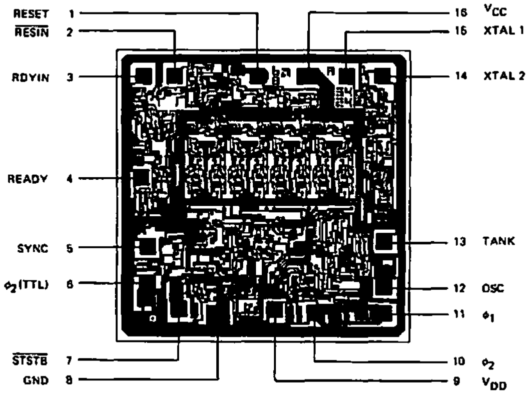
The Am8224 can be driven from an external source of frequency by connecting as shown and driven with approximately 500mV over a wide frequency range.



LIC-627

The Am8224 can oscillate without a xtal by placing a small value capacitor (10→200pF) in place of a crystal.

Metallization and Pad Layout



DIE SIZE 0.085" X 0.084"

5

Am8228 • Am8238

System Controller and Bus Driver for 8080A Compatible Microprocessors

Distinctive Characteristics

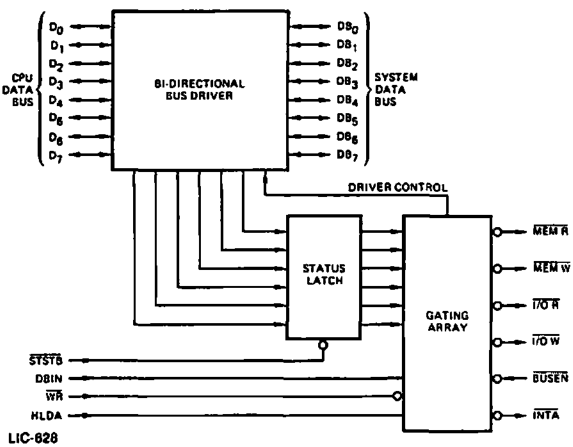
- Multi-byte instruction interrupt acknowledge
- Selectable single level vectored interrupt (RST-7)
- 28-pin molded or hermetic DIP package
- Single chip system controller and data bus driver for Am9080/8080A systems
- Am8238-4 high speed version available for use with 1μsec instruction cycle of Am9080A-4
- Bi-directional three-state bus driver for CPU independent operation
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- Available in military and commercial temperature range
- Am8238 has extended $\overline{\text{IOW}}/\overline{\text{MEMW}}$ pulse width

FUNCTIONAL DESCRIPTION

The Am8228 and Am8238 are single chip System Controller Data Bus drivers for the Am9080A Microcomputer System. They generate all control signals required to directly interface Am9080A/8080A compatible system circuits (memory and I/O) to the CPU.

Bi-directional bus drivers with three-state outputs are provided for the system data bus, facilitating CPU independent bus operations such as direct memory access. Interrupt processing is accommodated by means of a single vectored interrupt or by means of the standard 8080A multiple byte interrupt vector operation.

LOGIC DIAGRAM



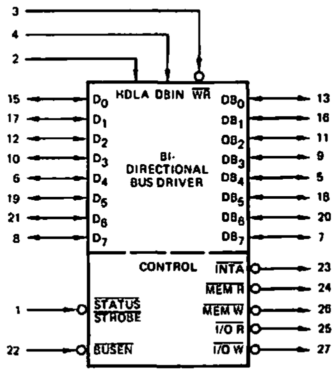
LIC-628

ORDERING INFORMATION

Package Type	Temperature Range	Am8228 Order Number	Am8238 Order Number
Molded DIP	0°C to +70°C	AM8228PC	AM8238PC
Hermetic DIP	0°C to +70°C	D8228	D8238
Hermetic DIP	−55°C to +125°C	AM8228DM	AM8238DM
Dice	0°C to +70°C	AM8228XC	AM8238XC
Hermetic DIP	0°C to +70°C		AM8238-4DC*
Molded DIP	0°C to +70°C		AM8238-4PC*

*For use with Am9080A-4 with minimum clock period of 250ns.

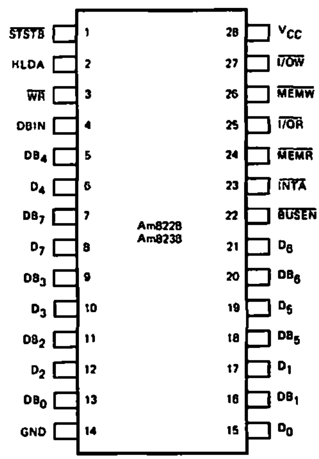
LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

LIC-629

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-630

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	$-65°C$ to $+150°C$
Temperature (Ambient) Under Bias	$-55°C$ to $+125°C$
Supply Volatge to Ground Potential (Pin 28 to Pin 14) Continuous	$-0.5V$ to $+7.0V$
DC Voltage Applied to Outputs for HIGH Output State	$-0.5V$ to $+V_{CC}$ max.
DC Input Voltage	$-1.5V$ to $+7.0V$
DC Output Current, Into Outputs	50mA
DC Input Current	$-30mA$ to $+5.0mA$

ELECTRICAL CHARACTERISTICS The Following Conditions Apply Unless Otherwise Noted:

Am8228XM, Am8238XM	$T_A = -55°C$ to $+125°C$	V_{CC}MIN. = 4.50V	V_{CC}MAX. = 5.50V
Am8228XC, Am8238XC, Am8238-4XC	$T_A = 0°C$ to $+70°C$	V_{CC}MIN. = 4.75V	V_{CC}MAX. = 5.25V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 2)				Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN.	$I_{OH} = -10\mu A$	D_0–D_7	MIL	3.35	3.8		Volts
					COM'L	3.6	3.8		
			$I_{OH} = -1.0mA$	All other outputs		2.4			
V_{OL}	Output Low Voltage	V_{CC} = MIN.	I_{OL} = 2.0mA	D_0–D_7				0.45	Volts
			I_{OL} = 10mA	All other outputs				0.45	
V_C	Input Clamp Voltage (All Inputs)	V_{CC} = MIN., $I_C = -5.0mA$					−0.75	−1.0	Volts
V_{TH}	Input Threshold Voltage (All Inputs)	V_{CC} = 5.0V				0.8		2.0	Volts
I_F	Input Load Current	V_{CC} = MAX., V_F = 0.45V		$\overline{STSTB}$				−500	μA
				D_2 and D_6				−750	
				All other inputs				−250	
I_R	Input Leakage Current	V_{CC} = MAX., V_R = 5.25V		DB_0–DB_7				20	μA
				All other inputs				100	
I_{INT}	INTA Current	See INTA test circuit						5.0	mA
$I_{O(OFF)}$	Offstate Output Current (All Control Outputs)	V_{CC} = MAX., V_O = 5.25V						100	μA
		V_O = 0.45V						−100	
I_{OS}	Short Circuit Current (All Outputs)	V_{CC} = 5.0V				−15		−90	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.					140	190	mA

5

AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

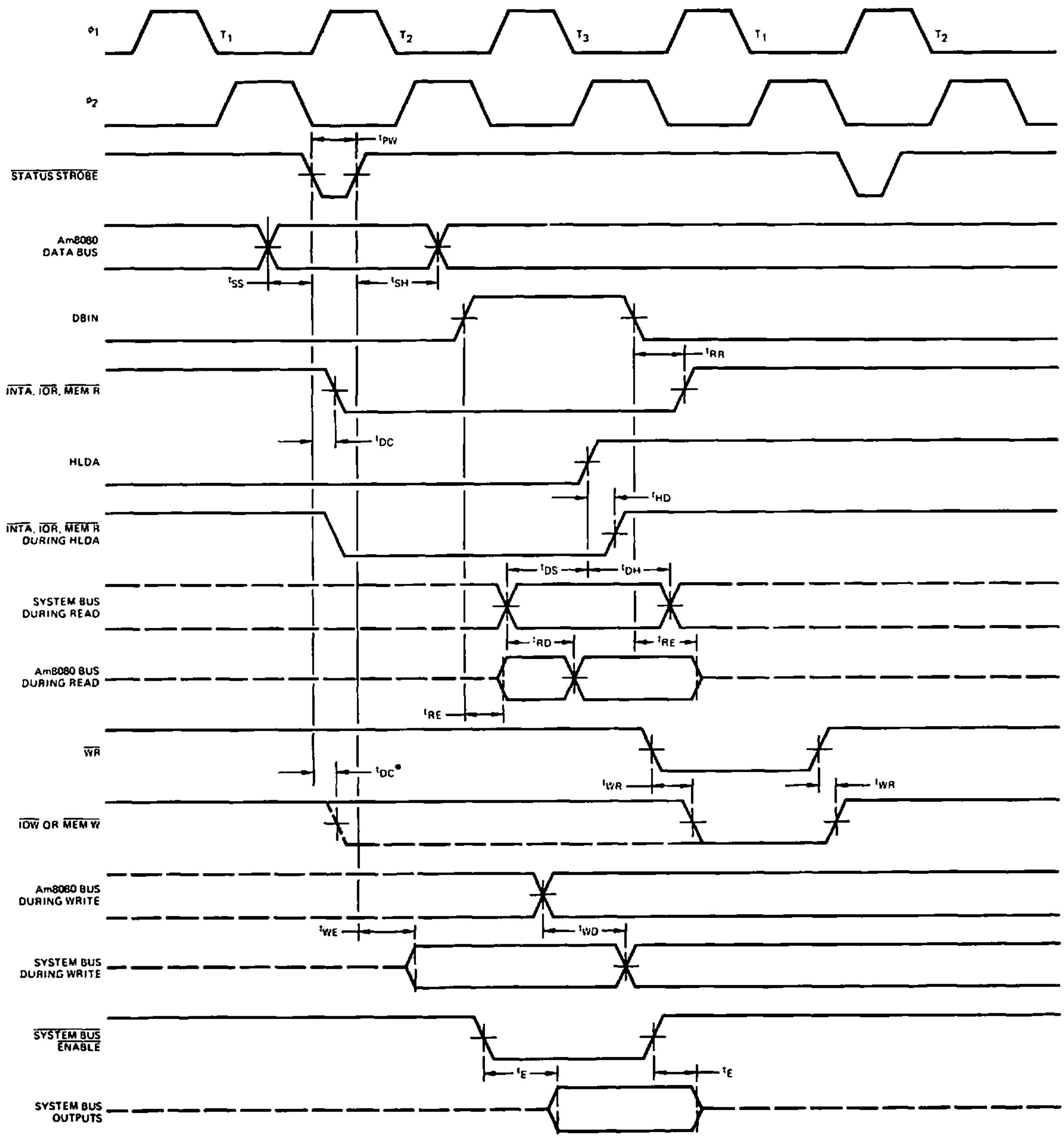
Parameters	Description		Test Conditions	Am8228XM/ Am8238XM Min.	Typ. (Note 1)	Max.	Am8228XC/ Am8238XC Min.	Typ. (Note 1)	Max.	Am8238-4XC Min.	Typ. (Note 1)	Max.	Units
t_{PW}	Width of Status Strobe			22			22			22			ns
t_{SS}	Set-up Time, Status Inputs D_0-D_7			12			8.0			8.0			ns
t_{SH}	Hold Time, Status Inputs D_0-D_7			5.0			5.0			5.0			ns
t_{DC}	Delay from $\overline{STSTB}$ to $\overline{MEMR}$		CL = 100pF	20	30	60	20	30	60	20	30	40	ns
	Delay from $\overline{STSTB}$ to $\overline{INTA}$, $\overline{IOR}$			20	30	60	20	30	60	20	30	45	
	Delay from $\overline{STSTB}$ to all other Control Signals			20	30	60	20	30	60	20	30	60	
t_{RR}	Delay from DBIN to Control Outputs				15	35		15	30		15	30	ns
t_{RE}	Delay from DBIN to 8080A Bus	Enable	C_L = 25pF		25	45		25	45		12	20	ns
		Disable			25	45		25	45		25	35	
t_{RO}	Delay from System Bus to 8080A Bus During Read				15	30		15	30		15	20	ns
t_{WR}	Delay from $\overline{WR}$ to Control Outputs		C_L = 100pF	5.0	20	45	5.0	20	45	5.0	20	45	ns
t_{WE}	Delay to Enable System Bus DB_0-DB_7 After $\overline{STSTB}$				25	36		25	30		25	30	ns
t_{WD}	Delay from 8080A Bus D_0-D_7 to System Bus DB_0-DB_7 During Write			5.0	20	40	5.0	20	40	5.0	20	40	ns
t_E	Delay from System Bus Enable to System Bus DB_0-DB_7				25	35		25	30		20	30	ns
t_{HD}	HLDA to Read Status Outputs				15	28		15	25		15	25	ns
t_{DS}	Set-up Time, System Bus Inputs to HLDA			10			10			10			ns
t_{DH}	Hold Time, System Bus Inputs to HLDA			20			20			20			ns

Notes: 1. Typical values are for T_A = 25°C and nominal supply voltages.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under electrical characteristics for the applicable device type.

CAPACITANCE (This parameter is periodically sampled and not 100% tested.)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
C_{IN}	Input Capacitance	V_{BIAS} = 2.5V, V_{CC} = 5.0V T_A = 25°C, f = 1.0MHz		8.0	12	pF
C_{OUT}	Output Capacitance Control Signals			7.0	15	pF
I/O	I/O Capacitance (D or DB)			8.0	15	pF

SWITCHING WAVEFORMS

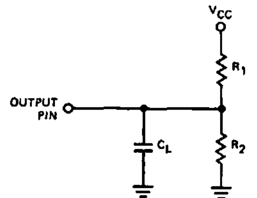


Voltage measurements points: $D_0 - D_7$ (when outputs) Logic "0" = 0.8 V, Logic "1" = 3.0 V. All other signals measured at 1.5 V.

*Extended $\overline{IOW}/\overline{MEMW}$ for Am8238 only.

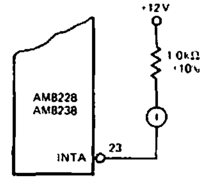
LIC-631

TEST CIRCUITS



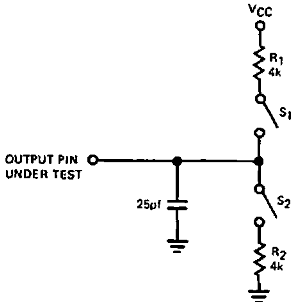
LIC-632

Note 1. For D_0-D_7: $R_1 = 4.0k\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$.
For all other outputs: $R_1 = 500\Omega$, $R_2 = 1.0k\Omega$, $C_L = 100pF$.



LIC-633

INTA (for RST 7)



LIC-634

Test Circuit for DBIN to 8080A BUS

t_{RE}	S_1	S_2
Enable 8080 bus, HIGH-Z to logic "0"	Closed	Open
Enable 8080 bus, HIGH-Z to logic "1"	Open	Closed
Disable 8080 bus, logic "0" to HIGH-Z	Closed	Open
Disable 8080 bus, logic "1" to HIGH-Z	Open	Closed

FUNCTIONAL DESCRIPTION

Bi-Directional Bus Driver: An eight-bit, bi-directional bus driver is provided to buffer the Am9080A/8080A data bus from Memory and I/O devices. The Am9080A data bus has an input requirement of *3.0 volts (min) and can drive (sink) a current of at least 3.2mA. The Am8228 • Am8238 data bus driver matches these input requirements and provides enhanced noise immunity. The output drive is set for 10mA typical for Memory and I/O devices.

The Bi-Directional Bus Drive is controlled by signals from the Gating Array for proper bus flow and the outputs can be forced to high impedance state (three-state) for DMA activities.

Status Latch: The Am8228 • Am8238 stores the status information in the Status Latch when the $\overline{\text{STSTB}}$ input goes "LOW". The output of the Status Latch is connected to the Gating Array and is part of the Control Signal generation.

Gating Array: The Gating Array generates control signals ($\overline{\text{MEM R}}$, $\overline{\text{MEM W}}$, $\overline{\text{I/O R}}$, $\overline{\text{I/O W}}$ and $\overline{\text{INTA}}$) by gating the outputs of the Status Latch Am9080A signals; i.e., DBIN, WE, and HLDA.

*The 8080A has an input requirement of 3.3V and can drive a maximum current of 1.9mA.

The "read" control signals (MEM R, I/O R and INTA) are derived by combinational logic from Status Bit and the DBIN input.

The "write" control signals (MEM W, I/O W) are similarly derived from the Status Bits and the WR input.

All Control Signals are "active LOW" and directly interface RAM, ROM and I/O components.

The INTA control signal is normally used to gate the "interrupt instruction port" onto the bus. It also provides a special feature in the Am8228 • Am8238. If only one basic vector is needed in the interrupt structure, the Am8228 • Am8238 can automatically insert a RST 7 instruction onto the bus. To use this option, connect the INTA output of the Am8228 • Am8238 (pin 23) to the +12 volt supply through a series resistor (1k ohms). The voltage is sensed internally by the Am8228 • Am8238 and logic is "set-up" so that when the DBIN input is active, a RST 7 instruction is gated on to the bus when an interrupt is acknowledged.

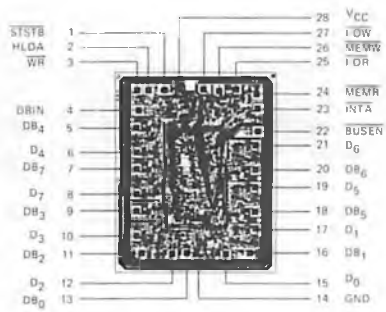
When using a multiple byte instruction as an Interrupt Instruction, the Am8228 • Am8238 will generate an INTA pulse for each of the instruction bytes.

The BUSEN (Bus Enable) input of the Gating Array is an asynchronous input that forces the data bus output buffers and control signal buffers into their high-impedance state if it is a "HIGH". If BUSEN is a "LOW", normal operation of the data buffer and control signals take place. This facilitates CPU independent bus operations such as direct memory access.

DEFINITION OF FUNCTIONAL TERMS

D_7-D_0	Data bus to-from Am9080A/8080A
DB_7-DB_0	Data bus to-from user system
$\overline{\text{I/OR}}$	Input/output read strobe output active LOW
$\overline{\text{I/OW}}$	Input/output write strobe output active LOW
$\overline{\text{MEM R}}$	Memory read strobe, output, active LOW
$\overline{\text{MEM W}}$	Memory write strobe, output, active LOW
DBIN	Data bus input strobe, input active HIGH
$\overline{\text{INTA}}$	Interrupt acknowledge strobe, input, active LOW
HLDA	Hold input from Am9080A/8080A active HIGH
$\overline{\text{WR}}$	Write input strobe, active HIGH
$\overline{\text{BUSEN}}$	BUS ENABLE INPUT, input, 3-state output control, active LOW for 3-state out
$\overline{\text{STSTB}}$	Status Strobe, input, strobes status on data bus into status latch, active LOW

Metallization and Pad Layout



DIE SIZE 0.110" X 0.136"

LOADING RULES

Signal	Pin No.	Input Load	Output Sink	Output Source
D_0	15	250μA	2mA	−10μA
D_1	17	250μA	2mA	−10μA
D_2	12	750μA	2mA	−10μA
D_3	10	250μA	2mA	−10μA
D_4	6	250μA	2mA	−10μA
D_5	19	250μA	2mA	−10μA
D_6	21	750μA	2mA	−10μA
D_7	8	250μA	2mA	−10μA
DB_0	13	250μA	10mA	−1mA
DB_1	16	250μA	10mA	−1mA
DB_2	11	250μA	10mA	−1mA
DB_3	9	250μA	10mA	−1mA
DB_4	5	250μA	10mA	−1mA
DB_5	18	250μA	10mA	−1mA
DB_6	20	250μA	10mA	−1mA
DB_7	7	250μA	10mA	−1mA
$\overline{\text{STSTB}}$	1	500μA	–	–
DBIN	4	250μA	–	–
$\overline{\text{WR}}$	3	250μA	–	–
HLDA	2	250μA	–	–
$\overline{\text{MEM R}}$	24	–	10mA	−1mA
$\overline{\text{MEM W}}$	26	–	10mA	−1mA
$\overline{\text{I/OR}}$	25	–	10mA	−1mA
$\overline{\text{IOW}}$	27	–	10mA	−1mA
$\overline{\text{BUSEN}}$	22	250μA	–	–
$\overline{\text{INTA}}$	23	–	10mA	−1mA
GND	14			
V_{CC}	28			

STATUS WORD CHART

		TYPE OF MACHINE CYCLE									
Data Bus Bit	Status Information	Instruction Fetch	Memory Read	Memory Write	Stack Read	Stack Write	Input Read	Output Write	Interrupt Acknowledge	Halt Acknowledge	Interrupt Acknowledge While Halt
		1	2	3	4	5	6	7	8	9	10
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{\text{WO}}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEM R	1	1	0	1	0	0	0	0	1	0

(N) STATUS WORD

$\overline{\text{INTA}}$
(NONE)
$\overline{\text{INTA}}$
$\overline{\text{I/O W}}$
$\overline{\text{I/O R}}$
$\overline{\text{MEM W}}$
$\overline{\text{MEM R}}$
$\overline{\text{MEM W}}$
$\overline{\text{MEM R}}$
$\overline{\text{MEM R}}$

CONTROL SIGNALS

Operational Amplifiers – Section VI

Am101/201/301

Operational Amplifiers

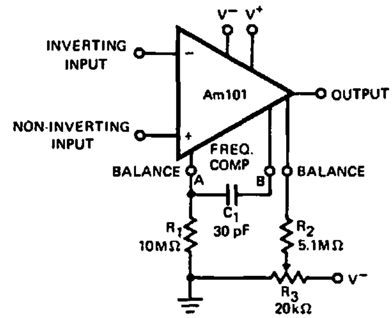
Description: The Am101/201/301 monolithic operational amplifiers are functionally, electrically and pin-for-pin equivalent to the National LM101, and LM201. They are available in the hermetic TO-99 metal can, dual-in-line packages, and flat packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883 Class B.
Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

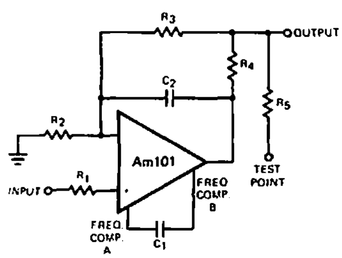
The Am101/201/301 are differential input, class AB output operational amplifiers. The inputs and outputs are protected against overload and the amplifiers may be frequency compensated with an external 30pF capacitor.

FUNCTIONAL DIAGRAM



LIC-635

APPLICATIONS



LIC-636

INPUT/OUTPUT OVERLOAD PROTECTION

If an input is driven from a low-impedance source, a series resistor, R_I should be used to limit the peak instantaneous output current of the source to less than 100 mA. A large capacitor (>0.1μF) is equivalent to a low source impedance and should be protected against by an isolation resistor.

The amplifier output is protected against damage from shorts to ground or to the power supplies by device design. Protection of the output from voltages exceeding the specified operating power supplies can be obtained by isolating the output via limiting resistors R_4 or R_5.

The power supplies must never become reversed, even under transient conditions. Reverse voltages as low as 1 volt can cause damage through excessive current. This hazard can be reduced by using clamp diodes of high peak current rating connected to the device supply lines.

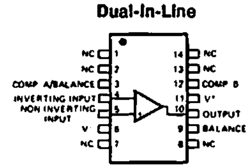
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am301	DIP	0°C to +70°C	LM301D
	Metal Can	0°C to +70°C	LM301H
	Dice	0°C to +70°C	LD301
Am201	DIP	−25°C to +80°C	LM201D
	Metal Can	−25°C to +80°C	LM201H
Am101	DIP	−55°C to +125°C	LM101D
	Metal Can	−55°C to +125°C	LM101H
	Dice	−55°C to +125°C	LD101

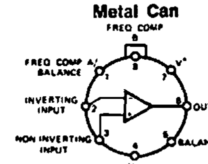
CONNECTION DIAGRAMS

Top Views

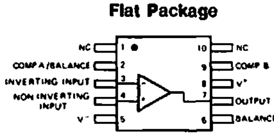
Dual-In-Line



Metal Can



Flat Package



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

(3) On Flat Package, pin 5 is connected to bottom of package.

LIC-637

MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am101	−55°C to +125°C
Am201	−25°C to +85°C
Am301	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 3)

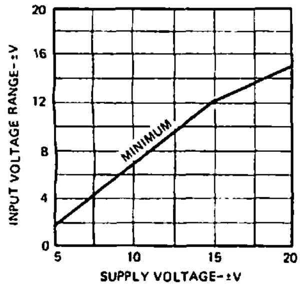
Parameter (see definitions)	Conditions	Am301 Min	Am301 Typ	Am301 Max	Am101 Am201 Min	Am101 Am201 Typ	Am101 Am201 Max	Units
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	7.5		1.0	5.0	mV
Input Offset Current			100	500		40	200	nA
Input Bias Current			250	1500		120	500	nA
Input Resistance		0.1	0.4		0.3	0.8		MΩ
Supply Current	$V_S = \pm 20$V		1.8	3.0		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15$V, $V_{OUT} = \pm 10$V, $R_L > 2$ kΩ	20	150		50	160		V/mV
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10$ kΩ			10			6.0	mV
Input Offset Current	$T_A = T_{A(min)}$ $T_A = T_{A(max)}$		150 50	750 400		100 10	500 200	nA nA
Input Bias Current	$T_A = T_{A(min)}$		0.32	2		0.28	1.5	μA
Large Signal Voltage Gain	$V_S = \pm 15$ V, $V_{OUT} = \pm 10$ V, $R_L > 2$ kΩ	15			25			V/mV
Input Voltage Range	$V_S = \pm 15$ V	±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	65	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Output Voltage Swing	$V_S = \pm 15$ V, $R_L = 10$ kΩ, $R_L = 2$ kΩ	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Supply Current	$T_A = +125$°C $V_S = \pm 20$ V					1.2	2.5	mA

Notes: 1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual-In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C.
2. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
3. Unless otherwise specified, these specifications apply for supply voltages from ±5 V to ±20 V and C_f = 30 pF.

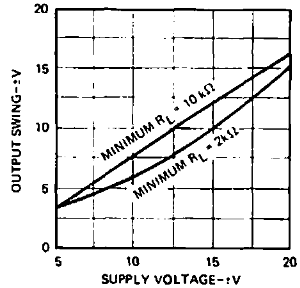
GUARANTEED PERFORMANCE CURVES

(Curves apply over the Operating Temperature Ranges)

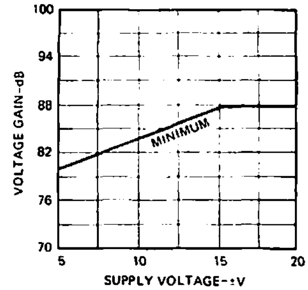
Input Voltage Range



Output Swing



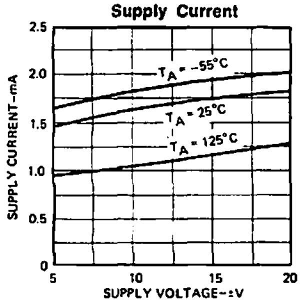
Voltage Gain



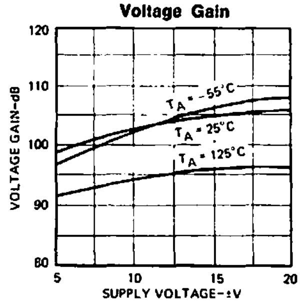
LIC-638

PERFORMANCE CURVES

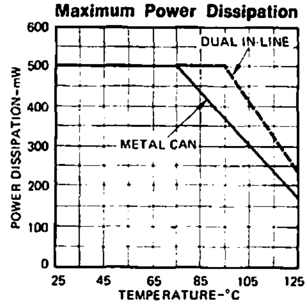
Supply Current



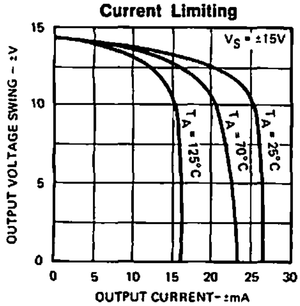
Voltage Gain



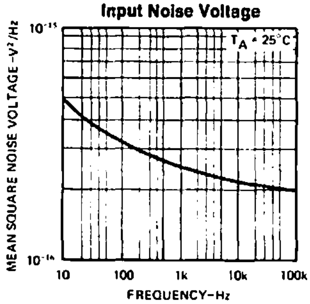
Maximum Power Dissipation



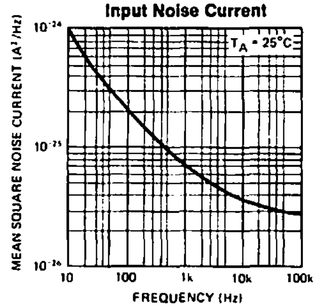
Current Limiting



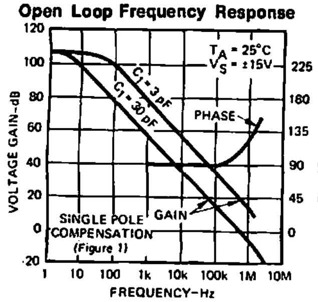
Input Noise Voltage



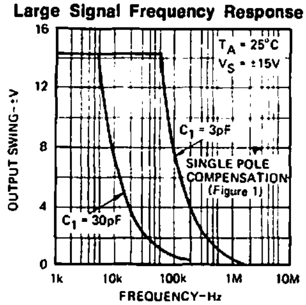
Input Noise Current



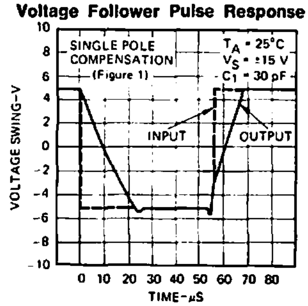
Open Loop Frequency Response



Large Signal Frequency Response



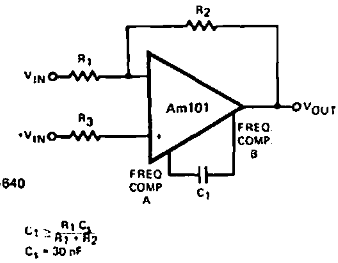
Voltage Follower Pulse Response



LIC-639

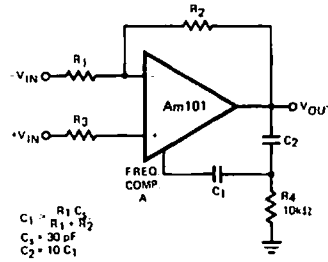
FREQUENCY COMPENSATION CIRCUITS

Single Pole Compensation



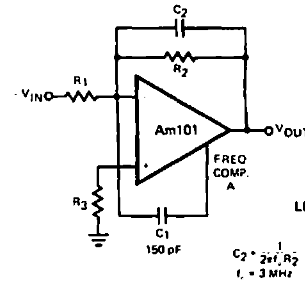
LIC-640

Two Pole Compensation



LIC-641

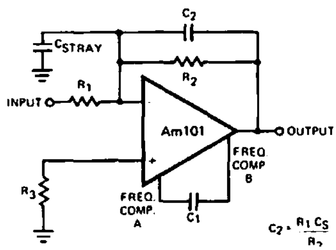
Feedforward Compensation



LIC-642

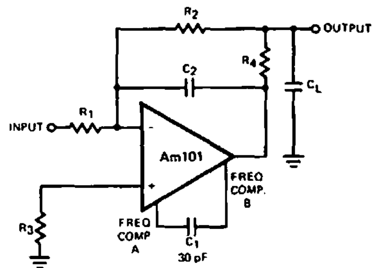
Power supplies should be bypassed to ground at one point, minimum, on each card. More bypass points should be considered for five or more amplifiers on a single card. For applications using feed-forward compensation, the power supply leads of each amplifier should be bypassed with low inductance capacitors.

Compensating for Stray Input Capacitance/Large Feedback Resistance



LIC-643

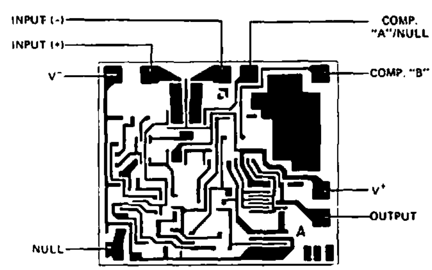
Isolating Large Capacitive Loads



LIC-644

The values given for the frequency compensation capacitor guarantee stability only for source resistances less than 10kΩ, stray capacitances on the summing junction less than 5pF and capacitive loads smaller than 100pF. If any of these conditions is not met, it is necessary to use a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors, or an RC network can be added to isolate capacitive loads.

Metallization and Pad Layout



49 x 56 Mils

Am101A/201A/301A

Operational Amplifiers

Description: The Am101A, Am201A and Am301A monolithic operational amplifiers are functionally, electrically and pin-for-pin equivalent to the National LM101A, LM201A, and LM301A. They are available in the hermetic TO-99 metal can, dual-in-line, and flat packages.

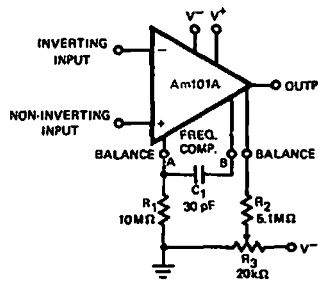
Distinctive Characteristics: 100% reliability ssurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL-STD-883.

Electrically tested and optically inspected dice tor the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am101A/Am201A/Am301A are differential input, class AB output operational amplifiers. The inputs and outputs are protected against overload and the amplifiers may be frequency compensated with an external 30pF capacitor. The combination of low-input currents, low-offset voltage, low noise, and versatility of compensation classify the Am101A/Am201A/Am301A amplifiers for low level and general purpose applications.

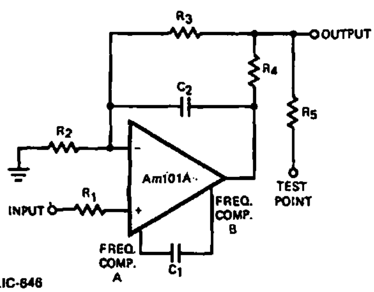
FUNCTIONAL DIAGRAM



LIC-645

APPLICATIONS

INPUT/OUTPUT OVERLOAD PROTECTION



LIC-646

If an input is driven from a low-impedance source, a series resistor, R_1 should be used to limit the peak instantaneous output current of the source to less than 100 mA. A large capacitor (>0.1μF) is equivalent to a low-source impedance and should be protected against by an isolation resistor.

The amplifier output is protected against damage from shorts to ground or to the power supplies by device design. Protection of the output from voltages exceeding the specified operating power supplies can be obtained by isolating the output via limiting resistors R_4 or R_5.

The power supplies must never become reversed, even under transient conditions. Reverse voltages as low as 1 volt can cause damage through excessive current. This hazard can be reduced by using clamp diodes of high peak current rating connected to the device supply lines.

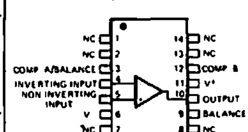
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am301A	DIP	0°C to +70°C	LM301AD
	Metal Can	0°C to +70°C	LM301AH
	Molded DIP	0°C to +70°C	LM301AN
	Dice	0°C to +70°C	LD301A
Am201A	DIP	−25°C to +85°C	LM201AD
	Metal Can	−25°C to +85°C	LM201AH
	Flat Pak	−25°C to +85°C	Lm201AF
Am101A	DIP	−55°C to +125°C	LM101AD
	Metal Can	−55°C to +125°C	LM101AH
	Flat Pak	−55°C to +125°C	LM101AF
	Dice	−55°C to +125°C	LD101A

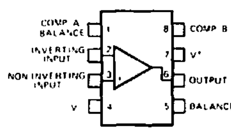
CONNECTION DIAGRAM

Top Views

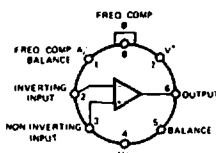
Dual-In-Line



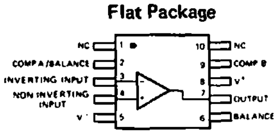
Dual-In-Line



Metal Can



Flat Package



LIC-647

NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

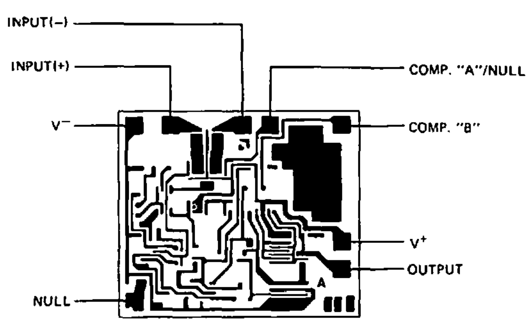
Supply Voltage Am101A, 201A Am301A	 ±22V ±18V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range Am101A Am201A Am301A	 −55°C to +125°C −25°C to +85°C 0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 3)

Parameter (see definitions)	Conditions	Am301A Min	Am301A Typ	Am301A Max	Am101A Am201A Min	Am101A Am201A Typ	Am101A Am201A Max	Units
Input Offset Voltage	$R_S \leq 50$ kΩ		2.0	7.5		0.7	2.0	mV
Input Offset Current			3	50		1.5	10	nA
Input Bias Current			70	250		30	75	nA
Input Resistance		0.5	2		1.5	4		MΩ
Supply Current	$V_S = \pm 20V$ $V_S = \pm 15V$		 1.8	 3.0		1.8	3.0	mA mA
Large Signal Voltage Gain	$V_S = \pm 15$ V, $V_{OUT} = \pm 10$ V, $R_L > 2$ kΩ	25	160		50	160		V/mV
Slew Rate	$V_S = \pm 20V$, $A_V = +1$		0.5			0.5		V/µs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 50$ kΩ			10			3.0	mV
Input Offset Current				70			20	nA
Average Temperature Coefficient of Input Offset Voltage	$T_{A(min)} \leq T_A \leq T_{A(max)}$		6.0	30		3.0	15	µV/°C
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{A(max)}$ $T_{A(min)} \leq T_A \leq 25°C$		0.01 0.02	0.3 0.6		0.01 0.02	0.1 0.2	nA/°C nA/°C
Input Bias Current				300			100	nA
Large Signal Voltage Gain	$V_S = \pm 15$ V, $V_{OUT} = \pm 10$ V, $R_L > 2$ kΩ	25			25			V/mV
Input Voltage Range	$V_S = \pm 20$ V $V_S = \pm 15$ V	 +15, −12			±15			V V
Common Mode Rejection Ratio	$R_S \leq 50$ kΩ	70	90		80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 50$ kΩ	70	96		80	96		dB
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10$ kΩ, $R_L = 2$ kΩ,	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Supply Current	$T_A = +125°C$ $V_S = \pm 20$ V					1.2	2.5	mA

Notes: 1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
3. Unless otherwise specified, these specifications apply for supply voltages from ±5 V to ±20 V for the 101A and 201A, and from ±5 V to ±15 V for the 301A.

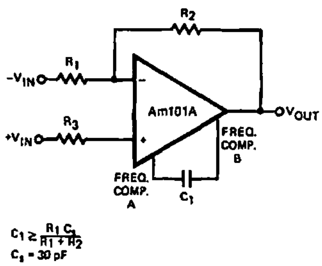
Metallization and Pad Layout



49 X 56 Mils

FREQUENCY COMPENSATION CIRCUITS

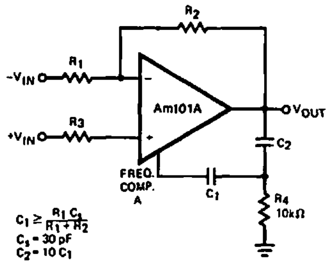
Single Pole Compensation



LIC-648

Figure 1

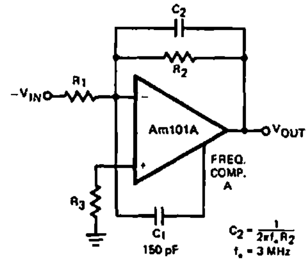
Two Pole Compensation



LIC-649

Figure 2

Feedforward Compensation

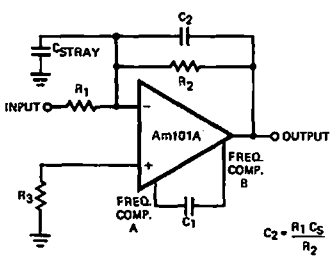


LIC-650

Figure 3

Power supplies should be bypassed to ground at one point, minimum, on each card. More bypass points should be considered for five or more amplifiers on a single card. For applications using feed-forward compensation, the power supply leads of each amplifier should be bypassed with low inductance capacitors.

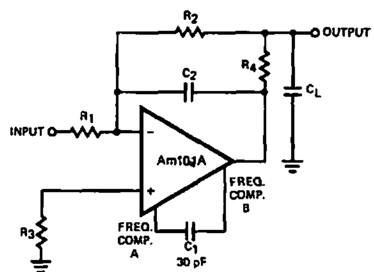
Compensating for Stray Input Capacitance/Large Feedback Resistance



LIC-651

Figure 4

Isolating Large Capacitive Loads



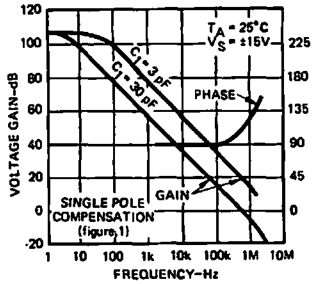
LIC-652

Figure 5

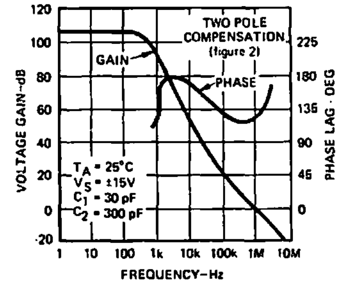
The values given for the frequency compensation capacitor guarantee stability only for source resistances less than 10kΩ, stray capacitances on the summing junction less than 5pF and capacitive loads smaller than 100pF. If any of these conditions is not met, it is necessary to use a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors, or an RC network can be added to isolate capacitive loads.

PERFORMANCE CURVES (Note 3)

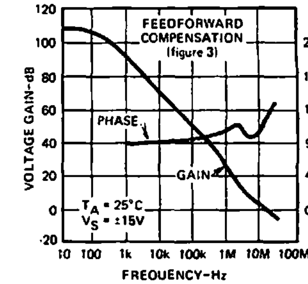
Open Loop Frequency Response



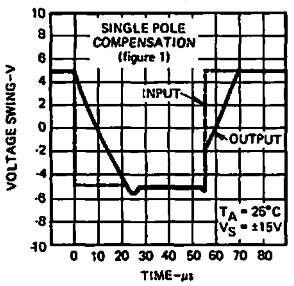
Open Loop Frequency Response



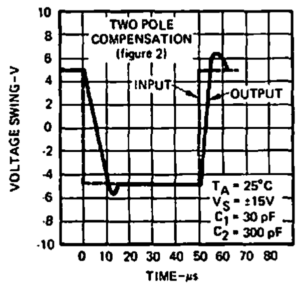
Open Loop Frequency Response



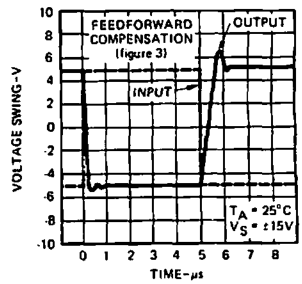
Voltage Follower Pulse Response



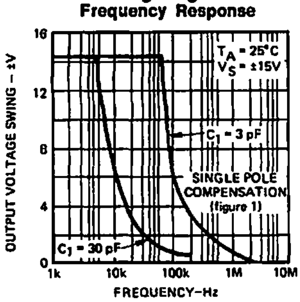
Voltage Follower Pulse Response



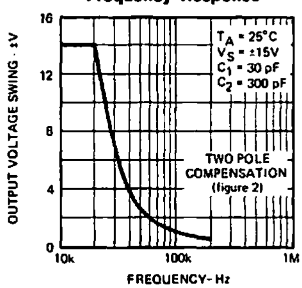
Inverter Pulse Response



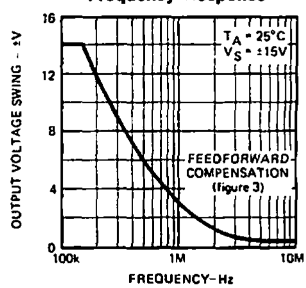
Large Signal Frequency Response



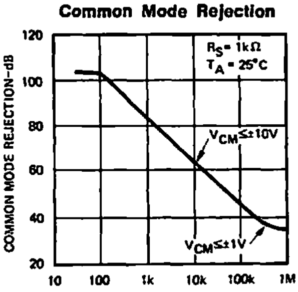
Large Signal Frequency Response



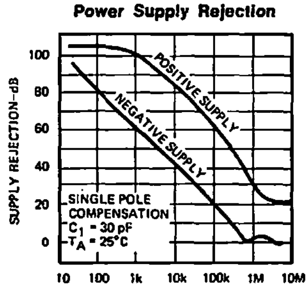
Large Signal Frequency Response



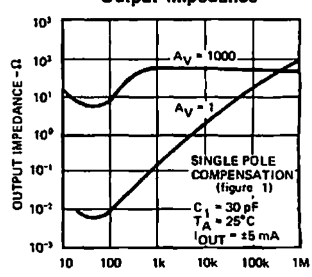
Common Mode Rejection



Power Supply Rejection



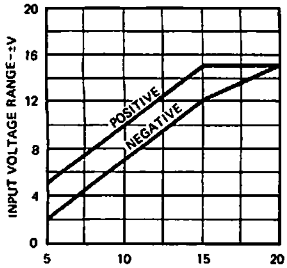
Closed Loop Output Impedance

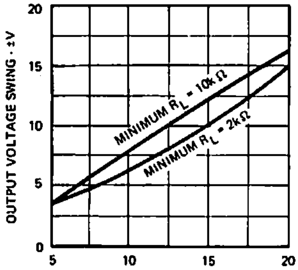


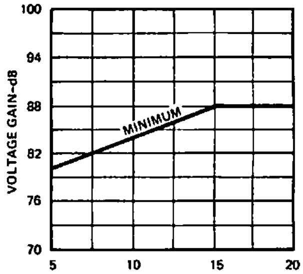
LIC-653

GUARANTEED PERFORMANCE CURVES (Note 3)

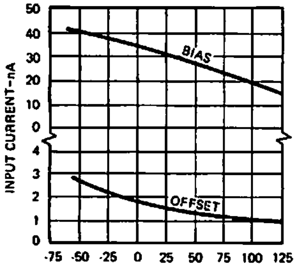
(Curves apply over the Operating Temperature Ranges)

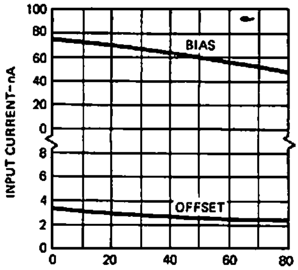


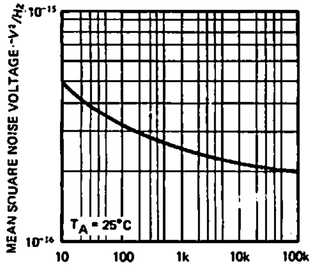


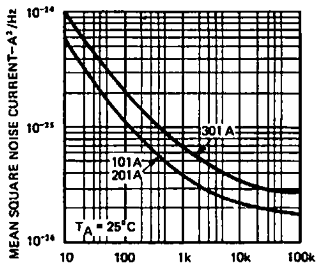


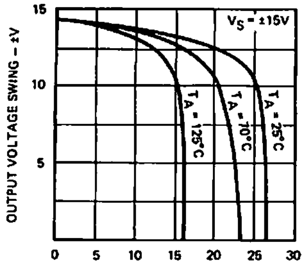
PERFORMANCE CURVES (Note 3)

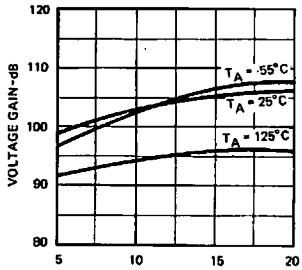


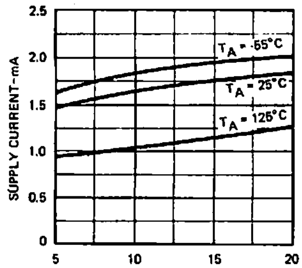












LIC-654

Am102/202/302

Voltage Follower

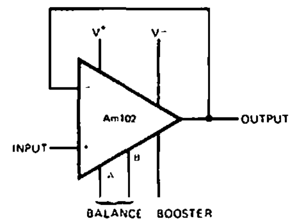
Distinctive Characteristics

- The Am102/202/302 are functionally, electrically, and pin-for-pin equivalent to the National LM102/202/302
- Slew rate: 20V/μs
- Small signal bandwidth: 20MHz
- Input current: 100nA max. over temperature
- Supply voltage range: ±5.0V to ±18V
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected dice for hybrid manufacturers
- Available in metal can, hermetic dual-in-line or hermetic flat packages

FUNCTIONAL DESCRIPTION

The Am102/202/302 is a monolithic Operational Amplifier internally connected as a unity gain non-inverting amplifier. This circuit is ideal for such applications as fast sample and hold circuits, active filters, or as a general purpose buffer. Super-beta transistors are used allowing the devices to operate at very low input currents without sacrificing speed. It may be used to replace conventional op amps such as 101 and the 741 in voltage follower applications, where lower offset voltage, drift, bias current, noise, plus higher speed and a wider operating voltage range is desirable.

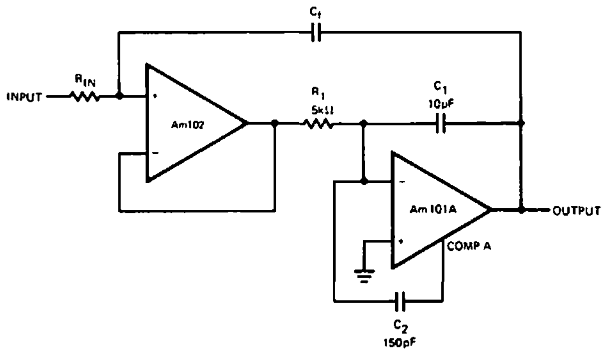
FUNCTIONAL DIAGRAM



LIC-655

TYPICAL APPLICATION

Fast Integrator With Low-Input Current



LIC-656

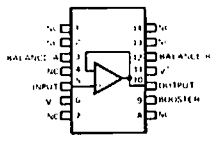
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am302	TO-99	0°C to +70°C	LM302H
	Hermetic DIP	0°C to +70°C	LM302D
	Dice	0°C to +70°C	LD302
Am202	TO-99	-25°C to +85°C	LM202H
	Hermetic DIP	-25°C to +85°C	LM202D
Am102	TO-99	-55°C to +125°C	LM102H
	Hermetic DIP	-55°C to +125°C	LM102D
	Flat Pak	-55°C to +125°C	LM102F
	Dice	-55°C to +125°C	LD102

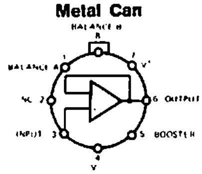
CONNECTION DIAGRAMS

Top Views

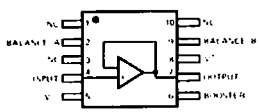
Dual-In-Line



Metal Can



Flat Package



LIC-657

NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

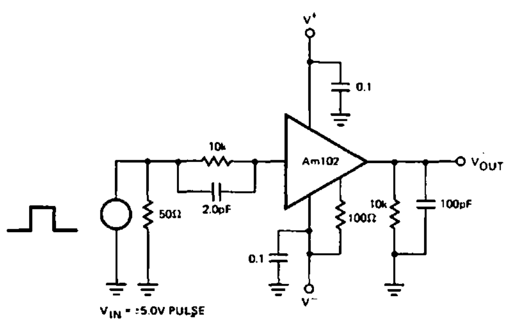
Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
Am102	−55°C to +125°C
Am202	−25°C to + 85°C
Am302	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 60 sec)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

Parameter (see definitions)	Conditions	Am302 Min.	Am302 Typ.	Am302 Max.	Am102 Am202 Min.	Am102 Am202 Typ.	Am102 Am202 Max.	Units
Input Offset Voltage			2.5	15		2.0	5.0	mV
Input Bias Current			2.0	30		3.0	10	nA
Input Resistance		10^3	10^6		10^4	10^6		MΩ
Input Capacitance			1.5			1.5		pF
Large-Signal Voltage Gain	R_L = 8.0kΩ, V_{OUT} = ±10V, V_S = ±15V	0.9985	0.9995		0.999	0.9996		V/V
Output Resistance			0.75	2.5		0.8	2.5	Ω
Supply Current			3.9	5.5		3.9	5.5	mA
Slew Rate	V_S = ±15V, V_{IN} = ±10V, R_L = 10kΩ		20			20		V/µs
The Following Specifications Apply Over The Operating Temperature Range								
Input Offset Voltage				10.0			7.5	mV
Input Bias Current				10.0		30	100	nA
Large-Signal Voltage Gain	R_L = 10kΩ, V_{OUT} = ±10V, V_S = ±15V	0.9985			0.999			V/V
Output Voltage Swing (Note 5)	R_L = 10kΩ, V_S = ±15V	±10			±10			V
Supply Current	T_A = +125°C					2.0	4.0	mA
Supply Voltage Rejection Ratio	±5.0V < V_S < ±18V	60			70			dB
Average Temperature Coefficient of Input Offset Voltage	0°C ≤ T_A < +70°C		20					µV/°C
	−55°C < T_A < +85°C					6.0		µV/°C
	+85°C < T_A < +125°C					12		µV/°C

Notes:
1. Derate Metal Can package 6.8mW/°C for operation at ambient temperatures above 75°C, the Dual-In-Line at 9.0mW/°C for operation at ambient temperatures above 95°C, and the Flat Packages at 5.4mW/°C for operation at ambient temperatures above 57°C.
2. For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.
3. To prevent damage when the output is shorted, it is necessary to insert a resistor larger than 2.0kΩ in series with the input. Continuous short circuit is allowed for case temperatures to +125°C and ambient temperatures to +70°C for the 102/202. For 302, the corresponding temperatures are +70°C and +55°C respectively.
4. Unless otherwise specified, these specifications apply for supply voltages from ±5.0V to ±18V.
5. Greater output voltage swing can be obtained by connecting a resistor from booster terminal to V−.

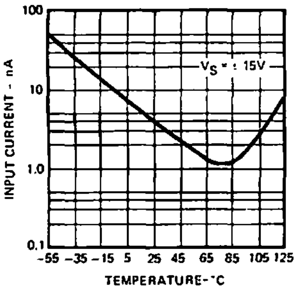
AC TEST CIRCUIT



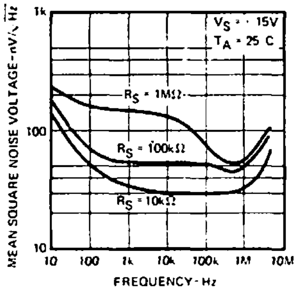
LIC-658

TYPICAL PERFORMANCE CURVES

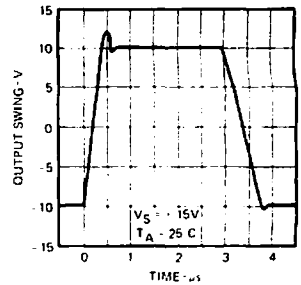
Input Current



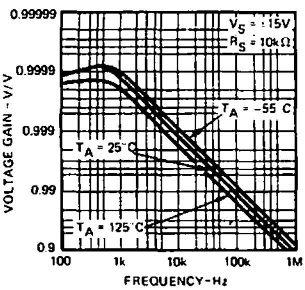
Output Noise Voltage



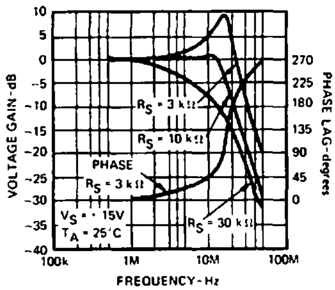
Large Signal Pulse Response



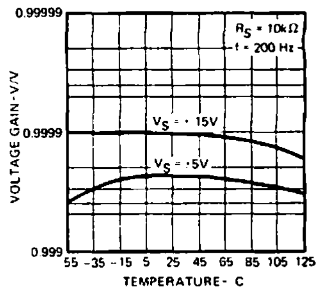
Voltage Gain



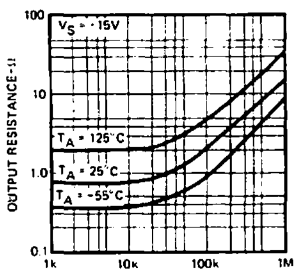
Voltage Gain



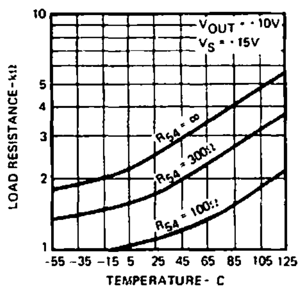
Voltage Gain



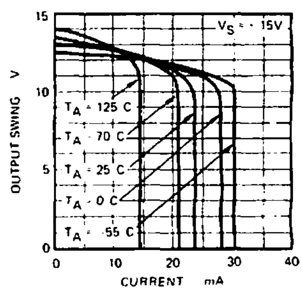
Output Resistance



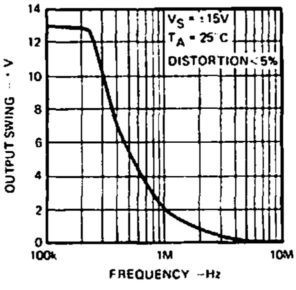
Symmetrical Output Swing



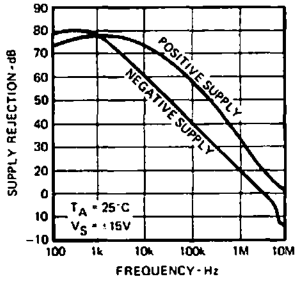
Positive Output Swing



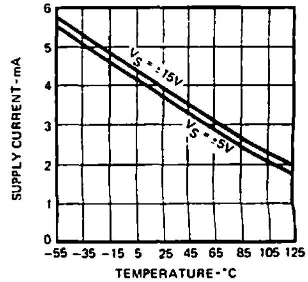
Large Signal Frequency Response



Power Supply Rejection



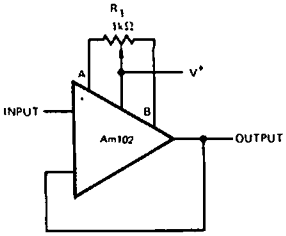
Supply Current



LIC-659

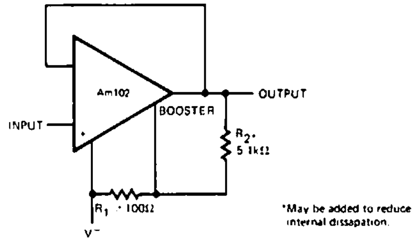
APPLICATIONS

Offset Nulling Circuit



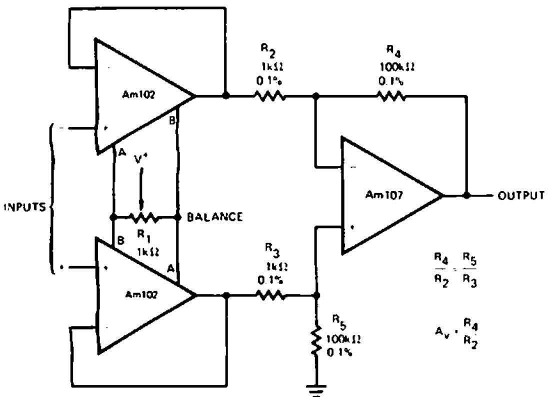
LIC-660

Increasing Negative Swing Under Load



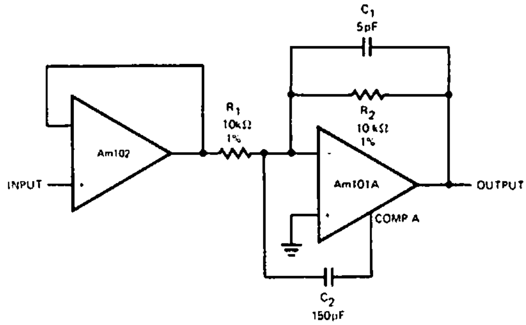
LIC-661

Differential Input Instrumentation Amplifier



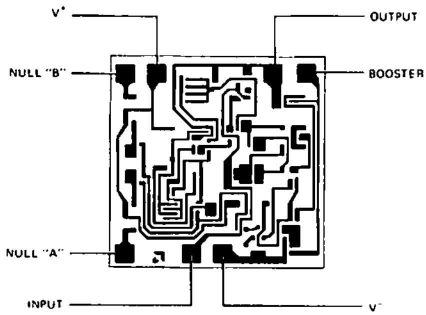
LIC-662

Fast Inverting Amplifier With High Input Impedance



LIC-663

Metallization and Pad Layout



40 x 40 Mils

Am107/207/307

Frequency Compensated Operational Amplifier

Description: The Am107/207/307 Operational Amplifiers are functionally, electrically, and pin-for-pin equivalent to the National LM107/207/307. They are available in the hermetic metal can, flat package, and dual-in-line packages.

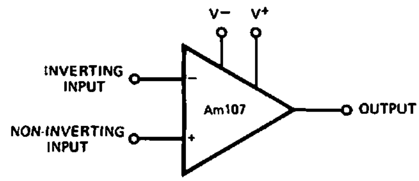
Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am107/207/307 monolithic operational amplifiers are internally frequency compensated and input/output overload protected. These differential input, class AB output amplifiers are intended to provide high accuracy and lower noise in high impedance applications. The Am107/207/307 provide improved electrical parameters and are pin-for-pin replacements for the 709, 101, 101A and 741 in most applications.

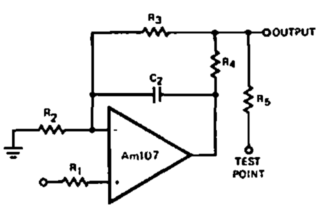
FUNCTIONAL DIAGRAM



LIC-664

APPLICATIONS

Input/Output Protection



LIC-665

If an input is driven from a low-impedance source, a series resistor, R_1 should be used to limit the peak instantaneous output current of the source to less than 100 mA. A large capacitor (>0.1μF) is equivalent to a low source impedance and should be protected against by an isolation resistor .

The amplifier output is protected against damage from shorts to ground or to the power supplies by device design. Protection of the output from voltages exceeding the specified operating power supplies can be obtained by isolating the output via limiting resistors R_4 or R_5.

The power supplies must never become reversed, even under transient conditions. Reverse voltages as low as 1 volt can cause damage through excessive current. This hazard can be reduced by using clamp diodes of high-peak current rating connected to the device supply lines.

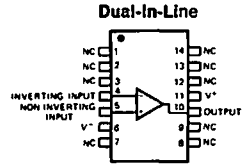
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
	DIP	0°C to +70°C	LM307D
Am307	Metal Can	0°C to +70°C	LM307H
	Dice	0°C to +70°C	LD307
	DIP	−25°C to +85°C	LM207D
Am207	Metal Can	−25°C to +85°C	LM207H
	Flat Package	−25°C to +85°C	LM207F
	DIP	−55°C to +125°C	LM107D
Am107	Metal Can	−55°C to +125°C	LM107H
	Flat Package	−55°C to +125°C	LM107F
	Dice	−55°C to +125°C	LD107

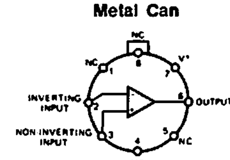
CONNECTION DIAGRAMS

Top View

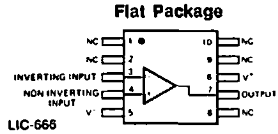
Dual-In-Line



Metal Can



Flat Package



LIC-666

NOTES:
(1) On Metal Can, pin 4 is connected to case.
(2) On DIP, pin 6 is connected to bottom of package.
(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage	
Am107, Am207,	±22V
Am307	±18V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am107	−55°C to +125°C
Am207	−25°C to +85°C
Am307	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified) (Note 3)

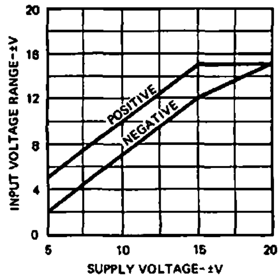
Parameter (see definitions)	Conditions	Am307 Min	Am307 Typ	Am307 Max	Am107 Am207 Min	Am107 Am207 Typ	Am107 Am207 Max	Units
Input Offset Voltage	$R_S \le 50$ kΩ		2.0	7.5		0.7	2.0	mV
Input Offset Current			3	50		1.5	10	nA
Input Bias Current			70	250		30	75	nA
Input Resistance		0.5	2		1.5	4		MΩ
Supply Current	$V_S = \pm 20V$ $V_S = \pm 15V$		 1.8	 3.0		1.8 	3.0 	mA mA
Large Signal Voltage Gain	$V_S = \pm 15$ V, $V_{OUT} = \pm 10$ V, $R_L \ge 2$ kΩ	25	160		50	160		V/mV
Slew Rate	$R_L \ge 2$ kΩ	0.2	0.5		0.2	0.5		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \le 50$ kΩ			10			3.0	mV
Input Offset Current				70			20	nA
Average Temperature Coefficient of Input Offset Voltage	$T_{A(min)} \le T_A \le T_{A(max)}$		6.0	30		3.0	15	μV/°C
Average Temperature Coefficient of Input Offset Current	$25°C \le T_A \le T_{A(max)}$ $T_{A(min)} \le T_A \le 25°C$		0.01 0.02	0.3 0.6		0.01 0.02	0.1 0.2	nA/°C nA/°C
Input Bias Current				300			100	nA
Large Signal Voltage Gain	$V_S = \pm 15$ V, $V_{OUT} = \pm 10$ V, $R_L > 2$ kΩ	25			25			V/mV
Input Voltage Range	$V_S = \pm 20$ V $V_S = \pm 15$ V	 +15, −12			±15 			V V
Common Mode Rejection Ratio	$R_S \le 50$ kΩ	70	90		80	96		dB
Supply Voltage Rejection Ratio	$R_S \le 50$ kΩ	70	96		80	96		dB
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10$ kΩ, $R_L = 2$ kΩ,	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Supply Current	$T_A = +125°C$ $V_S = \pm 20$ V					1.2	2.5	mA

Notes: 1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C, the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 75°C.
2. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
3. Unless otherwise specified, these specifications apply for supply voltages from ±5 V to ±20 V for the Am107 and Am207 and from ±5 V to ±15 V for the Am307.

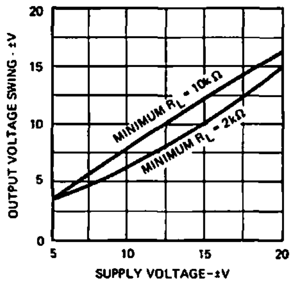
GUARANTEED PERFORMANCE CURVES (Note 3)

(Curves apply over the Operating Temperature Ranges)

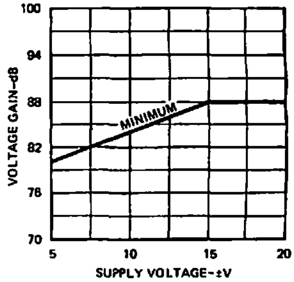
Input Voltage Range



Output Swing

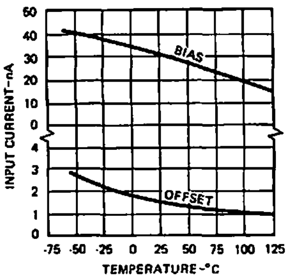


Voltage Gain

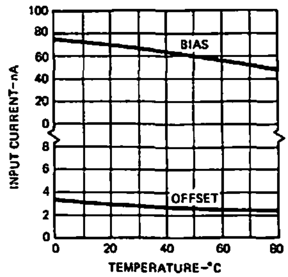


PERFORMANCE CURVES (Note 3)

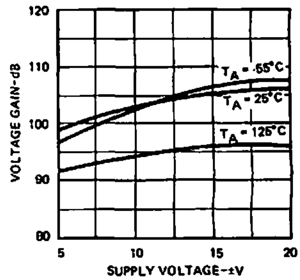
Input Current—Am107, Am207



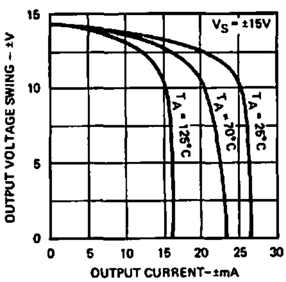
Input Current—Am307



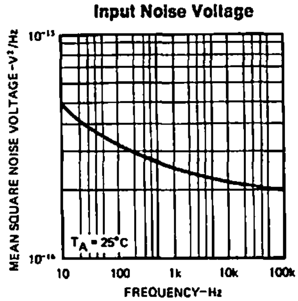
Voltage Gain



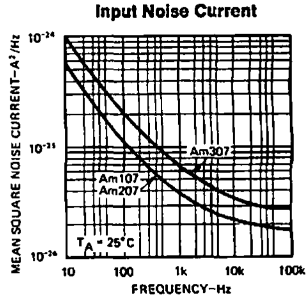
Current Limiting



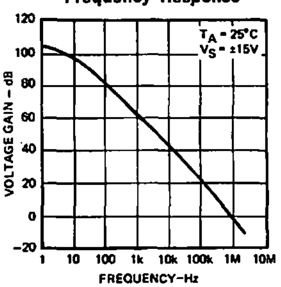
Input Noise Voltage



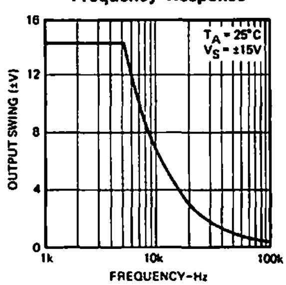
Input Noise Current



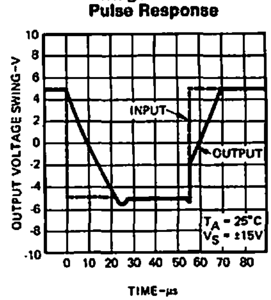
Open Loop Frequency Response



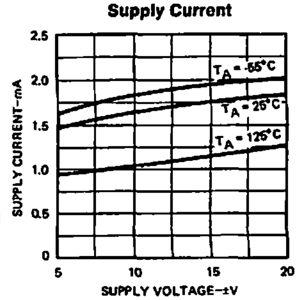
Large Signal Frequency Response



Voltage Follower Pulse Response



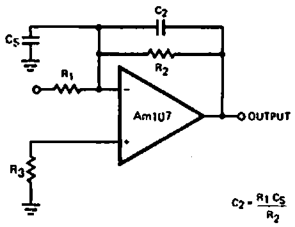
Supply Current



LIC-667

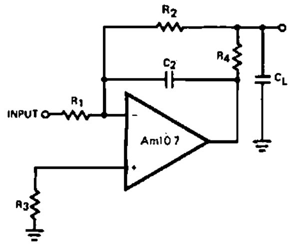
ADDITIONAL APPLICATION INFORMATION

Stray Input Capacitance/Large Feedback Resistance



LIC-668

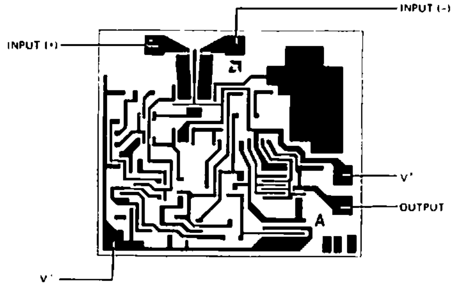
Large Capacitive Loads



LIC-669

Stability is guaranteed for source resistances less than 10 kΩ, stray capacitances on the summing junction less than 5 pF, and capacitive loads smaller than 100 pF. If any of these conditions is not met, lead capacitors may be used in the feedback network to negate the effect of stray capacitance and large feedback resistors, or an RC network can be added to isolate capacitive loads. Power supplies should be bypassed to ground at one point, minimum, on each card. More bypass points should be considered for five or more amplifiers on a single card.

Metallization and Pad Layout



49 x 56 Mils

Am108/208/308•Am108A/208A/308A

Operational Amplifiers

Description: The 108, 208, 308, 108A, 208A and 308A monolithic operational amplifiers are functionally, electrically and pin-for-pin equivalents to the National LM108, LM208, LM308, LM108A, LM208A and LM308A. They are available in the hermetic TO-99 metal can, dual-in-line, and flat packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883.

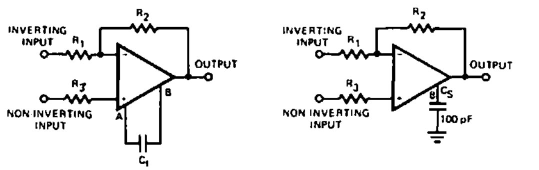
Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

These differential input, precision amplifiers provide low input current and offset voltage competitive with FET and chopper stabilized amplifiers. They feature low power consumption over a supply voltage range of ±2V to ±20V. The amplifiers may be frequency compensated with a single external capacitor and are pin-for-pin interchangeable with the 101A/201A/301A. The 108A, 208A, and 308A are high performance selections from the 108/208/308 amplifier family.

FUNCTIONAL DIAGRAM

Frequency Compensation Circuits



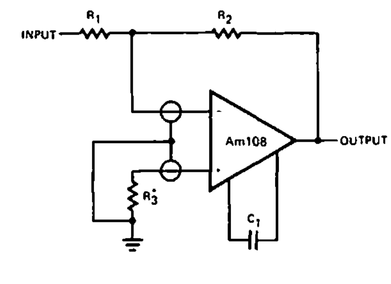
$$C_f \geq C_o \left(\frac{1}{1 + \frac{R_2}{R_1}} \right)$$

C_o = 30 pF

LIC-670

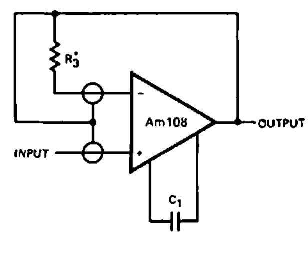
APPLICATIONS

Connection of Input Guards



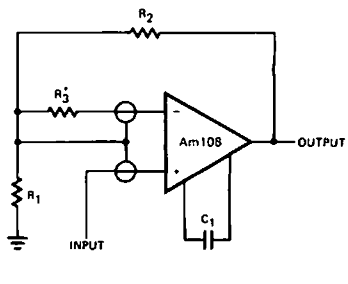
INVERTING AMPLIFIER

LIC-671



FOLLOWER

LIC-672



NON-INVERTING AMPLIFIER

LIC-673

*Use to compensate for large source resistances.

NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ Must be LOW impedance

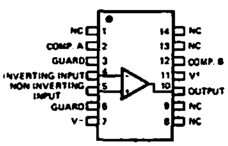
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am308	Hermetic DIP	0°C to +70°C	LM308D
	TO-99	0°C to +70°C	LM308H
	Molded DIP	0°C to +70°C	LM308N
	Dice	0°C to +70°C	LD308
Am308A	Hermetic DIP	0°C to +70°C	LM308AD
	TO-99	0°C to +70°C	LM308AH
	Molded DIP	0°C to +70°C	LM308AN
	Dice	0°C to +70°C	LD308A
Am208	Hermetic DIP	-25°C to +85°C	LM208D
	TO-99	-25°C to +85°C	LM208H
Am208A	Hermetic DIP	-25°C to +85°C	LM208AD
	TO-99	-25°C to +85°C	LM208AH
Am108	Hermetic DIP	-55°C to +125°C	LM108D
	TO-99	-55°C to +125°C	LM108H
	Dice	-55°C to +125°C	LD108
Am108A	Hermetic DIP	-55°C to +125°C	LM108AD
	TO-99	-55°C to +125°C	LM108AH
	Dice	-55°C to +125°C	LD108A

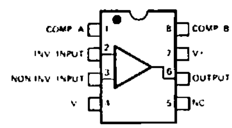
CONNECTION DIAGRAMS

Top Views

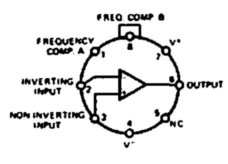
Dual-In-Line



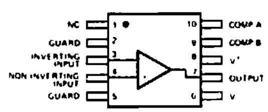
Dual-In-Line



Metal Can



Flat Package



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 7 is connected to bottom of package.

(3) On Flat Package, pin 6 is connected to bottom of package.

LIC-674

MAXIMUM RATINGS

Supply Voltage	
Am108, 208, 108A, 208A,	±20 V
Am308, 308A	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15 V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am108, 108A	−55°C to +125°C
Am208, 208A	−25°C to +85°C
Am308, 308A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

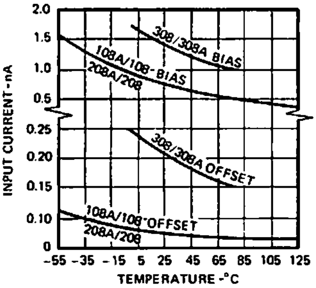
Parameter (see definitions)	Conditions	Am308			Am308A			Am108 Am208			Am108A Am208A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage			2.0	7.5		0.3	0.5		0.7	2.0		0.3	0.5	mV
Input Offset Current			0.2	1.0		0.2	1.0		0.05	0.2		0.05	0.2	nA
Input Bias Current			1.5	7		1.5	7		0.8	2.0		0.8	2.0	nA
Input Resistance		10	40		10	40		30	70		30	70		MΩ
Supply Current	V_S = ±20 V								0.3	0.6		0.3	0.6	mA
	V_S = ±15 V		0.3	0.8		0.3	0.8							mA
Large Signal Voltage Gain	V_S = ±15 V, V_{OUT} = ±10 V, $R_L \geq$ 10 kΩ	25	300		80	300		50	300		80	300		V/mV
The Following Specifications Apply Over The Operating Temperature Ranges														
Input Offset Voltage				10			0.73			3.0			1.0	mV
Input Offset Current				1.5			1.5			0.4			0.4	nA
Average Temperature Coefficient of Input Offset Voltage			6.0	30		1.0	5.0		3.0	15		1.0	5.0	μV/°C
Average Temperature Coefficient of Input Offset Current			2	10		2.0	10		0.5	2.5		0.5	2.5	pA/°C
Input Bias Current				10			10			3.0			3.0	nA
Large Signal Voltage Gain	V_S = ±15 V, V_{OUT} = ±10 V, $R_L \geq$ 10 kΩ	15			60			25			40			V/mV
Input Voltage Range	V_S = ±15 V	±13.5			±13.5			±13.5			±13.5			V
Common Mode Rejection Ratio		80	100		96	110		85	100		96	110		dB
Supply Voltage Rejection Ratio		80	96		96	110		80	96		96	110		dB
Output Voltage Swing	V_S = ±15 V, R_L = 10 kΩ,	±13	±14		±13	±14		±13	±14		±13	±14		V
Supply Current	V_S = ±20 V V_S = ±15 V		0.6	1.0		0.6	0.8		0.15	0.4		0.15	0.4	mA

Notes: 1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.
4. Unless otherwise specified, these specifications apply for supply voltages from ±5 V to ±20 V for the 108, 208, 108A and 208A and from ±5 V to ±15 V for the 308 and 308A.

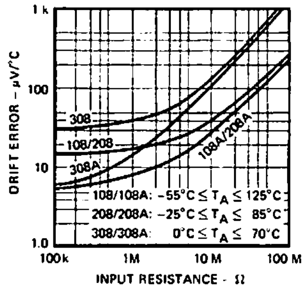
6

TYPICAL PERFORMANCE CURVES

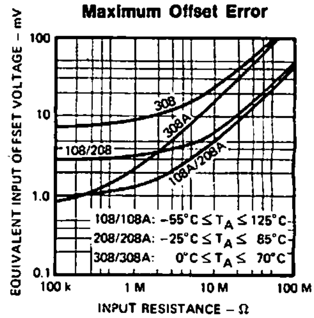
Input Currents



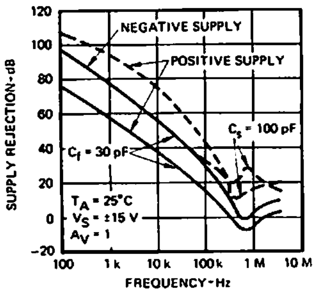
Maximum Drift Error



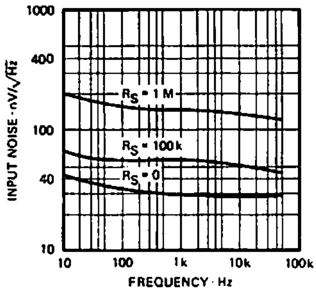
Maximum Offset Error



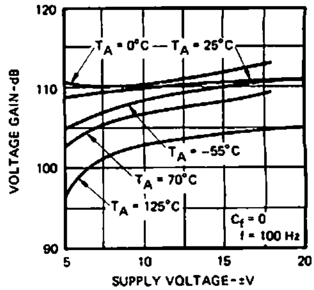
Power Supply Rejection



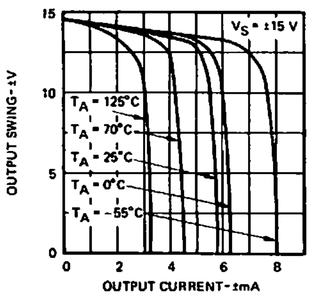
Input Noise Voltage



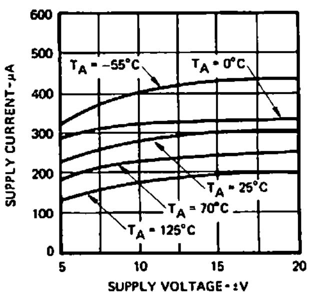
Voltage Gain



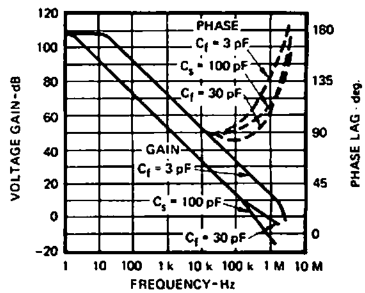
Output Swing



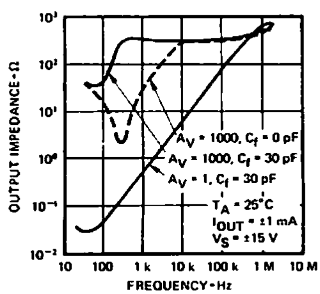
Supply Current



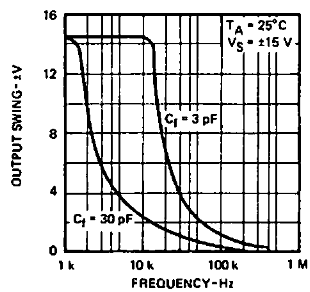
Open Loop Frequency Response



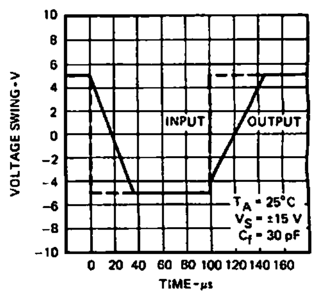
Closed Loop Output Impedance



Large Signal Frequency Response



Voltage Follower Pulse Response



LIC-675

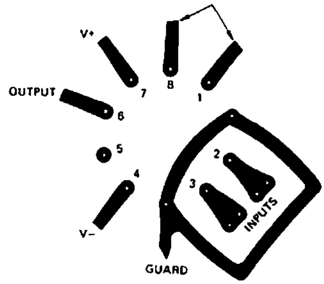
ADDITIONAL APPLICATION INFORMATION

GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

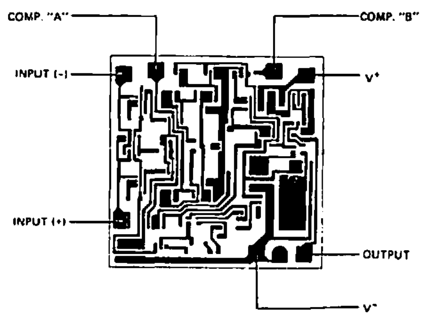
Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the dual-in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration.)



Board layout for Input Guarding with TO-99 package.

Metallization and Pad Layout



56 x 56 Mils

Am110/210/310

Voltage Follower

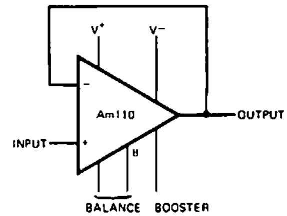
Distinctive Characteristics

- The Am110/210/310 are functionally, electrically, and pin-for-pin equivalent to the National LM 110/210/310
- Slew rate: 30V/μs
- Small signal bandwidth: 20 MHz
- Input current: 10 nA max. over temperature
- Supply voltage range: ±5V to ±18V
- 100% reliability assurance testing in compliance with MIL STD 883.
- Electrically tested and optically inspected dice for hybrid manufacturers.
- Available in metal can, hermetic dual-in-line or hermetic flat packages.

FUNCTIONAL DESCRIPTION

The Am110/210/310 are voltage followers featuring high-speed, low-input currents and large input voltage range. They are internally compensated with provision for external offset adjustment. Operation over wide supply voltages and temperature is possible.

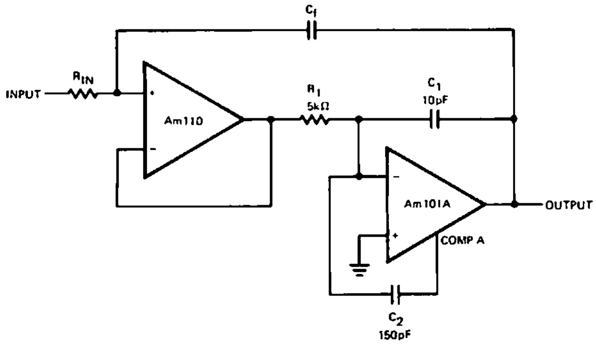
FUNCTIONAL DIAGRAM



LIC-676

TYPICAL APPLICATION

Fast Integrator With Low-Input Current



LIC-677

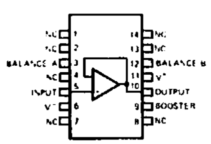
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am310	TO-99	0°C to +70°C	LM310H
	DIP	0°C to +70°C	LM310D
	Flat Package	0°C to +70°C	LM310F
	Molded DIP	0°C to +70°C	LM310N
	Dice	0°C to +70°C	LD310
Am210	TO-99	−25°C to +85°C	LM210H
	DIP	−25°C to +85°C	LM210D
	Flat Pak	−25°C to +85°C	LM210F
Am110	TO-99	−55°C to +125°C	LM110H
	DIP	−55°C to +125°C	LM110D
	Flat Package	−55°C to +125°C	LM110F
	Dice	−55°C to +125°C	LD110

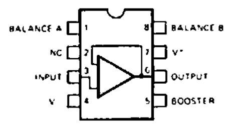
CONNECTION DIAGRAMS

Top Views

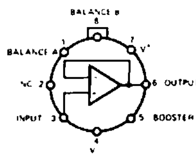
Dual-In-Line



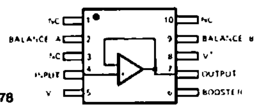
Dual-In-Line



Metal Can



Flat Package



LIC-678

NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

(3) On Flat Package, pin 5 is connected to bottom of package

MAXIMUM RATINGS

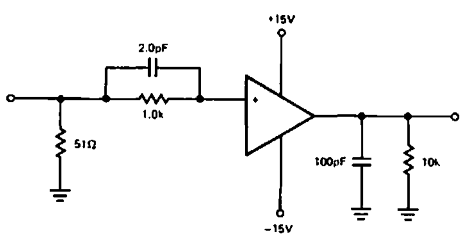
Supply Voltage		±18 V
Internal Power Dissipation (Note 1)		500 mW
Input Voltage (Note 2)		±15 V
Output Short-Circuit Duration (Note 3)		Indefinite
Operating Temperature Range	Am110	−55°C to +125°C
	Am210	−25°C to +85°C
	Am310	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (soldering, 60 sec)		300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

Parameter (see definitions)	Conditions	Am310 Min	Am310 Typ	Am310 Max	Am110 Am210 Min	Am110 Am210 Typ	Am110 Am210 Max	Units
Input Offset Voltage			2.5	7.5		1.5	4.0	mV
Input Bias Current			2.0	7.0		1.0	3.0	nA
Input Resistance		10^4	10^6		10^4	10^6		MΩ
Input Capacitance			1.5			1.5		pF
Large-Signal Voltage Gain	R_L = 8 kΩ, V_{out} = ±10 V, V_S = ±15 V	0.999	0.9999		0.999	0.9999		V/V
Output Resistance			0.75	2.5		0.75	2.5	Ω
Supply Current			3.9	5.5		3.9	5.5	mA
Slew Rate	V_S = ±15 V, V_{IN} = ±10 V, R_L = 10 kΩ		30		20	30		V/µs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage				10.0			6.0	mV
Input Bias Current				10.0			10.0	nA
Large-Signal Voltage Gain	R_L = 10 kΩ, V_{out} = ±10 V, V_S = ±15 V	0.999			0.999			V/V
Output Voltage Swing (Note 5)	R_L = 10 kΩ, V_S = ±15 V	±10			±10			V
Supply Current	T_A = +125°C					2.0	4.0	mA
Supply Voltage Rejection Ratio	±5 V ≤ V_S ≤ ±18 V	70			70			dB
Average Temperature Coefficient of Input Offset Voltage	0° ≤ T_A ≤ 70°C		10					µV/°C
	−55°C ≤ T_A ≤ 85°C +85°C ≤ T_A ≤ 125°C					6 12		µV/°C

Notes: 1. Derate Metal Can package 6.8 mW/°C for operation at ambient temperatures above 75°C, the Dual In-Line at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Packages at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
3. To prevent damage when the output is shorted, it is necessary to insert a resistor larger than 2 kΩ in series with the input. Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 70°C for the 110/210. For 310, the corresponding temperatures are 70°C and 55°C respectively.
4. Unless otherwise specified, these specifications apply for supply voltages from ±5 to ±18 V.
5. Greater output voltage swing can be obtained by connecting a resistor from booster terminal to V−.

AC TEST CIRCUIT

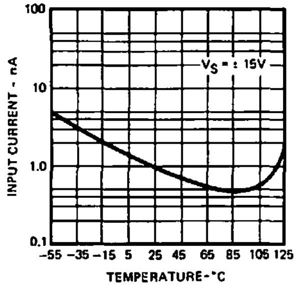


LIC-679

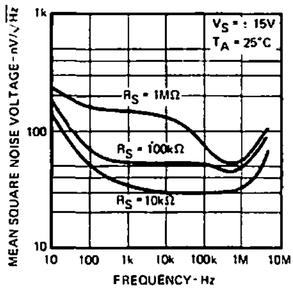
6

PERFORMANCE CURVES

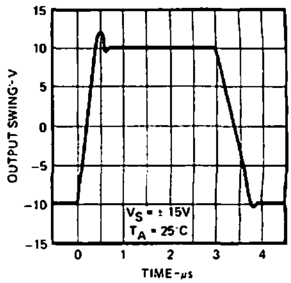
Input Current



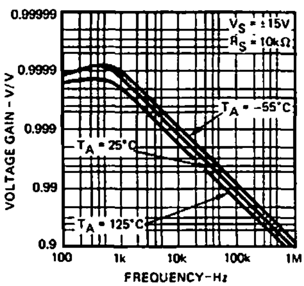
Output Noise Voltage



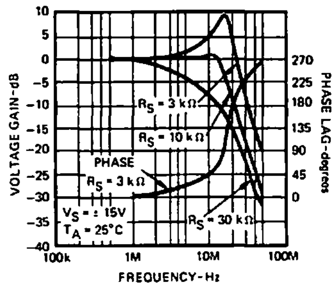
Large Signal Pulse Response



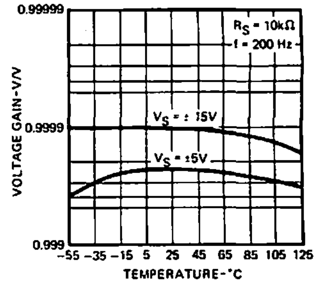
Voltage Gain



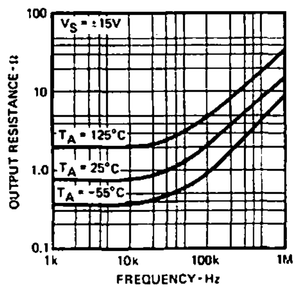
Voltage Gain



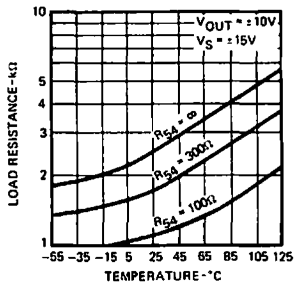
Voltage Gain



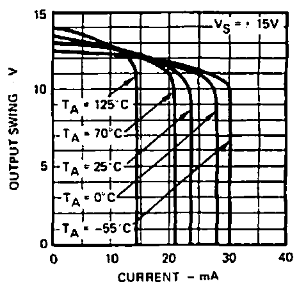
Output Resistance



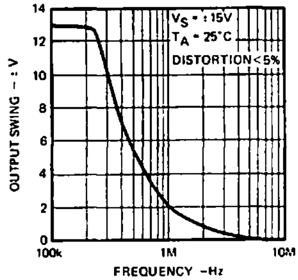
Symmetrical Output Swing



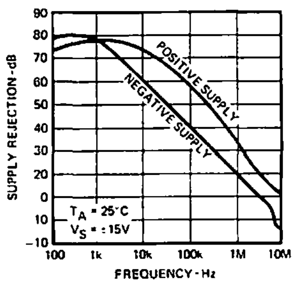
Positive Output Swing



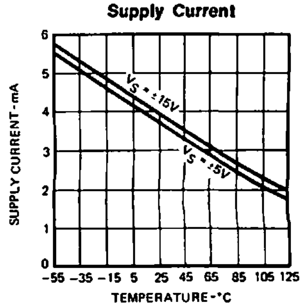
Large Signal Frequency Response



Power Supply Rejection



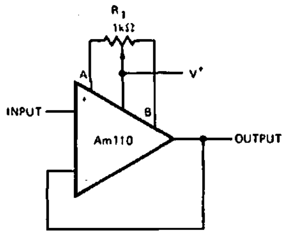
Supply Current



LIC-680

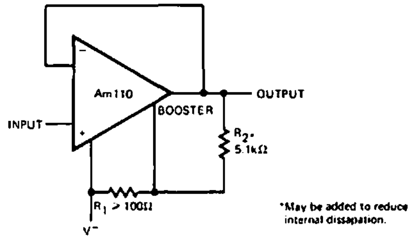
APPLICATIONS

Offset Nulling Circuit



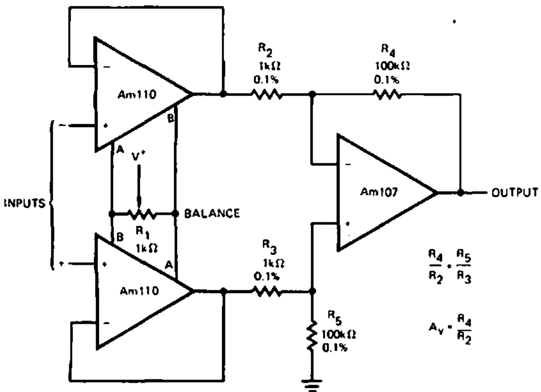
LIC-681

Increasing Negative Swing Under Load



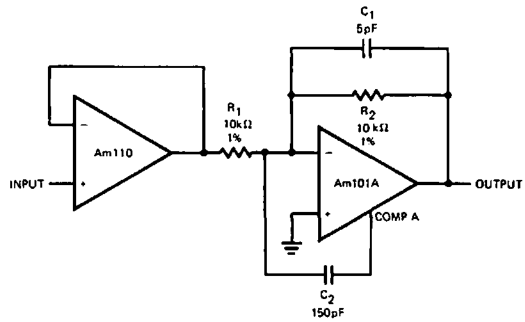
LIC-682

Differential Input Instrumentation Amplifier



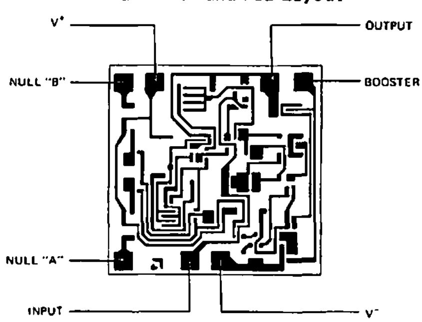
LIC-683

Fast Inverting Amplifier With High Input Impedance



LIC-684

Metallization and Pad Layout



40 x 40 Mils

Am112/212/312

Compensated, High-Performance Operational Amplifier

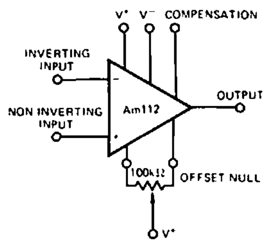
Distinctive Characteristics

- The Am112/212/312 are functionally, electrically, and pin-for-pin equivalents to the National LM112/212/312.
- Low input bias currents: 800pA
- Low input offset currents: 50pA
- Low power consumption: 3mW
- Internal frequency compensation.
- Offset nulling provisions.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected die for assemblers of hybrid products.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Available in metal can, hermetic dual-in-line or hermetic flat packages.

FUNCTIONAL DESCRIPTION

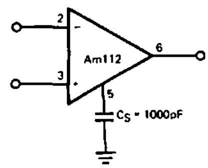
The Am112/212/312 are compensated high-performance operational amplifiers featuring very low offset voltage and input current errors competitive with FET and chopper-stabilized amplifiers. The devices will operate over a supply voltage range of ±2V to ±20V, drawing a typical quiescent current of only 300μA. The Am112/212/312 are internally frequency compensated and provision is made for offset adjustment with a single potentiometer. Overcompensation providing a greater stability margin is possible and the internal protection of the MOS capacitor makes it immune to overvoltage transients.

FUNCTIONAL DIAGRAM



LIC-685

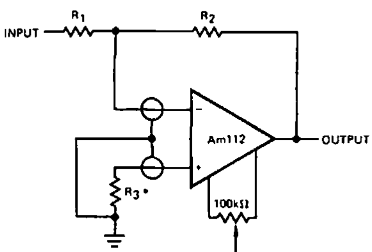
Overcompensation for Greater Stability Margin



LIC-686

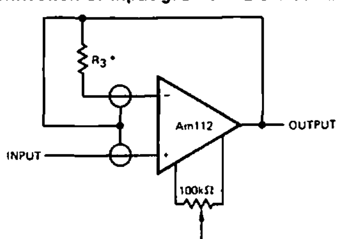
TYPICAL APPLICATIONS

Connection of input guards and offset null



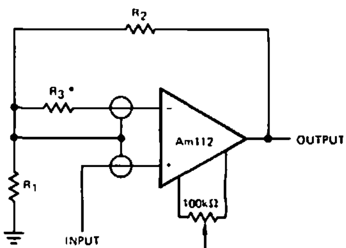
LIC-687

INVERTING AMPLIFIER



LIC-688

FOLLOWER



LIC-689

NON-INVERTING AMPLIFIER

•Use to compensate for large source resistances.

NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ Must be LOW impedance

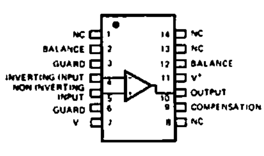
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am312	DIP	0°C to +70°C	LM312D
	Metal Can	0°C to +70°C	LM312H
	Dice	0°C to +70°C	LD312
Am212	DIP	−25°C to +85°C	LM212D
	Metal Can	−25°C to +85°C	LM212
	Flat Pak	−25°C to +85°C	LM212F
AM112	DIP	−55°C to +125°C	LM112D
	Metal Can	−55°C to +125°C	LM112
	Flat Pak	−55°C to +125°C	LM112F
	Dice	−55°C to +125°C	LD112

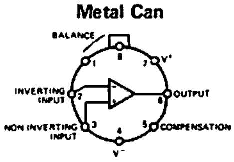
CONNECTION DIAGRAMS

Top Views

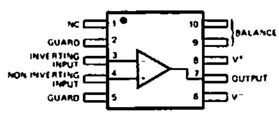
Dual-In-Line



Metal Can



Flat Package



LIC-690

NOTES:
(1) On metal can, pin 4 is connected to case.
(2) On DIP, pin 7 is connected to bottom of package.
(3) On flat package, pin 6 is connected to bottom of package. Compensation terminal is not brought out on the flat package.

MAXIMUM RATINGS

Supply Voltage	
Am112, 212	±20V
Am312	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Current (Note 2)	±10mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am112	−55°C to +125°C
Am212	−25°C to +85°C
Am312	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

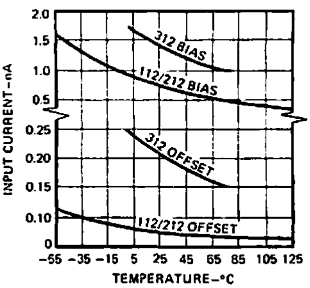
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

Parameter (see definitions)	Conditions	Am312 Min.	Am312 Max.	Am112 Am212 Min.	Am112 Am212 Max.	Units
Input Offset Voltage			7.5		2.0	mV
Input Offset Current			1		0.2	nA
Input Bias Current			7		2.0	nA
Input Resistance		10		30		MΩ
Supply Current			0.8		0.6	mA
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $V_S = \pm 15V$ $R_L > 10k\Omega$	25		50		V/mV
The Following Specifications Apply Over The Operating Temperature Ranges						
Input Offset Voltage			10		3.0	mV
Average Temperature Coefficient of Input Offset Voltage			30		15	μV/°C
Input Offset Current			1.5		0.4	nA
Average Temperature Coefficient of Input Offset Current			10		2.5	pA/°C
Input Bias Current			10		3.0	nA
Supply Current	$T_A = +125°C$				0.4	mA
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $V_S = \pm 15V$ $R_L > 10k\Omega$	15		25		V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	±13		±13		V
Input Voltage Range	$V_S = \pm 15V$	±13.5		±13.5		V
Common Mode Rejection Ratio		80		85		dB
Supply Voltage Rejection Ratio		80		80		dB

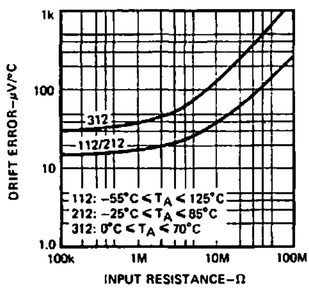
Notes:
1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual-In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
4. Unless otherwise specified, these specifications apply for supply voltages from ±5 V to ±20 V for the Am112, Am212 and from ±5 V to ±15 V for the Am312.

TYPICAL PERFORMANCE CURVES

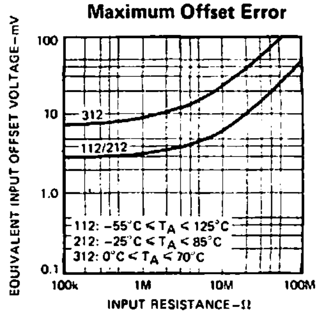
Input Currents



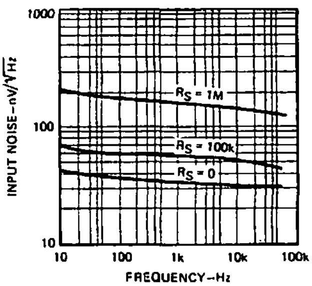
Maximum Drift Error



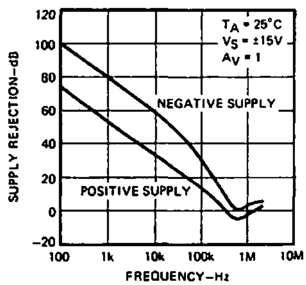
Maximum Offset Error



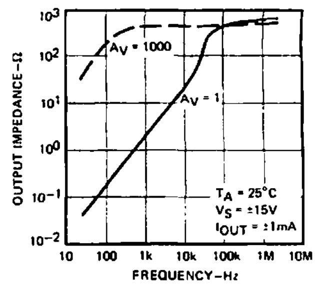
Input Noise Voltage



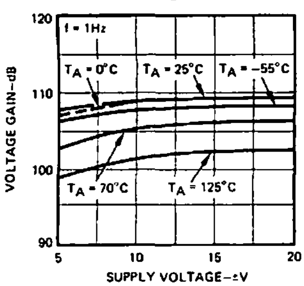
Power Supply Rejection



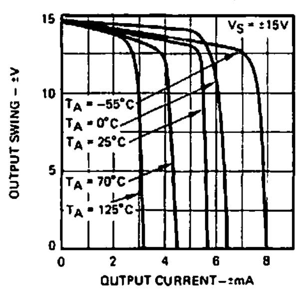
Closed Loop Output Impedance



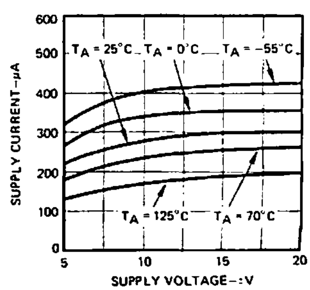
Voltage Gain



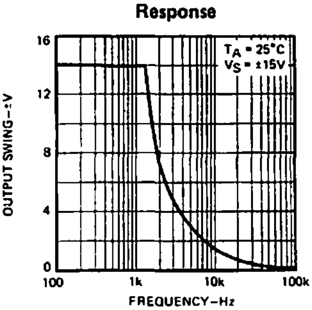
Output Swing



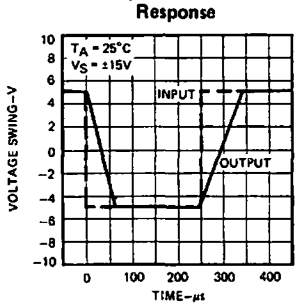
Supply Current



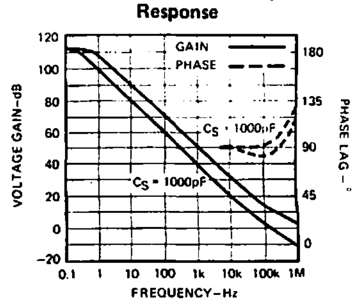
Large Signal Frequency Response



Voltage Follower Pulse Response



Open Loop Frequency Response



LIC-691

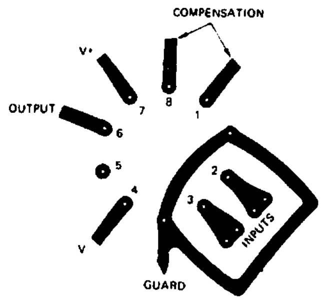
ADDITIONAL APPLICATION INFORMATION

GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 112 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

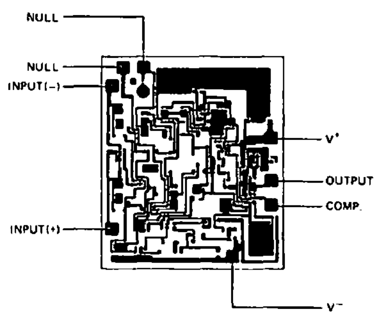
The pin configuration of the dual-in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard Am741 and Am101A pin configuration.)



BOTTOM VIEW

Note: Board layout for input Guarding with TO-99 package.

Metallization and Pad Layout



62 x 72 Mils

Am118/218/318

High-Speed Operational Amplifier

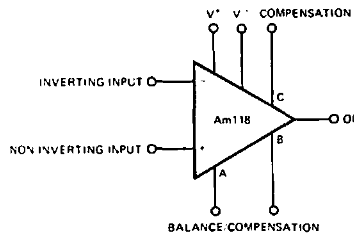
Distinctive Characteristics

- The Am118/218/318 are functionally, electrically, and pin-for-pin equivalent to the National LM118/218/318
- Slew rate: 70V/μs
- Small signal bandwidth: 15MHz
- Internal frequency compensation
- Supply voltage range: ±5V to ±20V
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected dice for hybrid manufacturers.
- Available in metal can, hermetic dual-in-line, hermetic flat package or plastic minidip.

FUNCTIONAL DESCRIPTION

The Am118/218/318 are internally compensated high-speed operational amplifiers featuring minimum slew rate of 50V/μs, low input bias currents, large input voltage range and excellent performance over a wide range of supply voltages and temperature. They have provision for increased speeds when operating in the inverting mode.

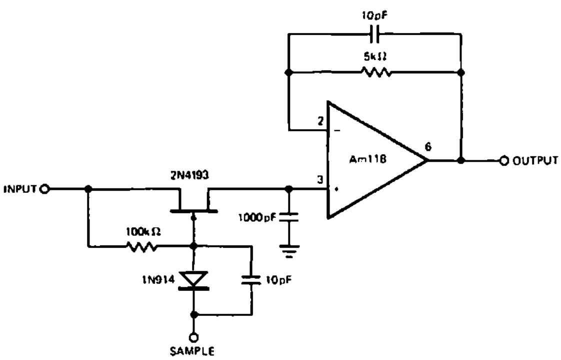
FUNCTIONAL DIAGRAM



LIC-692

TYPICAL APPLICATIONS

Fast Sample and Hold

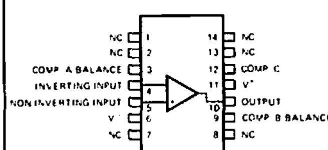


LIC-693

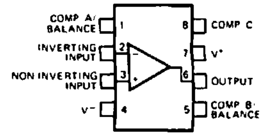
CONNECTION DIAGRAMS

Top Views

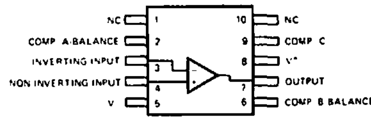
Dual-In-Line



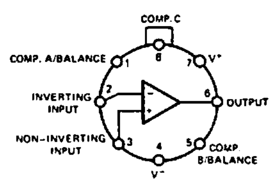
Dual-In-Line



Flat Package



Metal Can



LIC-694

Notes: 1. On Metal Can, pin 4 is connected to case.
2. On DIP, pin 6 is connected to bottom of package.
3. On Flat Package, pin 5 is connected to bottom of package.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am318	Metal Can	0°C to +70°C	LM318H
	DIP	0°C to +70°C	LM318D
	Flat Package	0°C to +70°C	LM318F
	Molded DIP	0°C to +70°C	LM318N
	Dice	0°C to +70°C	LD318
Am218	Metal Can	−25°C to +85°C	LM218H
	DIP	−25°C to +85°C	LM218D
	Flat Pak	−25°C to +85°C	LM218F
Am118	Metal Can	−55°C to +125°C	LM118H
	DIP	−55°C to +125°C	LM118D
	Flat Package	−55°C to +125°C	LM118F
	Dice	−55°C to +125°C	LD118

MAXIMUM RATINGS

Supply Voltage	±20V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage (Note 2)	±5V
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am118	−55°C to +125°C
Am218	−25°C to +85°C
Am318	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

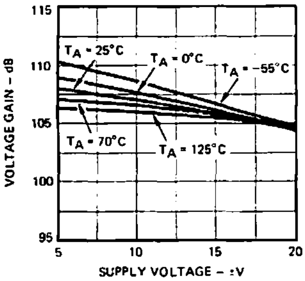
Parameter (see definitions)	Conditions	Am318 Min.	Am318 Typ.	Am318 Max.	Am118 Am218 Min.	Am118 Am218 Typ.	Am118 Am218 Max.	Units
Input Offset Voltage	$R_S \leq 5k\Omega$		4	10		2	4	mV
Input Offset Current			30	200		6	50	nA
Input Bias Current			150	500		120	250	nA
Input Resistance		0.5	3		1.0	3		MΩ
Supply Current	$V_S = \pm 20V$		5	10		5	8	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	25	200		50	200		V/mV
Slew Rate	$A_V = +1$, $V_S = \pm 15V$ (Fig.1), $R_L = 2k\Omega$, $C_L = 30pF$	50	70		50	70		V/µs
Small Signal Bandwidth	$V_S = \pm 15V$		15			15		MHz
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 5k\Omega$			15			6	mV
Input Offset Current				300			100	nA
Input Bias Current				750			500	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	20			25			V/mV
Input Voltage Range	$V_S = \pm 15V$	±11.5			±11.5			V
Common Mode Rejection Ratio	$R_S \leq 5k\Omega$	70			80			dB
Supply Voltage Rejection Ratio	$R_S \leq 5k\Omega$	65			70			dB
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 2k\Omega$	±12	±13		±12	±13		V
Supply Current	$V_S = \pm 20V$, $T_A = 125°C$						7	mA

Notes:
1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C, the Dual-In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. The inputs are shunted with diodes for overvoltage protection. To limit the current in the protection diodes, resistances of 2 kΩ or greater should be inserted in series with the input leads for differential input voltages greater than ±5 V.
3. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
4. Unless otherwise specified, these specifications apply for supply voltages from ±5 V to ±20 V.

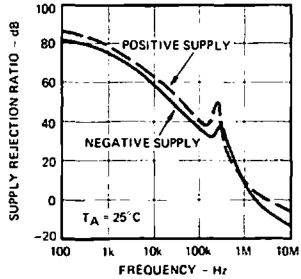
6

PERFORMANCE CURVES

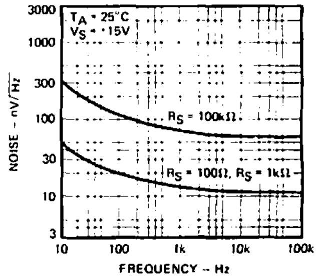
Voltage Gain



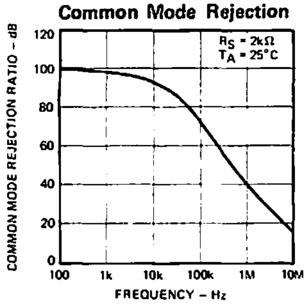
Power Supply Rejection



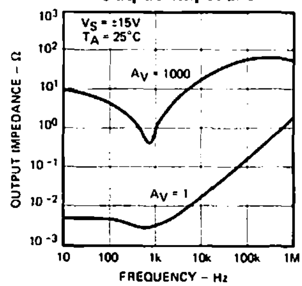
Input Noise Voltage



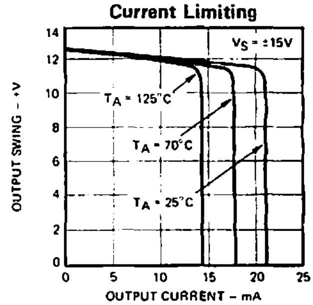
Common Mode Rejection



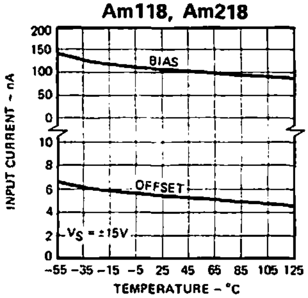
Closed Loop Output Impedance



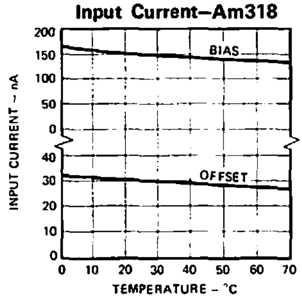
Current Limiting



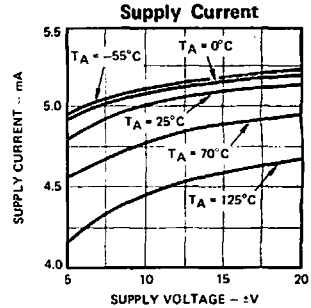
Input Current Am118, Am218



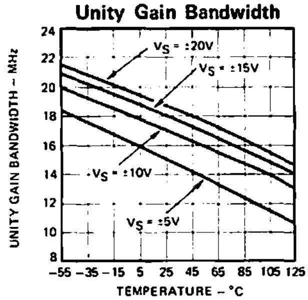
Input Current–Am318



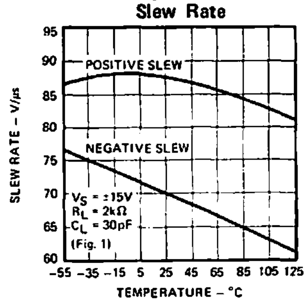
Supply Current



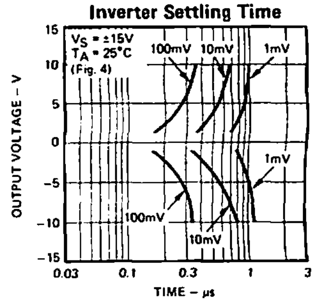
Unity Gain Bandwidth



Voltage Follower Slew Rate



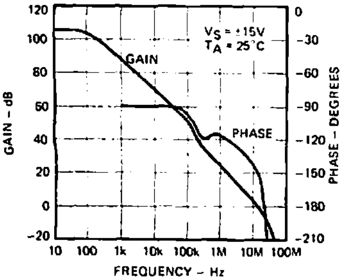
Inverter Settling Time



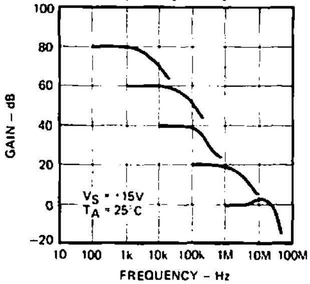
LIC-695

PERFORMANCE CURVES

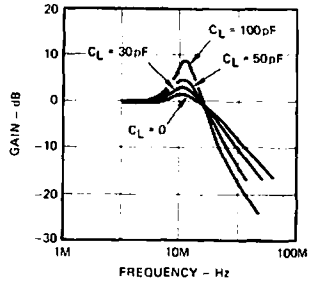
Open Loop Frequency Response



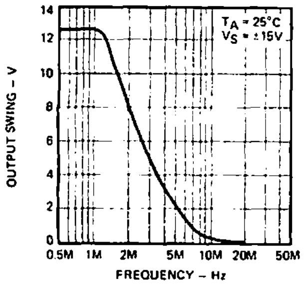
Closed Loop Frequency Response



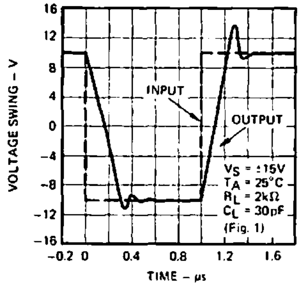
Effect of Capacitive Loading on Closed Loop Frequency Response



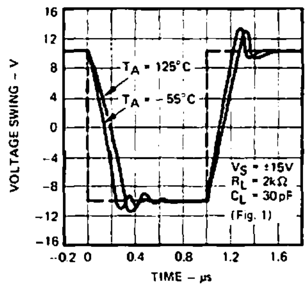
Large Signal Frequency Response



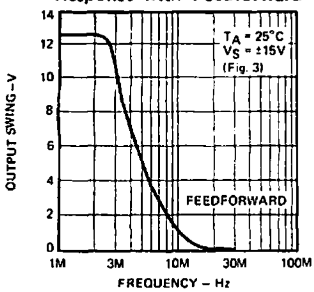
Voltage Follower Pulse Response



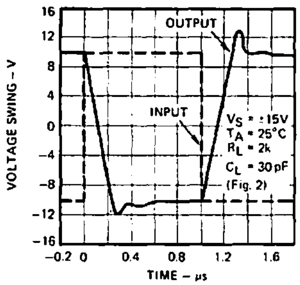
Voltage Follower Pulse Response Over Temperature



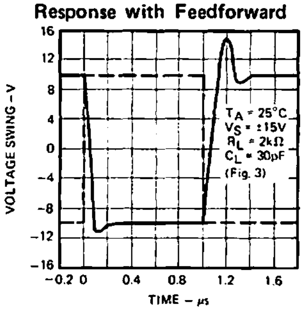
Large Signal Frequency Response with Feedforward



Inverter Pulse Response without Feedforward



Inverter Pulse Response with Feedforward



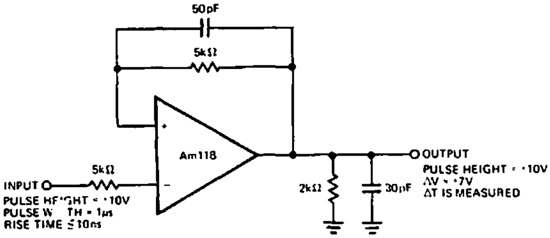
The high gain and large bandwidth of the Am118 make it mandatory to observe the following precautions in using the device, as is the case with any high-frequency amplifier. Circuit layout should be arranged to keep all lead lengths as short as possible and the output separated from the inputs. The values of the feedback and source impedances should be kept small to reduce the effect of stray capacitance at the inputs. The power supplies must be bypassed to ground at the supply leads of the amplifier with low inductance capacitors. Capacitive loading must be kept to minimum, or the amplifier must be isolated as shown in the applications.

LIC-696

6

APPLICATIONS

Voltage Follower (Slew Rate Test Circuit)



LIC-697

Figure 1

Inverter

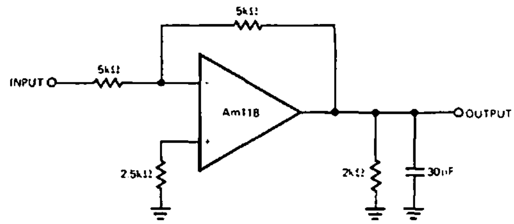
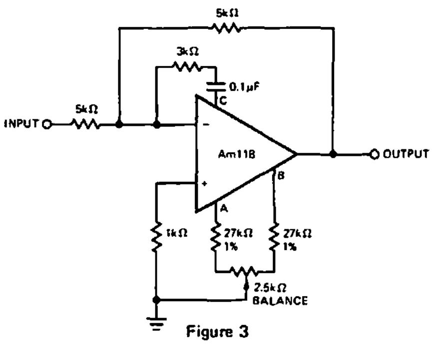


Figure 2

LIC-698

Inverter with Feedforward Compensation for Higher Slew Rate



LIC-699

Figure 3

Compensation for Minimum Settling Time

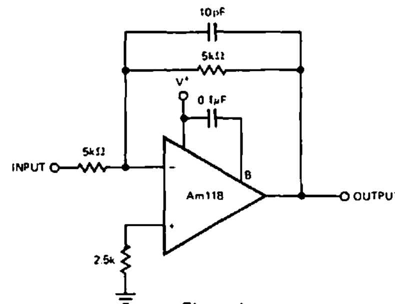
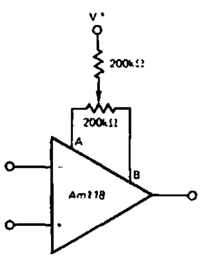


Figure 4

LIC-700

Offset Nulling



LIC-701

Figure 5

Isolating Large Capacitive Loads

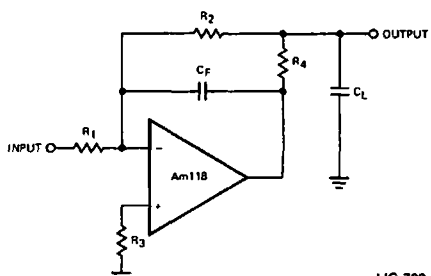


Figure 6

LIC-702

Over Compensation

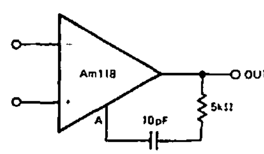
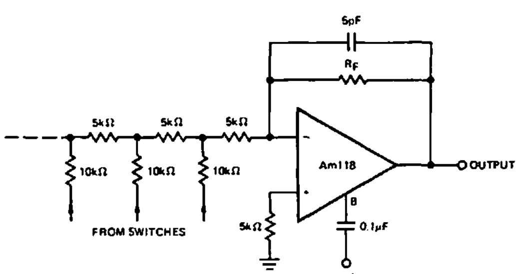


Figure 7

LIC-703

D/A Converter with Ladder Network



LIC-704

Figure 8

D/A Converter with Binary Network

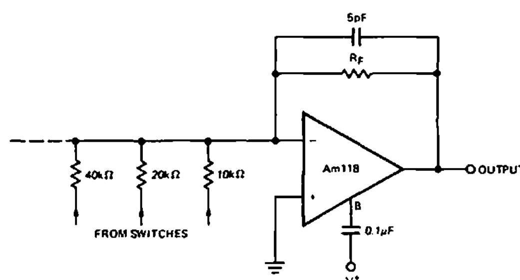


Figure 9

LIC-705

ADDITIONAL APPLICATIONS

High Speed Summing Amplifier with Low Input Bias Currents

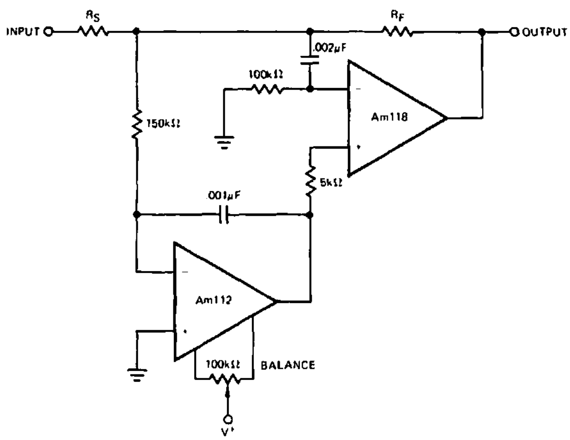
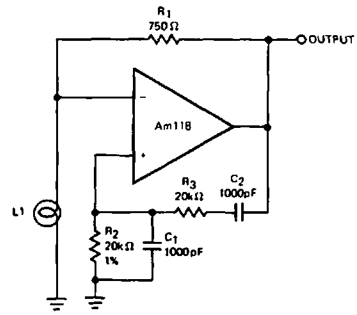


Figure 10

LIC-706

Wien Bridge Oscillator

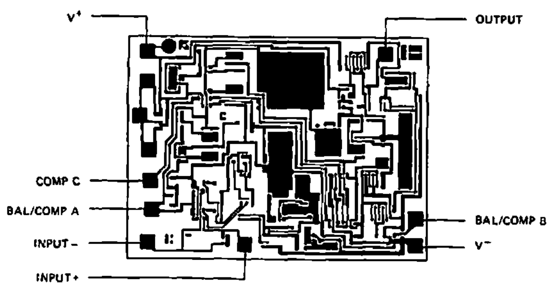


L1–10V–14mA
bulb ELDEMA 1869
$R1 = R_2$
$C_1 = C_2$
$f = \frac{1}{2\pi R1C1}$

Figure 11

LIC-707

Metallization and Pad Layout



64 X 86 Mils

Am124/224/324
Am124A/224A/324A

Quad Op Amps

Distinctive Characteristics

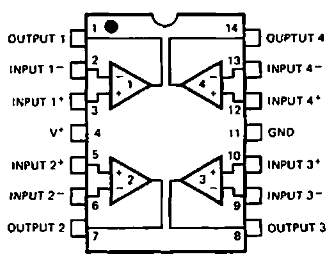
- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated
- Internally frequency compensated for unity gain
- Large dc voltage gain – 100dB
- Wide bandwidth (unity gain) – 1MHz (temperature compensated)
- Wide power supply range:
  Single supply – 3V to 30V
  Dual supplies – ±1.5V to ±15V
- Very low supply current drain (800μA) – essentially independent of supply voltage (1mW/op amp at +5V)
- Low input biasing current – 45nA (temperature compensated)
- Low input offset voltage – 2mV and offset current – 5nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing – 0V to V^+ –1.5V

FUNCTIONAL DESCRIPTION

The Am124 series consists of four independent, high gain, internally frequency compensated operational amplifiers designed primarily to operate from a single power supply over a wide range of voltages. These devices can also operate from split power supplies and the low power supply current drain is independent of the magnitude of the power supply voltage.

Functional applications consist of all the conventional op amp circuits which can now be more easily implemented in single power supply systems along with transducer amplifiers and dc gain blocks.

CONNECTION DIAGRAM
Top View



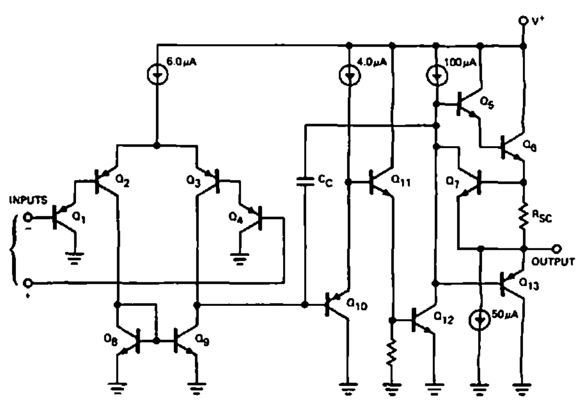
Note: Pin 1 is marked for orientation.

LIC-708

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
	Hermetic DIP	0°C to +70°C	LM324D
Am324	Molded DIP	0°C to +70°C	LM324N
	Dice	0°C to +70°C	LD324
Am224	Hermetic DIP	−25°C to +85°C	LM224D
	Hermetic DIP	−55°C to +125°C	LM124D
Am124	Flat Pack	−55°C to +125°C	LM124F
	Dice	−55°C to +125°C	LM124
	Hermetic DIP	0°C to +70°C	LM324AD
Am324A	Molded DIP	0°C to +70°C	LM324AN
	Dice	0°C to +70°C	LM324A
Am224A	Hermetic DIP	−25°C to +85°C	LM224AD
	Hermetic DIP	−55°C to +125°C	LM124AD
Am124A	Flat Pack	−55°C to +125°C	LM124AF
	Dice	−55°C to +125°C	LD124A

SCHEMATIC DIAGRAM (Each Amplifier)



LIC-709

ELECTRICAL CHARACTERISTICS ($V^+ = +5.0 V_{DC}$, Note 4)

Parameter	Conditions	Am124A Min.	Am124A Typ.	Am124A Max.	Am224A Min.	Am224A Typ.	Am224A Max.	Am324A Min.	Am324A Typ.	Am324A Max.	Am124/Am224 Min.	Am124/Am224 Typ.	Am124/Am224 Max.	Am324 Min.	Am324 Typ.	Am324 Max.	Units
Input Offset Voltage	$T_A = 25°C$ (Note 5)		1.0	2.0		1.0	3.0		2.0	3.0		±2.0	±5.0		±2.0	±7.0	mV_{DC}
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$		20	50		40	80		45	100		45	150		45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		2.0	10		2.0	15		5.0	30		±3.0	±30		±5.0	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30V_{DC}$, $T_A = 25°C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Supply Current	$R_L = \infty$, $V_{CC} = 30V$		1.5	3.0		1.5	3.0		1.5	3.0		1.5	3.0		1.5	3.0	mA_{DC}
Supply Current	$R_L = \infty$		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	mA_{DC}
Large Signal Voltage Gain	$V^+ = 15V_{DC}$ (For large V_O swing) $R_L > 2.0k\Omega$, $T_A = 25°C$	50	100		50	100		25	100		50	100		25	100		V/mV
Output Voltage Swing	$R_L = 2.0k\Omega$, $T_A = 25°C$										0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Common-Mode Rejection Ratio	DC, $T_A = 25°C$	70	85		70	85		65	85		70	85		65	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		dB
Amplifier to Amplifier Coupling (Note 8)	f = 1.0kHz to 20kHz, $T_A = 25°C$ (Input referred)		−120			−120			−120			−120			−120		dB
Output Current — Source	$V_{IN^+} = 1.0V_{DC}$, $V_{IN^-} = 0V_{DC}$, $V^+ = 15V_{DC}$, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		mA_{DC}
Output Current — Sink	$V_{IN^-} = 1.0V_{DC}$, $V_{IN^+} = 0V_{DC}$, $V^+ = 15V_{DC}$, $T_A = 25°C$	10	20		10	20		10	20		10	20		10	20		mA_{DC}
Output Current — Sink	$V_{IN^-} = 1.0V_{DC}$, $V_{IN^+} = 0V_{DC}$, $T_A = 25°C$, $V_O = 200mV_{DC}$	12	50		12	50		12	50		12	50		12	50		μA_{DC}
Short Circuit to Ground	$T_A = 25°C$ (Note 2)		40	60		40	60		40	60		40	60		40	60	mA_{DC}
Input Offset Voltage	Note 5			4.0			4.0			5.0			±7.0			±9.0	mV_{DC}
Input Offset Voltage Drift	$R_S = 0\Omega$		7.0	20		7.0	20		7.0	30		7.0			7.0		μV/°C
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			30			30			75			±100			±150	nA_{DC}
Input Offset Current Drift			10	200		10	200		10	300		10			10		$pA_{DC}/°C$
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30V_{DC}$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	V_{DC}
Large Signal Voltage Gain	$V^+ = +15V_{DC}$ (For large V_O swing) $R_L > 2.0k\Omega$	25			25			15			25			15			V/mV
Output Voltage Swing — V_{OH}	$V^+ = +30V_{DC}$, $R_L = 2.0k\Omega$	26			26			26			26			26			V_{DC}
Output Voltage Swing — V_{OH}	$R_L > 10k\Omega$	27	28		27	28		27	28		27	28		27	28		V_{DC}
Output Voltage Swing — V_{OL}	$V^+ = 5.0V_{DC}$, $R_L \leq 10k\Omega$		5.0	20		5.0	20		5.0	20		5.0	20		5.0	20	mV_{DC}
Output Current — Source	$V_{IN^+} = 1.0V_{DC}$, $V_{IN^-} = 0V_{DC}$, $V^+ = 15V_{DC}$	10	20		10	20		10	20		10	20		10	20		mA
Output Current — Sink	$V_{IN^-} = 1.0V_{DC}$, $V_{IN^+} = 0V_{DC}$, $V^+ = 15V_{DC}$	10	15		5.0	8.0		5.0	8.0		5.0	8.0		5.0	8.0		mA
Differential Input Voltage	Note 7			V^+			V^+			V^+			V^+			V^+	V_{DC}

6

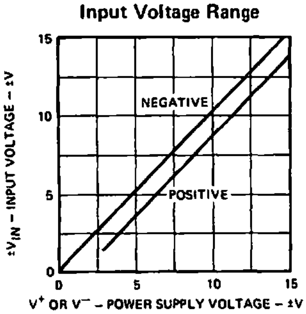
Notes:
1. For operating at high temperatures, the Am324 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The Am224 and Am124 can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers – use external resistors, where possible to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.
2. Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V.
4. These specifications apply for $V^+ = +5V_{DC}$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the Am224, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and the Am324 temperature specifications are limited to $0°C \leq T_A \leq +70°C$.
5. $V_O \cong 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ −1.5V).
6. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
7. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ −1.5V, but either or both inputs can go to +32V without damage.
8. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive coupling increases at higher frequencies.

MAXIMUM RATINGS (Above which the useful life may be impaired)

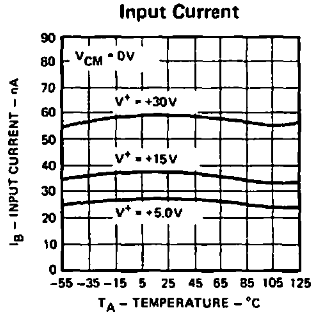
Supply Voltage, V^+	32V or ±16V
Differential Input Voltage	32V
Input Voltage	−0.3V to +32V
Power Dissipation (Note 1)	
Molded DIP	570mW
Cavity DIP	900mW
Flat Pak (Am124F)	800mW
Output Short Circuit to GND (Note 2)	
(One Amplifier) $V^+ \leqslant 15V$ and $T_A = 25°C$	Continuous
Input Current ($V_{IN} < -0.3V_{OL}$) (Note 3)	50mA
Operating Temperature Range	
Am324/Am324A	0°C to +70°C
Am224/Am224A	−25°C to +85°C
Am124/Am124A	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

TYPICAL PERFORMANCE CURVES

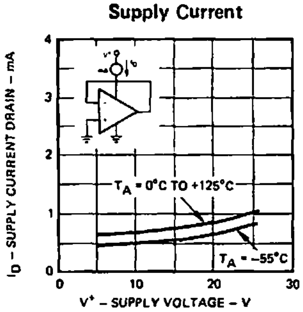
Input Voltage Range



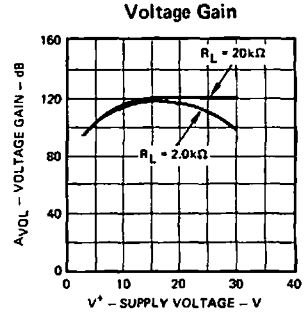
Input Current



Supply Current



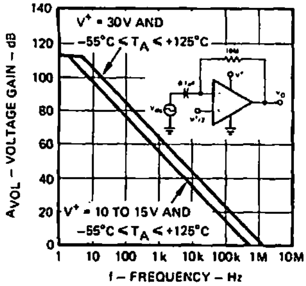
Voltage Gain



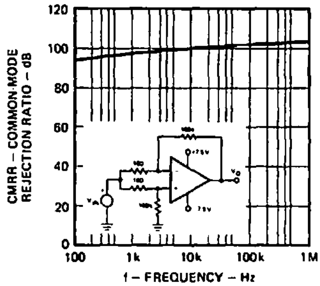
LIC-710

TYPICAL PERFORMANCE CURVES (Cont.)

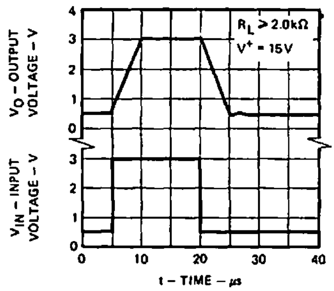
Open Loop Frequency Response



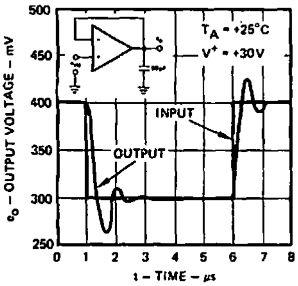
Common-Mode Rejection Ratio



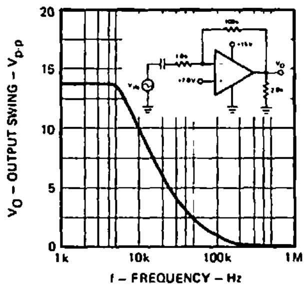
Voltage Follower Pulse Response



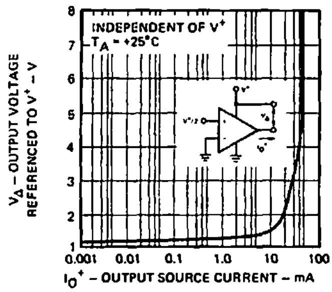
Voltage Follower Pulse Response (Small Signal)



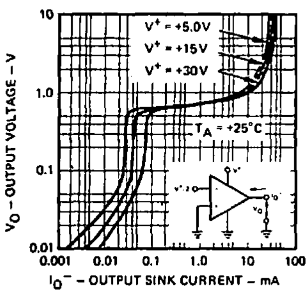
Large Signal Frequency Response



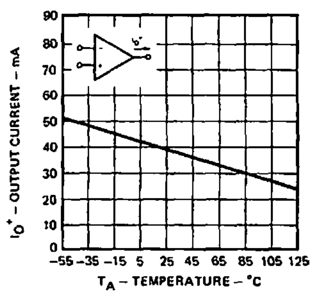
Output Characteristics Current Sourcing



Output Characteristics Current Sinking

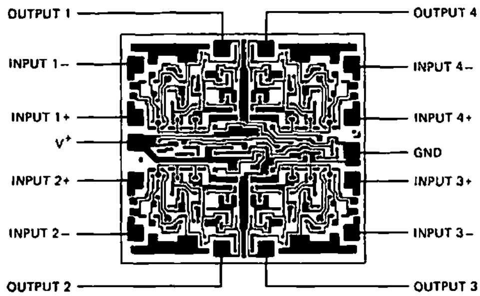


Current Limiting



LIC-711

Metallization and Pad Layout



58 x 63 MILS

APPLICATION INFORMATION

The Am124 series are op amps primarily operating from a single power supply voltage and have true-differential inputs remaining in the linear mode with an input common-mode voltage of 0V. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. The bias network of the amplifier establishes a drain current independent of the magnitude of the power supply voltage over the range of from 3V to 30V.

The pin configuration is designed to simplify PC board layouts. Since the amplifier outputs are placed at the corners of the package (pins 1, 7, 8, and 14) and are adjacent to the inverting inputs.

Extra care should be taken to insure that the power for the circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket. This prevents a possible fusing of the internal conductors and becoming a destroyed unit which could occur from the unlimited current surge through the resulting forward diode within the IC.

The use of input differential voltage protection diodes is not needed since large differential voltages can be readily applied resulting in no large input currents. The differential input voltage may be larger than V^+ without damaging the device. Protection, such as an input clamp diode with a resistor to the IC input terminal, should be provided to prevent the input voltages from going negative more than –0.3V (at 25°C).

The amplifiers contain a class A output stage for small signal levels which converts to class B in a large signal mode, to reduce the power supply current drain. Since this allows the amplifiers to both source and sink large output currents, both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to rise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For AC coupled applications crossover distortion can be minimized by utilizing a resistor from the output of the amplifier to ground. However, in DC applications, where the load is directly coupled, there is no crossover distortion.

To maintain resistance to destruction, output short circuits either to ground or to the positive power supply should be restricted to short time durations. The possibility of destruction exists, not as a result of the short circuit current metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short circuits on more than one amplifier at a time increases the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see section on typical performance characteristics) than a standard IC op amp.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50pF can be accomodated using the worst case noninverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

The series, as presented in the section on typical applications, emphasize operations on only a single power supply voltage. Yet, if complementary power supplies are available, all of the standard op amp circuits can be implemented. A unique feature in introducing a pseudo-ground (a bias voltage reference of $V^+/2$) is allowing operation above and below this value in single power supply systems. In most cases, input biasing is not required and input voltages which range to ground can be easily accomodated.

Am148 • Am149

Quad 741 Operational Amplifiers

Distinctive Characteristics

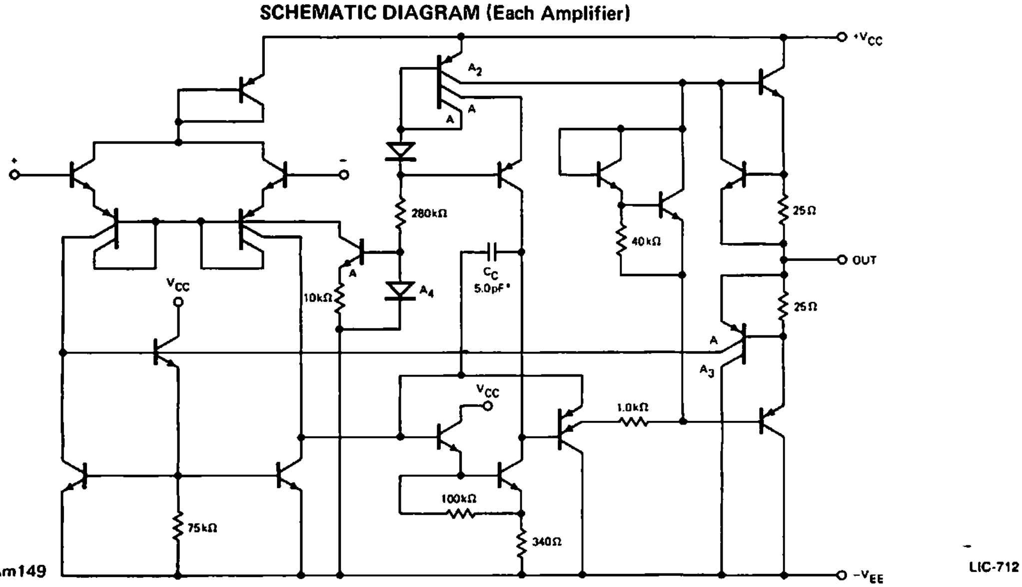
- 741 op amp operating characteristics
- Low supply current drain – 0.6mA/amplifier
- Class AB output state – no crossover distortion
- Pin compatible with the Am124
- Low input offset voltage – 1.0mV
- Low input offset current – 4.0nA
- Low input bias current – 30nA
- Gain bandwidth product
  Am148 (unity gain) – 1.0MHz
  Am149 ($A_V \geqslant 5$) – 4.0MHz
- High degree of isolation between amplifiers – 120dB
- Overload protection for inputs and outputs

FUNCTIONAL DESCRIPTION

The Am148 series is a true quad 741. It consists of four independent, high gain, internally compensated, low-power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling. The Am149 series has the same features as the Am148 plus a gain bandwidth product of 4.0MHz at a gain of 5.0 or greater.

The Am148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

SCHEMATIC DIAGRAM (Each Amplifier)



*1.0pF on the Am149

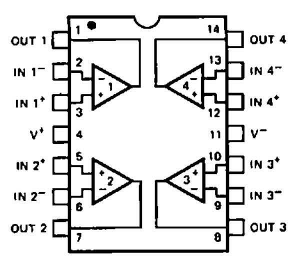
LIC-712

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am348	Hermetic DIP	0°C to +70°C	LM348D
	Molded DIP	0°C to +70°C	LM348N
	Dice	0°C to +70°C	LD348
Am248	Hermetic DIP	−25°C to +85°C	LM248D
Am148	Hermetic DIP	−55°C to +125°C	LM148D
	Dice	−55°C to +125°C	LD148
Am349	Hermetic DIP	0°C to +70°C	LM349D
	Molded DIP	0°C to +70°C	LM349N
	Dice	0°C to +70°C	LD349
Am249	Hermetic DIP	−25°C to +85°C	LM249D
Am149	Hermetic DIP	−55°C to +125°C	LM149D
	Dice	−55°C to +125°C	LD149

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

LIC-713

6

ABSOLUTE MAXIMUM RATINGS

	Am148/Am149	Am248/Am249	Am348/Am349
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage	±44V	±36V	±36V
Input Voltage	±22V	±18V	±18V
Output Short Circuit Duration (Note 1)	Continuous	Continuous	Continuous
Power Dissipation (P_d at 25°C) and Thermal Resistance (θ_{jA}), (Note 2)			
Molded DIP (N) – P_d		570mW	500mW
– θ_{jA}		150°C/W	150°C/W
Cavity DIP (D) (J) – P_d	900mW	900mW	900mW
– θ_{jA}	100°C/W	100°C/W	100°C/W
Maximum Junction Temperature ($T_{jmax.}$)	150°C	110°C	100°C
Operating Temperature Range	$-55°C \leq T_A \leq +125°C$	$-25°C \leq T_A \leq +85°C$	$0°C \leq T_A \leq +70°C$
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C	300°C	300°C

See Am741 for Typical Performance Characteristics.

ELECTRICAL CHARACTERISTICS (Note 3)

Parameters	Conditions		Am148/Am149 Min.	Typ.	Max.	Am248/Am249 Min.	Typ.	Max.	Am348/Am349 Min.	Typ.	Max.	Units
Input Offset Voltage	T_A = 25°C, $R_S \leq 10k\Omega$			1.0	5.0		1.0	6.0		1.0	6.0	mV
Input Offset Current	T_A = 25°C			4.0	25		4.0	50		4.0	50	nA
Input Bias Current	T_A = 25°C			30	100		30	200		30	200	nA
Input Resistance	T_A = 25°C		0.8	2.5		0.8	2.5		0.8	2.5		MΩ
Supply Current All Amplifiers	T_A = 25°C, V_S = ±15V			2.4	3.6		2.4	4.5		2.4	4.5	mA
Large Signal Voltage Gain	T_A = 25°C, V_S = ±15V V_{OUT} = ±10V, R_L > 2.0kΩ		50	160		25	160		25	160		V/mV
Amplifier to Amplifier Coupling	T_A = 25°C, f = 1.0Hz to 20kHz (Input Referred)			−120			−120			−120		dB
Small Signal Bandwidth	T_A = 25°C	Am148 Series		1.0			1.0			1.0		MHz
		Am149 Series		4.0			4.0			4.0		
Phase Margin	T_A = 25°C	Am148 Series (A_V = 1)		60			60			60		degrees
		Am149 Series (A_V = 5)		60			60			60		
Slew Rate	T_A = 25°C	Am148 Series (A_V = 1)		0.5			0.5			0.5		V/µs
		Am149 Series (A_V = 5)		2.0			2.0			2.0		
Output Short Circuit Current	T_A = 25°C			25			25			25		mA
Input Offset Voltage	$R_S \leq 10k\Omega$				6.0			7.5			7.5	mV
Input Offset Current					75			125			100	nA
Input Bias Current					325			500			400	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, R_L > 2.0kΩ		25			15			15			V/mV
Output Voltage Swing	V_S = ±15V	R_L = 10kΩ	±12	±13		±12	±13		±12	±13		V
		R_L = 2.0kΩ	±10	±12		±10	±12		±10	±12		
Input Voltage Range	V_S = ±15V		±12			±12			±12			V
Common-Mode Rejection Ratio	$R_S \leq 10k\Omega$		70	90		70	90		70	90		dB
Supply Voltage Rejection	$R_S \leq 10k\Omega$		77	96		77	96		77	96		dB

Notes:
1. Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
2. The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by $T_{jmax.}$, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jmax.} - T_A)/\theta_{jA}$ or the 25°C $P_{dmax.}$, whichever is less. Derate Dual In-Line package at 9mW/°C for operation at ambient temperatures above 95°C.
3. These specifications apply for V_S = ±15V and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted.
4. For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

LF155/LF156/LF157

Monolithic JFET Input Operational Amplifiers

DISTINCTIVE CHARACTERISTICS

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance — very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000pF) without stability problems
- Internal compensation and large differential input voltage capability

GENERAL DESCRIPTION

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

The LF155, LF156, LF157 series are direct replacements for National LF155, LF156, LF157 series.

COMMON FEATURES
(LF155A, LF156A, LF157A)

Low input bias current	30pA
Low input offset current	3.0pA
High input impedance	$10^{12}\Omega$
Low input offset voltage	1.0mV
Low input offset voltage temperature drift	3.0μV/°C
Low input noise current	0.01pA/$\sqrt{Hz}$
High common-mode rejection ratio	100dB
Large dc voltage gain	106dB

APPLICATIONS

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

UNCOMMON FEATURES

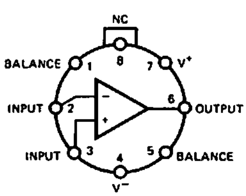
	LF155A	LF156A	LF157A (A_V = 5)	Units
Extremely fast settling time to 0.01%	4.0	1.5	1.5	μs
Fast slew rate	5.0	12	50	V/μs
Wide gain bandwidth	2.5	5.0	20	MHz
Low input noise voltage	20	12	12	nV/$\sqrt{Hz}$

ORDERING INFORMATION

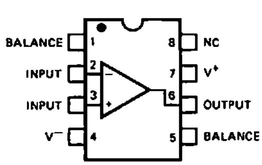
Part Number	Package Type	Temperature Range	Order Number
LF355	Metal Can	0°C to +70°C	LF355H
	Molded DIP	0°C to +70°C	LF355N
	Dice	0°C to +70°C	LD355
LF255	Metal Can	−25°C to +85°C	LF255H
LF155	Metal Can	−55°C to +125°C	LF155H
	Dice	−55°C to +125°C	LD155
LF355A	Metal Can	0°C to +70°C	LF355AH
	Dice	0°C to +70°C	LD355A
LF155A	Metal Can	−55°C to +125°C	LF155AH
	Dice	−55°C to +125°C	LD155A
LF356	Metal Can	0°C to +70°C	LF356H
	Molded DIP	0°C to +70°C	LF356N
	Dice	0°C to +70°C	LD356
LF256	Metal Can	−25°C to +85°C	LF256H
LF156	Metal Can	−55°C to +125°C	LF156H
	Dice	−55°C to +125°C	LD156
LF356A	Metal Can	0°C to +70°C	LF356AH
	Dice	0°C to +70°C	LD356A
LF156A	Metal Can	−55°C to +125°C	LF156AH
	Dice	−55°C to +125°C	LD156A
LF357	Metal Can	0°C to +70°C	LF357H
	Molded DIP	0°C to +70°C	LF357N
	Dice	0°C to +70°C	LD357
LF257	Metal Can	−25°C to +85°C	LF257H
LF157	Metal Can	−55°C to +125°C	LF157H
	Dice	−55°C to +125°C	LD157
LF357A	Metal Can	0°C to +70°C	LF357AH
	Dice	0°C to +70°C	LD357A
LF157A	Metal Can	−55°C to +125°C	LF157AH
	Dice	−55°C to +125°C	LD157A

CONNECTION DIAGRAMS
Top Views

Metal Can



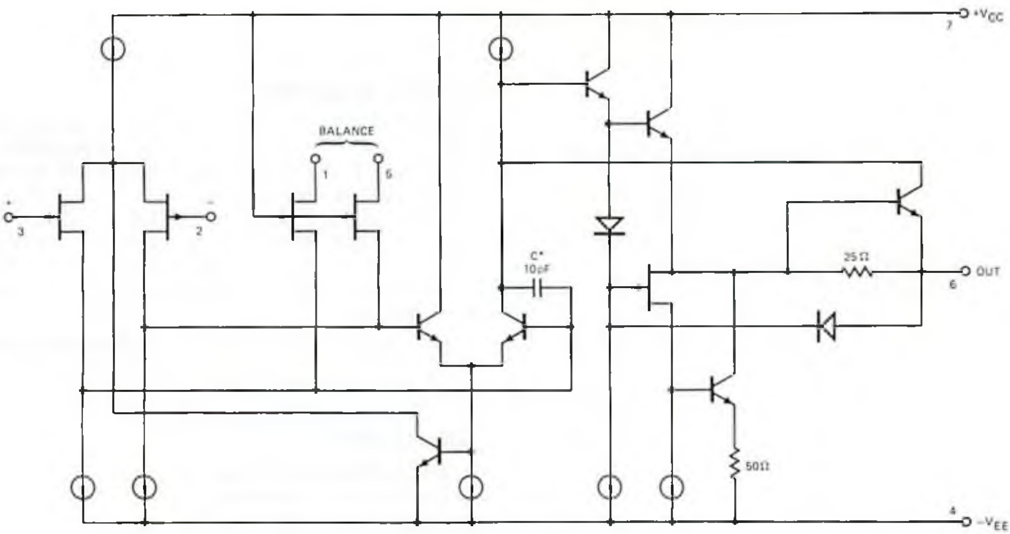
Dual-In-Line



Notes: 1. On Dual-In-Line Pin 1 is marked for orientation.
2. On Metal Can Pin 4 is connected to case.

LIC-714

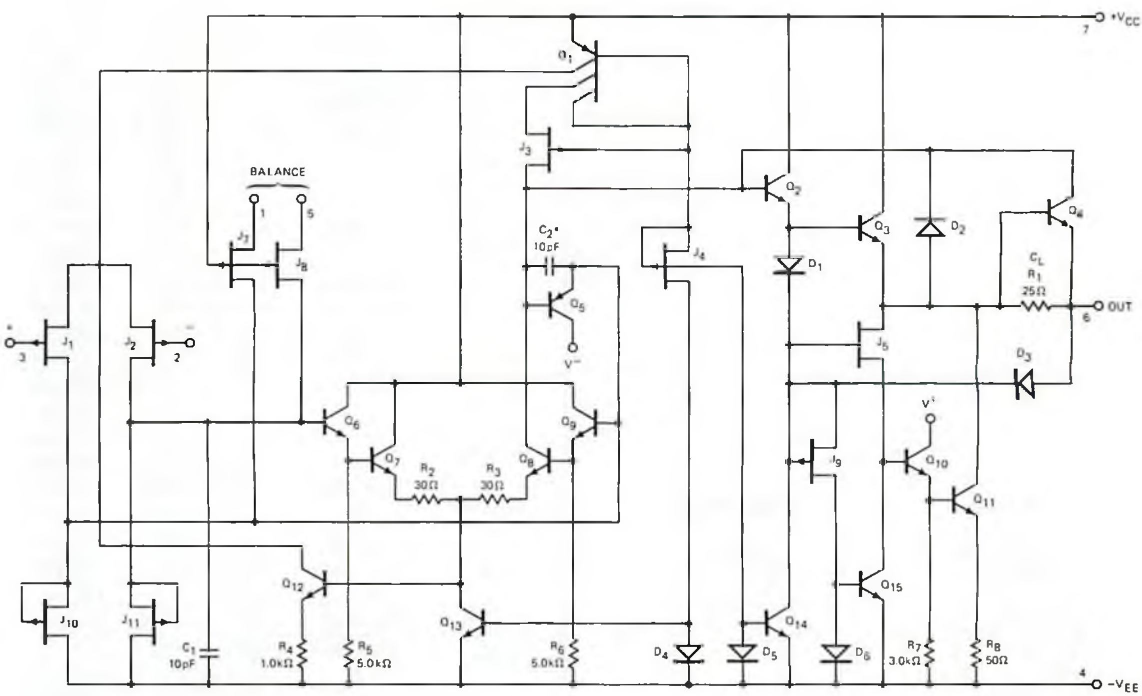
SIMPLIFIED SCHEMATIC



*C = 2pF on LF157

LIC-715

DETAILED SCHEMATIC



*C = 2pF on LF157

LIC-716

ABSOLUTE MAXIMUM RATINGS

	LF155A/6A/7A	LF155/6/7	LF255/6/7	LF355A/6A/7A LF355/6/7
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (Note 1) TO-99 (H Package)	670mW	670mW	570mW	500mW
Operating Temperature Range	−55°C to +125°C	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
T_J(Max.)	150°C	150°C	115°C	100°C
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continous	Continuous	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Note 3)

DC CHARACTERISTICS

Parameters	Description	Test Conditions	LF155A/6A/7A Min.	LF155A/6A/7A Typ.	LF155A/6A/7A Max.	LF355A/6A/7A Min.	LF355A/6A/7A Typ.	LF355A/6A/7A Max.	Units
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		1.0	2.0		1.0	2.0	mV
		Over Temperature			2.5			2.3	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3.0	5.0		3.0	5.0	μV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		μV/°C per mV
I_{OS}	Input Offset Current	$T_J = 25°C$, (Note 3, 5)		3.0	10		3.0	10	pA
		$T_J < T_{HIGH}$			10			1.0	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	50		30	50	pA
		$T_J < T_{HIGH}$			25			5.0	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$	50	200		50	200		V/mV
		$V_O = \pm10V$, $R_L = 2k\Omega$ Over Temperature	25			25			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k\Omega$	±12	±13		±12	±13		Volts
		$V_S = \pm15V$, $R_L = 2k\Omega$	±10	±12		±10	±12		Volts
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15.1 −12		±11	+15.1 −12		Volts
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

AC CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm15V$)

Parameters	Description	Test Conditions	LF155A/355A Min.	LF155A/355A Typ.	LF155A/355A Max.	LF156A/356A Min.	LF156A/356A Typ.	LF156A/356A Max.	LF157A/357A Min.	LF157A/357A Typ.	LF157A/357A Max.	Units
SR	Slew Rate	LF155A/6A: $A_V = 1$	3.0	5.0		10	12					V/μs
		LF157A: $A_V = 5$							40	50		V/μs
GBW	Gain-Bandwidth Product			2.5		4.0	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4.0			1.5			1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100Hz		25			15			15		$nV/\sqrt{Hz}$
		f = 1000Hz		20			12			12		
i_n	Equivalent Input Noise Current	f = 100Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
		f = 1000Hz		0.01			0.01			0.01		
C_{IN}	Input Capacitance			3.0			3.0			3.0		pF

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

DC CHARACTERISTICS (Note 3)

Parameters	Description	Test Conditions	LF155/6/7 Min.	LF155/6/7 Typ.	LF155/6/7 Max.	LF255/6/7 Min.	LF255/6/7 Typ.	LF255/6/7 Max.	LF355/6/7 Min.	LF355/6/7 Typ.	LF355/6/7 Max.	Units
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		3.0	5.0		3.0	5.0		3.0	10	mV
		Over Temperature			7.0			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5.0			5.0			5.0		$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		$\mu V/°C$ per mV
I_{OS}	Input Offset Current	$T_J = 25°C$, (Notes 3, 5)		3.0	20		3.0	20		3.0	50	pA
		$T_J \le T_{HIGH}$			20			1.0			2.0	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	100		30	100		30	200	pA
		$T_J \le T_{HIGH}$			50			5.0			8.0	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$	50	200		50	200		25	200		V/mV
		$V_O = \pm 10V$, $R_L = 2k\Omega$ Over Temperature	25			25			15			
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	±12	±13		±12	±13		±12	±13		Volts
		$V_S = \pm 15V$, $R_L = 2k\Omega$	±10	±12		±10	±12		±10	±12		
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15.1 −12			+15.1 −12		±11	+15.1 −12		Volts
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm 15V$)

Parameters	LF155A/355A LF155/255 Typ.	LF155A/355A LF155/255 Max.	LF355 Typ.	LF355 Max.	LF156A LF156/256 Typ.	LF156A LF156/256 Max.	LF356A/356 Typ.	LF356A/356 Max.	LF157A LF157/257 Typ.	LF157A LF157/257 Max.	LF357A/357 Typ.	LF357A/357 Max.	Units
Supply Current	2.0	4.0	2.0	4.0	5.0	7.0	5.0	10	5.0	7.0	5.0	10	mA

AC CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm 15V$)

Parameters	Description	Test Conditions	LF155/255/ LF355 Typ.	LF156/256 Min.	LF156/256/ LF356 Typ.	LF157/257 Min.	LF157/257 LF357 Typ.	Units
SR	Slew Rate	LF155/6: $A_V = 1$,	5.0	7.5	12			V/µs
		LF157: $A_V = 5$				30	50	V/µs
GBW	Gain-Bandwidth Product		2.5		5.0		20	MHz
t_s	Settling Time fo 0.01%	(Note 7)	4.0		1.5		1.5	µs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100Hz	25		15		15	$nV/\sqrt{Hz}$
		f = 1000Hz	20		12		12	
i_n	Equivalent Input Noise Current	f = 100Hz	0.01		0.01		0.01	$pA/\sqrt{Hz}$
		f = 1000Hz	0.01		0.01		0.01	
C_{IN}	Input Capacitance		3.0		3.0		3.0	pF

Notes: 1. The TO-99 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case; for the DIP package, the device must be derated based on thermal resistance of 175°C/W junction to ambient.

2. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

3. These specifications apply for $\pm 15V \le V_S \le \pm 20V$, $-55°C \le T_A \le +125°C$ and $T_{HIGH} = +125°C$ unless otherwise stated for the LF155A/6A/7A and the LF155/6/7. For the LF255/6/7, these specifications apply for $\pm 15V \le V_S \le \pm 20V$, $-25°C \le T_A \le +85°C$ and $T_{HIGH} = 85°C$ unless otherwise stated. For the LF355A/6A/7A, these specifications apply for $\pm 15V \le V_S \le \pm 20V$, $0°C \le T_A \le +70°C$ and $T_{HIGH} = +70°C$, and for the LF355/6/7 these specifications apply for $V_S = \pm 15V$ and $0°C \le T_A \le +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

4. The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5µV/°C) typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

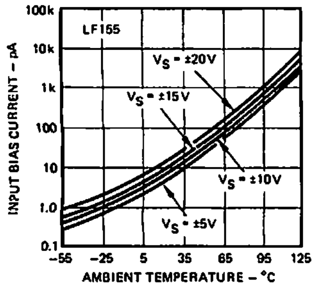
5. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta_{jA} Pd$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

6. Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

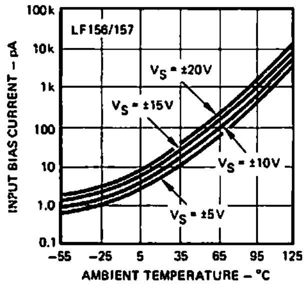
7. Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2kΩ and the output step is 10V (See Settling Time Test Circuit, page 9).

TYPICAL DC PERFORMANCE CHARACTERISTICS

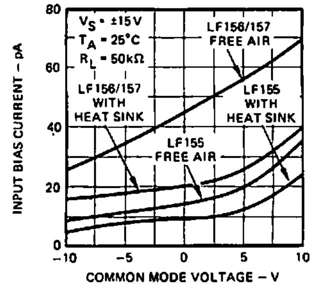
Input Bias Current



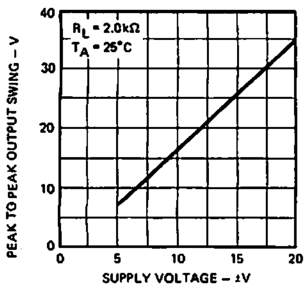
Input Bias Current



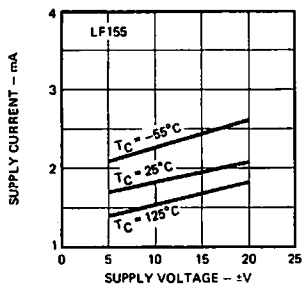
Input Bias Current



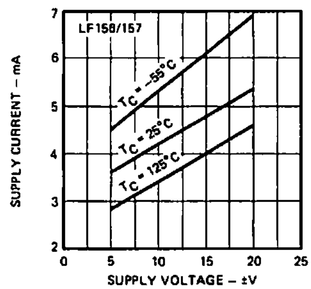
Voltage Swing



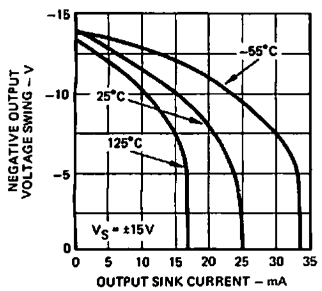
Supply Current



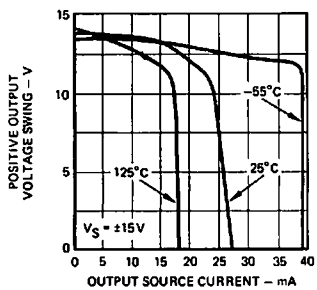
Supply Current



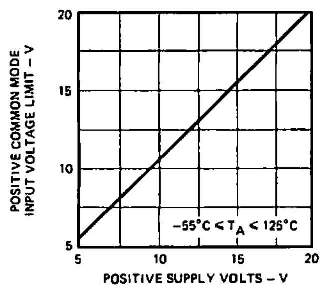
Negative Current Limit



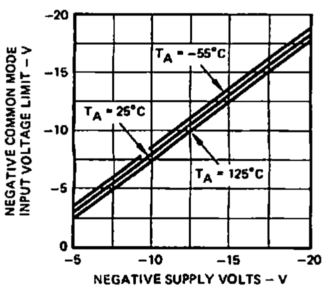
Positive Current Limit



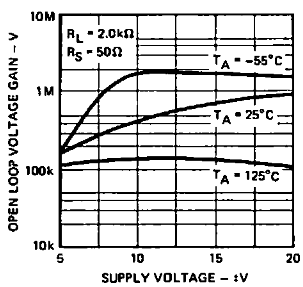
Positive Common-Mode Input Voltage Limit



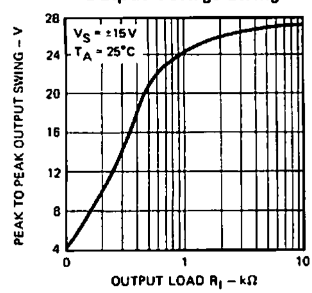
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain



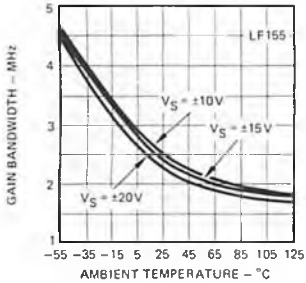
Output Voltage Swing

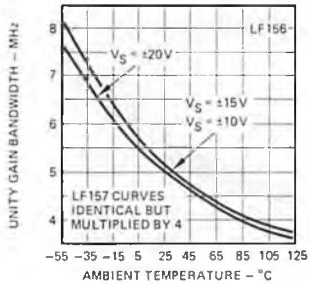


LIC-717

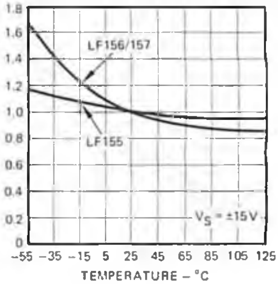
TYPICAL AC PERFORMANCE CHARACTERISTICS

Gain Bandwidth

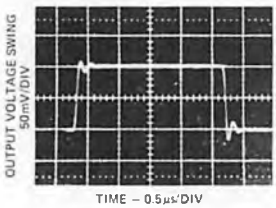




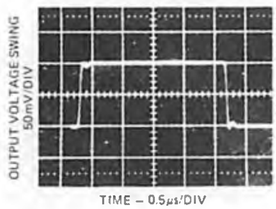
Normalized Slew Rate



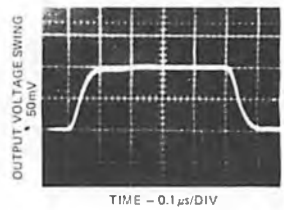
LF155 Small Signal Pulse Response, A_V = +1



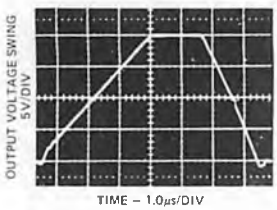
LF156 Small Signal Pulse Response, A_V = +1



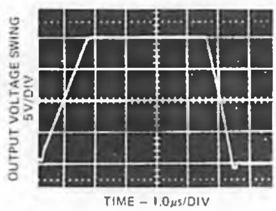
LF157 Small Signal Pulse Response, A_V = +5



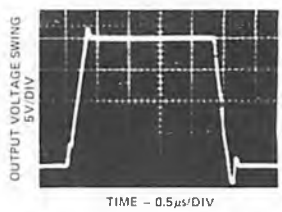
LF155 Large Signal Pulse Response, A_V = +1



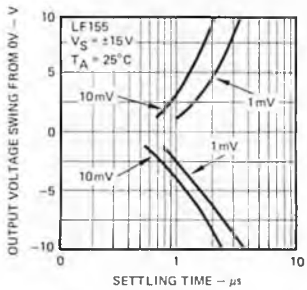
LF156 Large Signal Pulse Response, A_V = +1



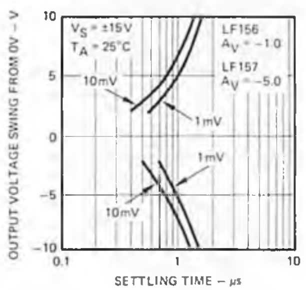
LF157 Large Signal Pulse Response, A_V = +5



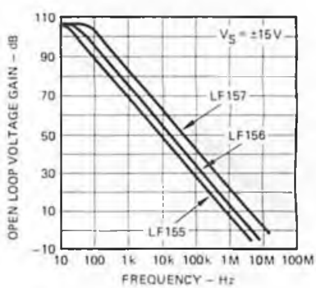
Inverter Settling Time



Inverter Settling Time



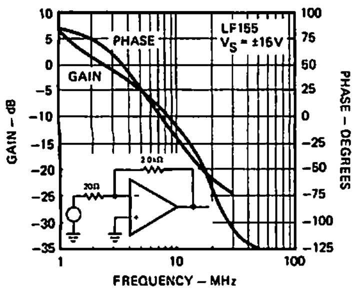
Open Loop Frequency Response



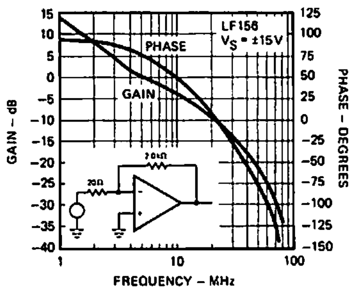
LIC-718

TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont.)

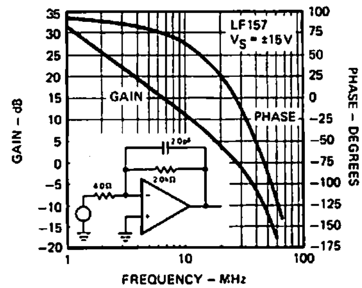
Bode Plot



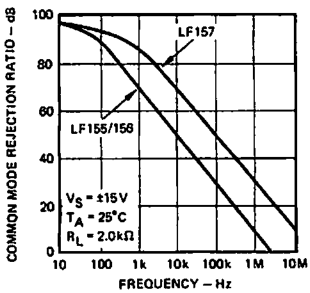
Bode Plot



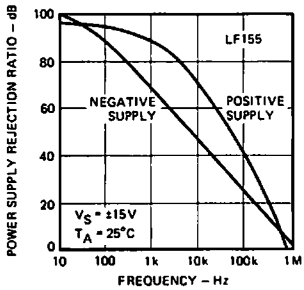
Bode Plot



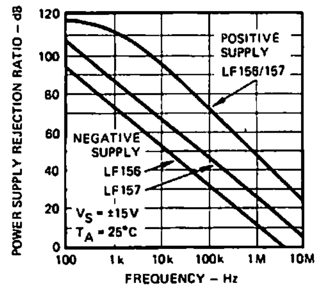
Common-Mode Rejection Ratio



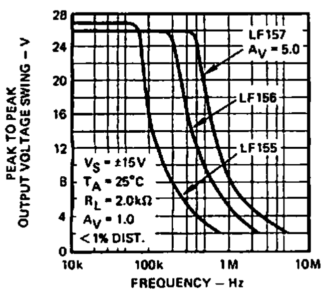
Power Supply Rejection Ratio



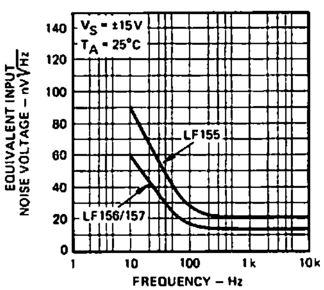
Power Supply Rejection Ratio



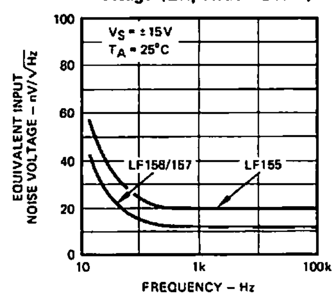
Undistorted Output Voltage Swing



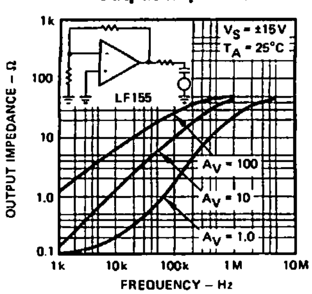
Equivalent Input Noise Voltage



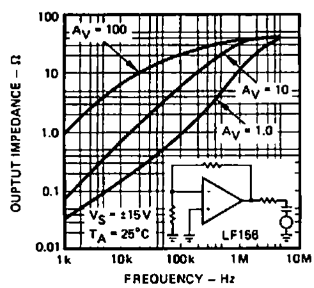
Equivalent Input Noise Voltage (Expanded Scale)



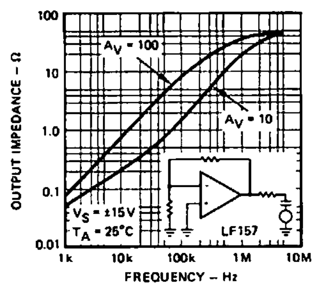
Output Impedance



Output Impedance



Output Impedance



LIC-719

APPLICATION HINTS

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

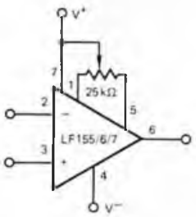
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

TYPICAL CIRCUIT CONNECTIONS AND PAD LAYOUT

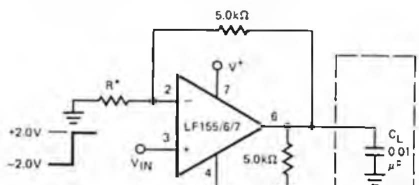
V_{OS} Adjustment



LIC-720

V_{OS} is adjusted with a 25k potentiometer.
The potentiometer wiper is connected to V^+

Driving Capacitive Loads

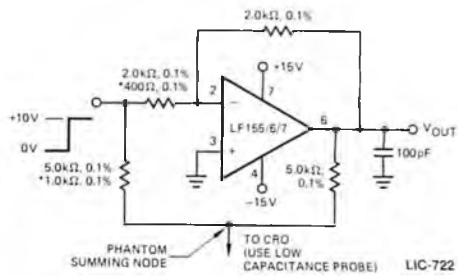


*R = 5.0kΩ (LF155/156)
*R = 1.25kΩ (LF157)

LIC-721

Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability.
C_L Max. ≥ 0.01 µF
Overshoot ≤ 20%
Settling time (t_s) ≥ 5.0µs

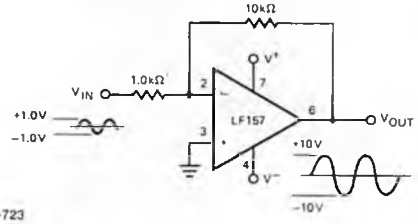
Settling Time Test Circuit



LIC-722

Settling time is tested with the LF155/156 connected as unity gain converter and LF157 connected for A_V = −5.0
Output = 10V step
*A_V = −5.0 for LF157

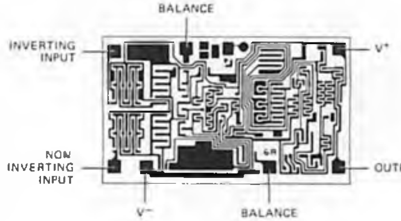
A Large Power BW Amplifier (LF157)



LIC-723

For distortion ≤ 1% and a 20Vp-p V_{OUT} swing, power bandwidth is: 500kHz.

Metallization and Pad Layout



75 x 45 Mils

Am216/316·Am216A/316A

Compensated, High-Performance Operational Amplifier

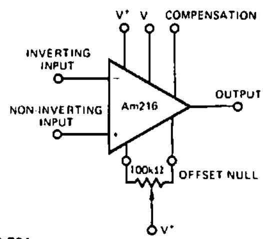
Distinctive Characteristics

- The Am216/Am216A/Am316/Am316A are functionally, electrically, and pin-for-pin equivalent to the National LM216/LM216A/LM316/LM316A.
- Low input bias currents: 50pA
- Low input offset currents: 15pA
- Low power consumption: 3mW
- Internal frequency compensation
- Offset nulling provisions
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically and optically inspected dice for assemblers of hybrid products.
- Available in metal can, hermetic dual-in-line and flat packages.

FUNCTIONAL DESCRIPTION

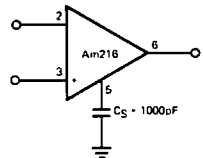
The Am216/Am216A/Am316/Am316A are compensated high performance operational amplifiers featuring extremely low input-current errors. High input impedance achieved using supergain transistors in a Darlington input stage produces input bias currents that are equal to high quality FET amplifiers. These devices are internally frequency compensated and provision is made for offset adjustment with a single potentiometer.

FUNCTIONAL DIAGRAM



LIC-724

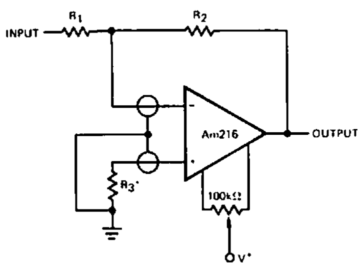
Overcompensation for Greater Stability Margin



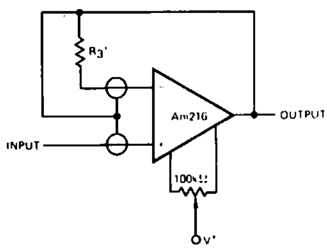
LIC-725

TYPICAL APPLICATIONS

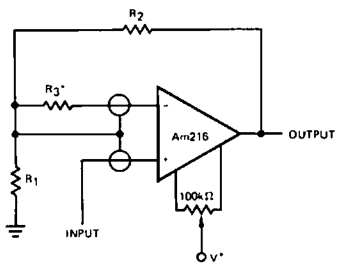
Connection of Input Guards and Offset Null



Inverting Amplifier



Follower



Non-Inverting Amplifier

*Use to compensate for large source resistances.

NOTE: $\frac{R_1R_2}{R_1+R_2}$ Must be LOW impedance

LIC-726 LIC-727 LIC-728

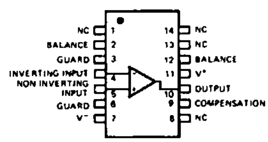
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am316	DIP	0°C to +70°C	LM316D
	Metal Can	0°C to +70°C	LM316H
	Flat Pak	0°C to +70°C	LM316F
	Dice	0°C to +70°C	LD316
Am361A	DIP	0°C to +70°C	LM316AD
	Metal Can	0°C to +70°C	LM316AH
	Flat Pak	0°C to +70°C	LM316AF
	Dice	0°C to +70°C	LD316A
Am216	DIP	–25°C to +85°C	LM216D
	Metal Can	–25°C to +85°C	LM216H
	Flat Pak	–25°C to +85°C	LM216F
	Dice	–25°C to +85°C	LD216
Am216A	DIP	–25°C to +85°C	LM216AD
	Metal Can	–25°C to +85°C	LM216AH
	Flat Pak	–25°C to +85°C	LM216AF
	Dice	–25°C to +85°C	LD216A

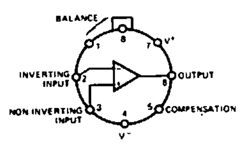
CONNECTION DIAGRAMS

Top Views

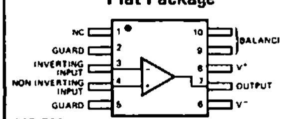
Dual-In-Line



Metal Can



Flat Package



LIC-729

Notes:
(1) On Metal Can, pin 4 is connected to case.
(2) On DIP, pin 7 is connected to bottom of package.
(3) On Flat Package, pin 6 is connected to bottom of package. Compensation terminal is not brought out on the flat package.

6

MAXIMUM RATINGS

Supply Voltage	±20 V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15 V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am216/Am216A	−25°C to 85°C
Am316/Am316A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

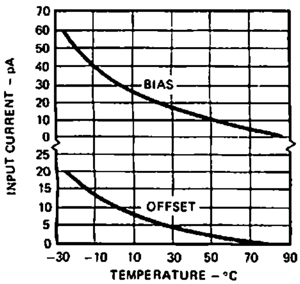
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

Parameter (see definitions)	Conditions	Am216	Am216A	Am316	Am316A	Units
Input Offset Voltage		10	3	10	3	mV
Input Offset Current		50	15	50	15	pA
Input Bias Current		150	50	150	50	pA
Input Resistance		1	5	1	5	GΩ
Supply Current		0.8	0.6	0.8	0.6	mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V R_L > 10kΩ	20	40	20	40	V/mV
The Following Specifications Apply Over The Operating Temperature Ranges						
Input Offset Voltage		15	6	15	6	mV
Input Offset Current		100	30	100	30	pA
Input Bias Current		250	100	250	100	pA
Supply Current	$T_A = T_{MAX.}$		0.5		0.5	mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V R_L > 10kΩ	10	20	15	30	V/mV
Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±13	±13	±13	±13	V
Input Voltage Range	V_S = ±15V	±13	±13	±13	±13	V
Common Mode Rejection Ratio		80	80	80	80	dB
Supply Voltage Rejection Ratio		80	80	80	80	dB

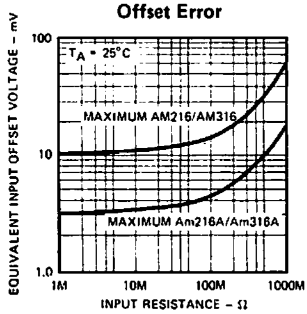
Notes:
1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual-In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
4. Unless otherwise specified, these specifications apply for supply voltages from ±5 V to ±20 V.

TYPICAL PERFORMANCE CHARACTERISTICS

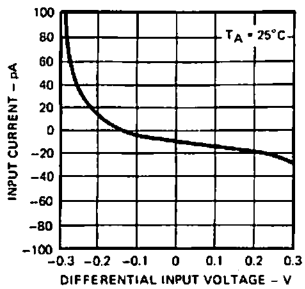
Input Currents



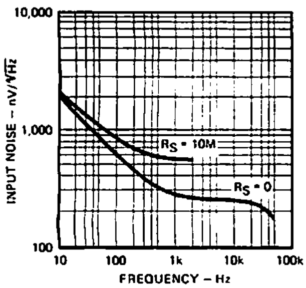
Offset Error



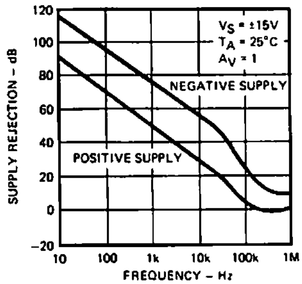
Input Current



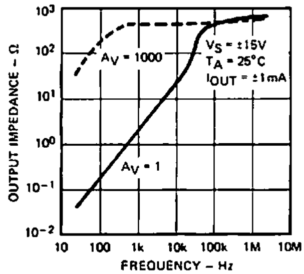
Input Noise Voltage



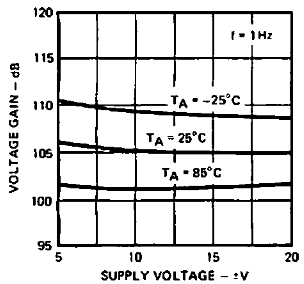
Power Supply Rejection



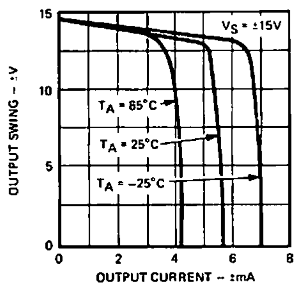
Closed Loop Output Impedance



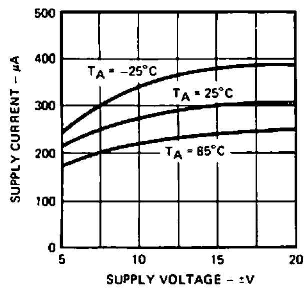
Voltage Gain



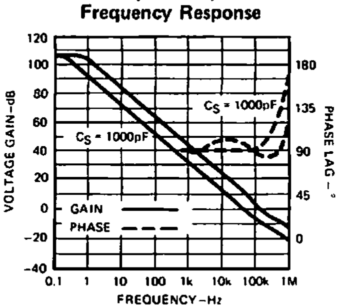
Output Swing



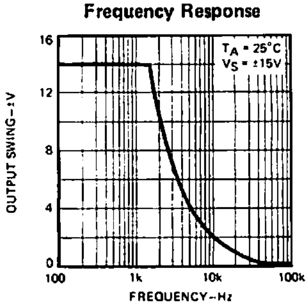
Supply Current



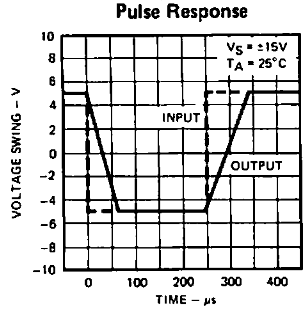
Open Loop Frequency Response



Large Signal Frequency Response



Voltage Follower Pulse Response



LIC-730

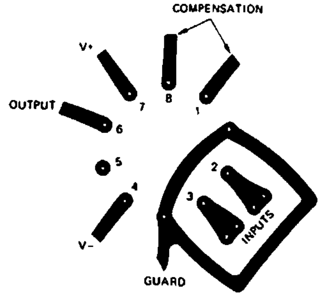
ADDITIONAL APPLICATION INFORMATION

GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the Am216 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

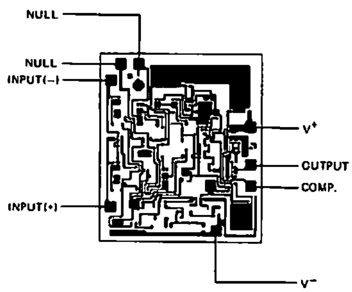
The pin configuration of the dual-in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration.)



BOTTOM VIEW

Note: Board layout for Input Guarding with TO-99 package.

Metallization and Pad Layout



62 x 72 Mils

Am715/715C

High-Speed Operational Amplifier

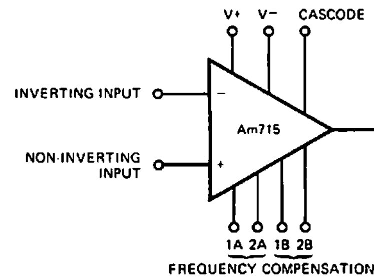
Description: The Am715 and Am715C high-speed operational amplifiers are functionally, electrically, and pin-for-pin equivalent to the Fairchild μA715 and μA715C. Both are available in the hermetic metal can, dual-in-line, and flat packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL-STD-883.
Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am is a differential input, single-ended output operational amplifier having wide bandwidth and high slew rate. It has internal lead compensation and four points for external lag compensation networks, providing many possible combinations of frequency compensation. In addition, a point is brought out for use with an external diode to prevent latch-up in voltage follower applications.

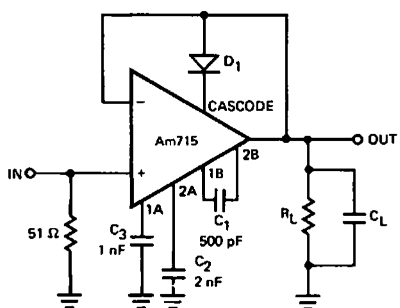
FUNCTIONAL DIAGRAM



LIC-731

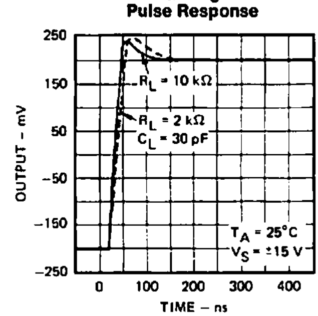
APPLICATIONS

Voltage Follower



LIC-732

Voltage Follower Small-Signal Pulse Response



LIC-733

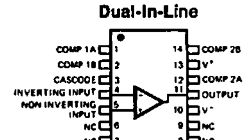
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am715C	Metal Can	0°C to +70°C	715HC
	DIP	0°C to +70°C	715DC
	Dice	0°C to +70°C	715XC
Am715	Metal Can	−55°C to +125°C	715HM
	DIP	−55°C to +125°C	715DM
	Flat Pak	−55°C to +125°C	715FM
	Dice	−55°C to +125°C	715XM

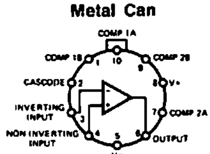
CONNECTION DIAGRAMS

Top Views

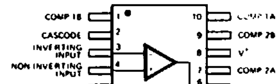
Dual-In-Line



Metal Can



Flat Package



NOTES:
(1) On Metal Can, pin 5 is connected to case.
(2) On DIP, pin 10 is connected to bottom of package
(3) On Flat Package, pin is connected to bottom of package

LIC-734

MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±6 V
Input Voltage (Note 2)	±15 V
Operating Temperature Range Am715C Am715	 0°C to +70°C −55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS ($V_S = \pm15$ V, $T_A = 25°C$ unless otherwise specified)

Parameter (see definitions)	Conditions	Am715C Min	Am715C Typ	Am715C Max	Am715 Min	Am715 Typ	Am715 Max	Units
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	7.5		2.0	5.0	mV
Input Offset Current			70	250		70	250	nA
Input Bias Current			0.4	1.5		0.4	0.75	μA
Input Resistance			1.0			1.0		MΩ
Input Voltage Range		±10	±12		±10	±12		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	74	92		74	92		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		70	400		70	300	μV/V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm10$ V	10	30		15	30		V/mV
Output Voltage Swing	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Output Resistance			75			75		Ω
Supply Current			5.5	10		5.5	7.0	mA
Power Consumption			165	300		165	210	mW
Transient Response (Voltage Follower) Risetime Overshoot	$V_{out} = \pm200$ mV, $R_L = 2$ kΩ, $C_L = 30$ pF	 	 30 30	 75 50		 30 30	 60 40	 ns %
Slew Rate	Av = 100 (Fig. 8) $V_{out} = 0$ to $+10$ V, Av = 10 (Fig. 7) $R_L = 2$ kΩ, Av = 1 (Figs. 1 & 2) $C_L = 30$ pF	 10	65 40 20		 15	65 40 20		V/μs V/μs V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10$ kΩ			10			7.5	mV
Input Offset Current	$T_A = T_{A\,max}$ $T_A = T_{A\,min}$			250 750			250 800	nA nA
Input Bias Current	$T_A = T_{A\,max}$ $T_A = T_{A\,min}$			1.5 7.5			0.75 4.0	μA μA
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	74			74			dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ			400			300	μV/V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm10$ V	8.0			10			V/mV
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			±10			V

Notes: 1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual-In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.

PERFORMANCE CURVES

Voltage Follower

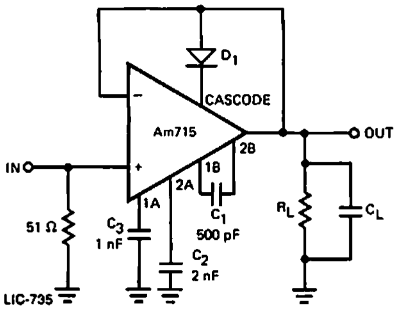


Figure 1

X1 Inverting Amplifier

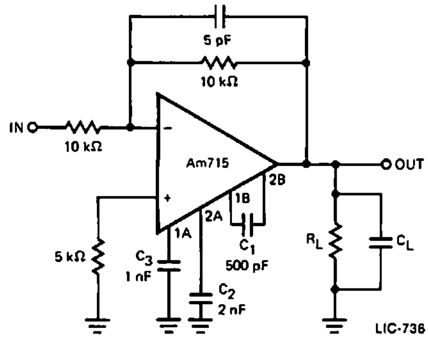
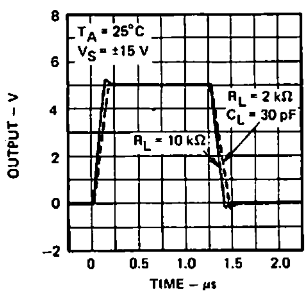


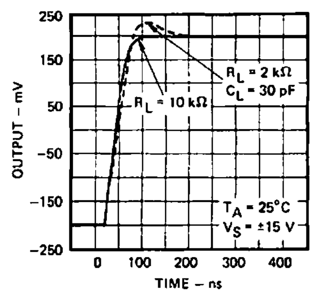
Figure 2

The high gain and large bandwidth of the Am715 make it mandatory to observe the following precautions in using the device, as is the case with any high frequency amplifier. Circuit layout should be arranged to keep all lead lengths as short as possible and the output separated from the inputs and frequency compensation pins. The values of the feedback and source impedances should be kept small to reduce the effect of stray capacitance of the inputs. The power supplies must be bypassed to ground at the supply leads of the amplifier with low inductance capacitors. Capacitive loading must be kept to an absolute minimum, since the amplifier cannot tolerate more than 30 pF directly at its output with full feedback.

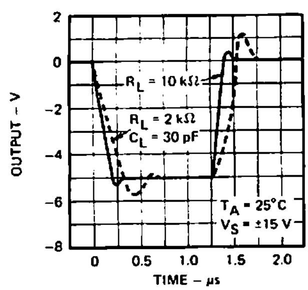
Follower & X1 Inverter Positive Large-Signal Pulse Response



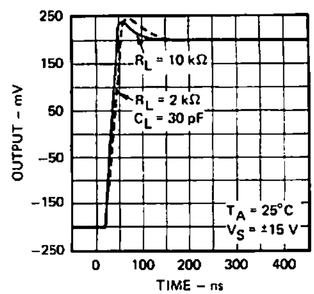
X1 Inverter Small-Signal Pulse Response



Follower & X1 Inverter Negative Large-Signal Pulse Response



Voltage Follower Small-Signal Pulse Response



LIC-737

X10 Amplifier

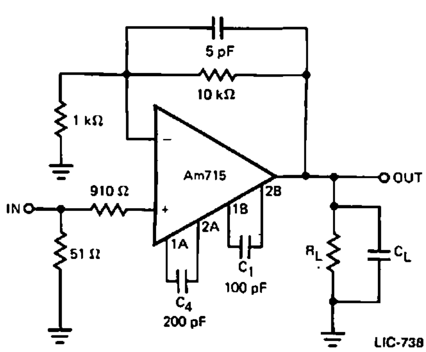


Figure 3

X100 Amplifier

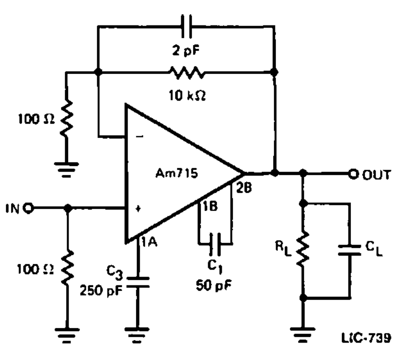
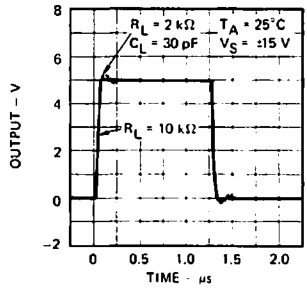


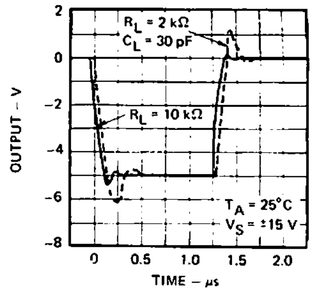
Figure 4

PERFORMANCE CURVES

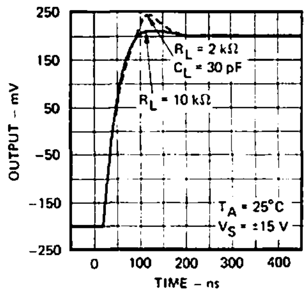
X10 Amplifier Positive Large-Signal Pulse Response



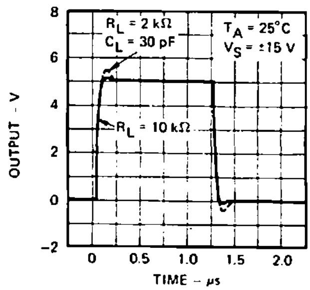
X10 Amplifier Negative Large-Signal Pulse Response



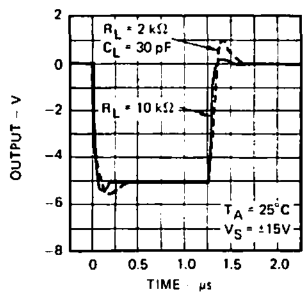
X10 Amplifier Small-Signal Pulse Response



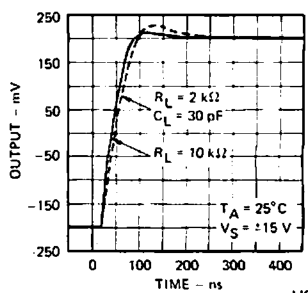
X100 Amplifier Positive Large-Signal Pulse Response



X100 Amplifier Negative Large-Signal Pulse Response

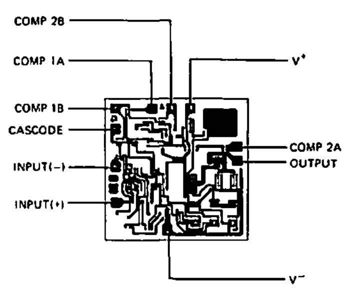


X100 Amplifier Small-Signal Pulse Response



LIC-740

Metallization and Pad Layout



62 x 62 Mils

Am725/725C

Instrumentation Operational Amplifiers

Description:

The Am725 and Am725C monolithic operational amplifiers are functionally, electrically and pin-for-pin equivalent to the Fairchild 725 and 725C. They are available in the hermetic metal can and DIP packages.

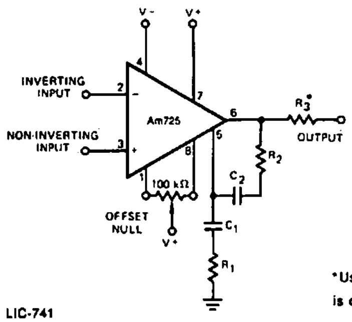
Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The 725/725C are instrumentation operational amplifiers. Device design has been optimized to provide low noise voltage, low offset voltage, low offset voltage drift and high common mode rejection. The 725 is offset voltage adjustable and is pin-for-pin compatible with the 108 and 101A amplifiers. However, additional frequency compensation components are required and should be determined by the desired closed loop gain.

FUNCTIONAL DIAGRAM



Compensation Component Values

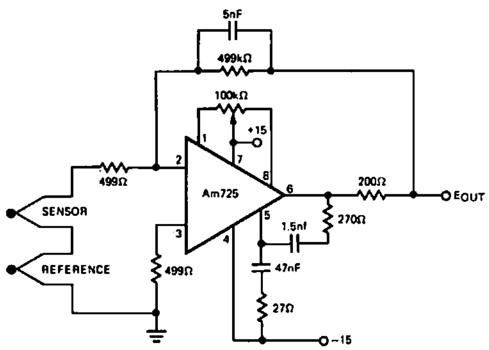
A_{VCL}	R_1 (Ω)	C_1 (nF)	R_2 (Ω)	C_2 (nF)
1000	470	1.0	—	—
100	47	10	—	—
10	27	50	270	1.5
1	10	50	39	20

*Use R_3 = 51Ω when the amplifier is operated with capacitive loads.

LIC-741

APPLICATION

Thermocouple Amplifier



LIC-742

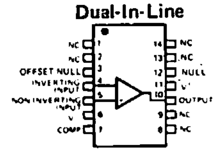
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am725C	TO-99	0°C to +70°C	725HC
	DIP	0°C to +70°C	725DC
	Molded DIP	0°C to +70°C	725CN
	Dice	0°C to +70°C	725XC
Am725	TO-99	−55°C to +125°C	725HM
	DIP	−55°C to +125°C	725DM
	Dice	−55°C to +125°C	725XM

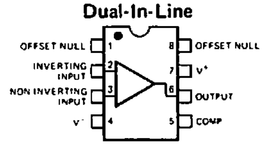
CONNECTION DIAGRAMS

Top Views

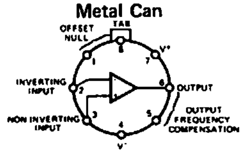
Dual-In-Line



Dual-In-Line



Metal Can



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

LIC-743

MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±5V
Input Voltage (Note 2)	±22V
Operating Temperature Range Am725 Am725C	 −55°C to +125°C 0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

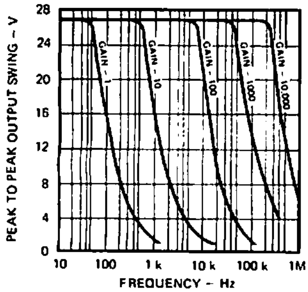
ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified)

Parameter	Test Conditions	Am725C Min	Am725C Typ	Am725C Max	Am725 Min	Am725 Typ	Am725 Max	Units
Input Offset Voltage (Without external trim)	R_S <10 kΩ		0.5	2.5		0.5	1.0	mV
Input Offset Current			3.0	35		2.0	20	nA
Input Bias Current			50	125		42	100	nA
Input Noise Voltage	f_o = 10Hz f_o = 100Hz f_o = 1kHz		15 12 8.0			15 9.0 8.0		nV/$\sqrt{Hz}$ nV/$\sqrt{Hz}$ nV/$\sqrt{Hz}$
Input Noise Current	f_o = 10Hz f_o = 100Hz f_o = 1kHz		1.0 0.8 0.6			1.0 0.3 0.15		pA/$\sqrt{Hz}$ pA/$\sqrt{Hz}$ pA/$\sqrt{Hz}$
Input Resistance			3.0			1.5		MΩ
Input Voltage Range		±13.5	±14		±13.5	±14		V
Large Signal Voltage Gain	R_L >2kΩ V_{OUT} = ±10V	0.25	3.0		1.0	3.0		V/μV
Common Mode Rejection Ratio	R_S <10kΩ	96	120		110	120		dB
Power Supply Rejection Ratio	R_S <10kΩ		2.0	35		2.0	10	μV/V
Output Voltage Swing	R_L >10kΩ R_L >2kΩ	±12 ±10	±13 ±13		±12 ±12	±13.5 ±13.5		V V
Output Resistance			150			150		Ω
Power Consumption			80	150		80	105	mW
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage (Without external trim)	R_S <10kΩ		0.8	3.5			1.5	mV
Average Temperature Coefficient of Input Offset Voltage (Without external trim)	R_S = 50Ω		1.2			2.0	5.0	μV/°C
Average Temperature Coefficient of Input Offset Voltage (With external trim)	R_S = 50Ω		0.5			0.6		μV/°C
Input Offset Current	T_A(max) T_A(min)		1.2 4.0	35 50		1.2 7.5	20 40	nA nA
Average Temperature Coefficient of Input Offset Current			25			25	150	pA/°C
Input Bias Current	T_A(max) T_A(min)		25 100	125 250		20 80	100 200	nA nA
Large Signal Voltage Gain	R_L >2kΩ T_A(max) R_L >2kΩ, T_A(min)	0.125 0.125			1.0 0.25			V/μV
Common Mode Rejection Ratio	R_S <10kΩ		115		100			dB
Power Supply Rejection Ratio	R_S <10kΩ		20				20	μV/V
Output Voltage Swing	R_L >2kΩ	±10	±13		±10			V

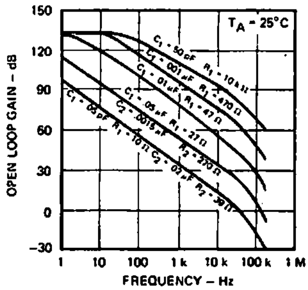
Notes: 1. Derate at 6.8 mW/°C for operation at ambient temperatures above 75°C.
2. For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

PERFORMANCE CURVES

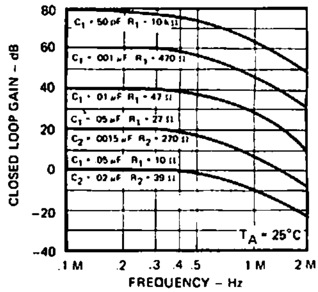
Maximum Undistorted Sinusoidal Output Versus Frequency



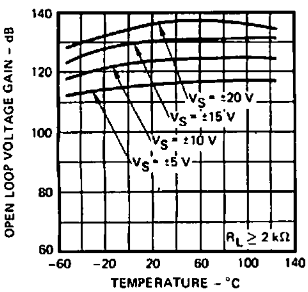
Open Loop Response For Various Values Of Compensation



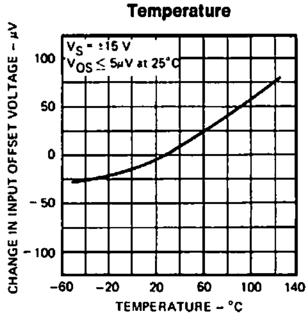
Frequency Response For Various Closed Loop Gains



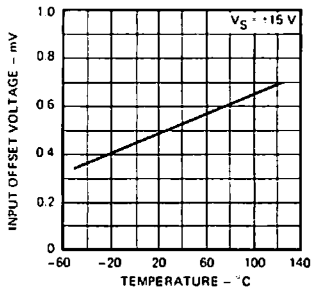
Open Loop Voltage Gain As A Function Of Temperature For Various Supply Voltages



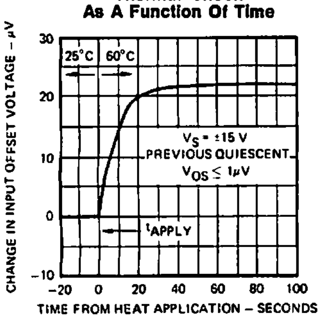
Nulled Input Offset Voltage As A Function Of Temperature



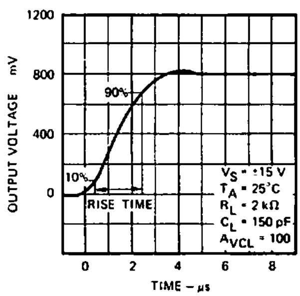
Unnulled Input Offset Voltage As A Function Of Temperature



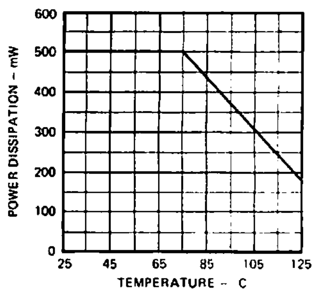
Change In Input Offset Voltage Due To Thermal Shock As A Function Of Time



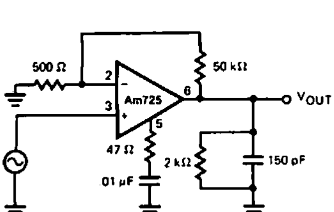
Transient Response



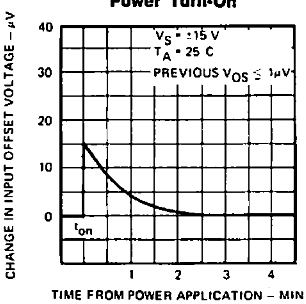
Absolute Maximum Power Dissipation As A Function Of Ambient Temperature



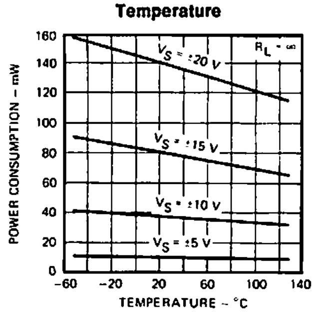
Transient Response Test Circuit



Stabilization Time Of Input Offset Voltage From Power Turn-On



Power Consumption As A Function Of Temperature

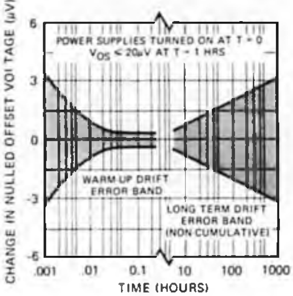


LIC-744

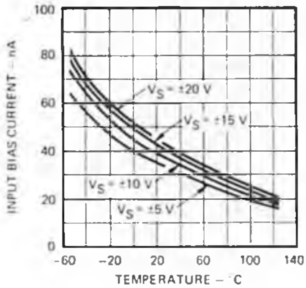
6

PERFORMANCE CURVES

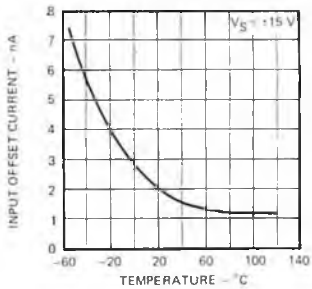
Input Offset Voltage Drift As A Function Of Time



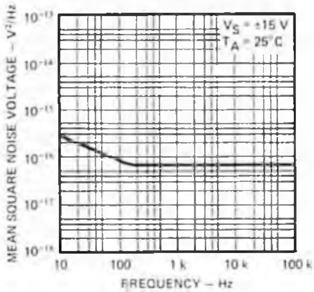
Input Bias Current As A Function Of Temperature



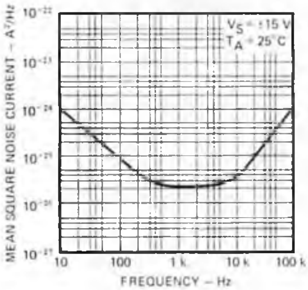
Input Offset Current As A Function Of Temperature



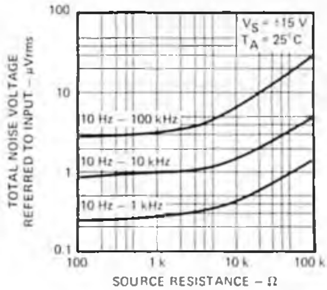
Input Noise Voltage As A Function Of Frequency



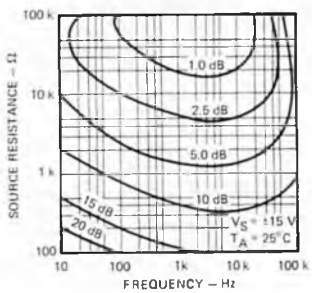
Input Noise Current As A Function Of Frequency



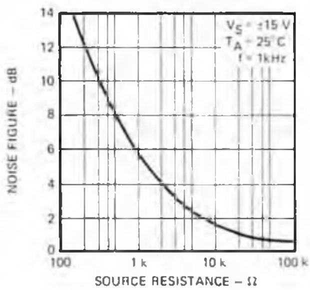
Broadband Noise For Various Bandwidths



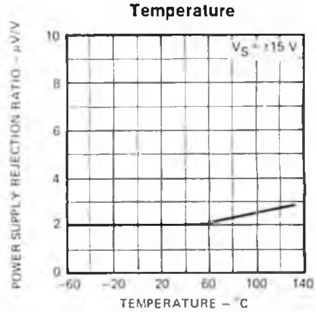
Narrow Band Spot Noise Figure Contours



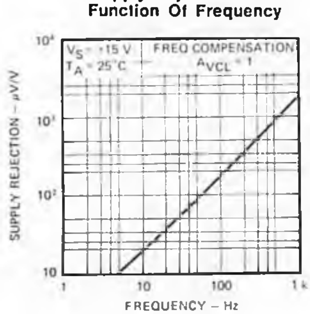
Noise Figure As A Function Of Source Resistance



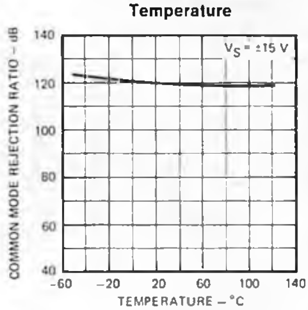
Supply Voltage Rejection Ratio As A Function Of Temperature



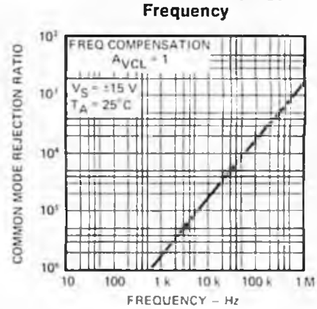
Supply Rejection As A Function Of Frequency



Common Mode Rejection Ratio As A Function Of Temperature

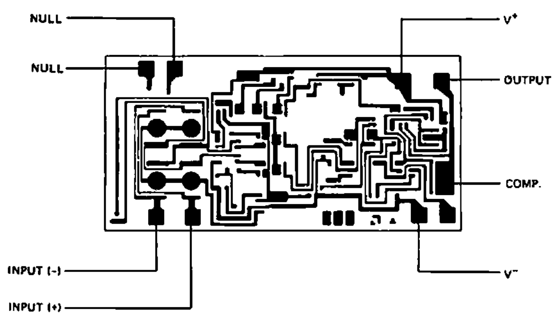


Common Mode Rejection Ratio As A Function Of Frequency



LIC-745

Metallization and Pad Layout



50 x 95 Mils

SSS725 • SSS741 • SSS747

High-Performance Operational Amplifiers

Functional Description

The SSS series are high-performance operational amplifiers designed for systems demanding extremely high accuracy. Superior DC and AC characteristics of low input offset voltage, low input offset current, low input bias current and high large signal voltage gain provide performance comparable to discrete or hybrid modules. The SSS series are functionally, electrically and pin-for-pin equivalent to the PMI SSS series.

Distinctive Characteristics

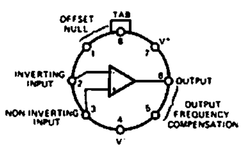
- Superior DC and AC characteristics V_{OS}, I_{OS}, A_{VO}, I_B, CMRR, PSRR
- 100% reliability assurance testing in compliance with MIL-STD-883

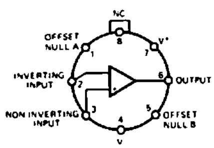
CONNECTION DIAGRAMS

Top View

SSS725 | **SSS741**

Metal Cans



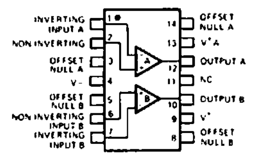


Notes:
(1) All leads through. No pins connected to case on SSS725.
(2) Pin 4 connected to case on SSS741.

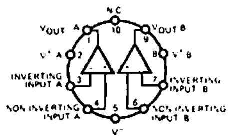
LIC-746

SSS747

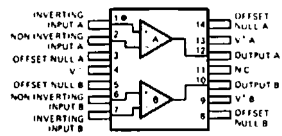
Dual-In-Line



Metal Can



Flat Package

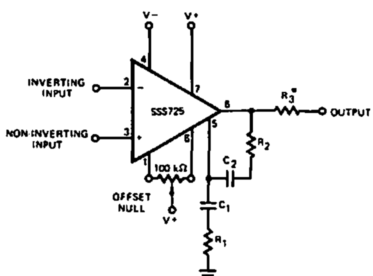


Notes:
(1) On Metal Can, pin 5 is connected to case.
(2) On DIP, pin 4 is connected to bottom of package.
(3) On Flat Package, pin 4 is connected to bottom of package.

LIC-747

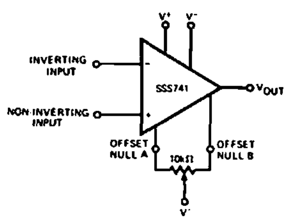
FUNCTIONAL DIAGRAMS

SSS725



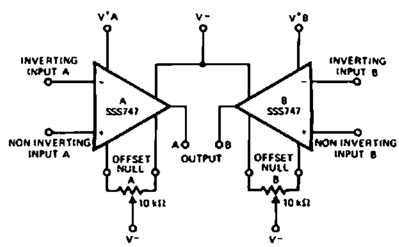
LIC-748

SSS741



LIC-749

SSS747



LIC-750

ORDERING INFORMATION

Order Number	Package Type	Temperature Range
SSS725J	Metal Can	−55°C - +125°C
SSS725BJ	Metal Can	−25°C - +85°C
SSS725EJ	Metal Can	0°C - +70°C
SSS741J	Metal Can	−55°C - +125°C
SSS741CJ	Metal Can	0°C - +70°C
SSS747K	Metal Can	−55°C - +125°C
SSS747Y	Hermetic DIP	−55°C - +125°C
SSS747M	Flat Pak	−55°C - +125°C
SSS747CK	Metal Can	0°C - +70°C
SSS747CY	Hermetic DIP	0°C - +70°C

SSS725 FREQUENCY

Compensation Component Values

A_{VCL}	R_1 (Ω)	C_1 (nF)	R_2 (Ω)	C_2 (nF)
1000	470	1.0	–	–
100	47	10	–	–
10	27	50	270	1.5
1	10	50	39	20

*Use R_3 = 51 Ω when the amplifier is operated with capacitive loads.

MAXIMUM RATINGS HIGH PERFORMANCE INSTRUMENTATION OP AMP SSS725

Supply Voltage	±22V
Internal Power Dissipation (Note 1) Metal Can (TO-99)	500mW
Differential Input Voltage	±5V
Input Voltage (Note 2)	±22V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range SSS725 SSS725B SSS725E	 −55°C to +125°C −25°C to +85°C 0°C to +70°C
Lead Temperature (Soldering, 60 sec.)	300°C
Output Short-Circuit Duration	Indefinite

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = 25°C Unless Otherwise Noted)

Symbol	Parameter	Condition	SSS725/725E Min.	SSS725/725E Max.	SSS725B Min.	SSS725B Max.	Units
V_{os}	Input Offset Voltage (Without external trim)	$R_s \leq 20k\Omega$		0.5		0.75	mV
I_{os}	Input Offset Current			5.0		5.0	nA
I_B	Input Bias Current			80		80	nA
e_n	Input Noise Voltage (Note 3)	f_o = 10Hz f_o = 100Hz f_o = 1kHz		15.0 9.0 7.5		15.0 9.0 7.5	nV/√Hz nV/√Hz nV/√Hz
i_n	Input Noise Current (Note 3)	f_o = 10Hz f_o = 100Hz f_o = 1kHz		1.2 0.6 0.25		1.2 0.6 0.25	pA/√Hz pA/√Hz pA/√Hz
R_{in}	Input Resistance		0.7		0.7		MΩ
A_{vo}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$ V_o = ±10V	1,000,000		1,000,000		
V_{om}	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±11.0		±12.5 ±12.0 ±11.0		V V V
CMVR	Input Voltage Range		±13.5		±13.5		V
CMRR	Common Mode Rejection Ratio	$R_s \leq 20k\Omega$	120		110		dB
PSRR	Power Supply Rejection Ratio	$R_s \leq 20k\Omega$		5.0		5.0	μV/V
P_d	Power Consumption			120		120	mW
A_{vo}	Large Signal Voltage Gain	$R_L \geq 500\Omega$ V_o = ±0.5V V_s = ±3V	100,000		100,000		
P_d	Power Consumption	V_s = ±3V		6		6	mW

The Following Specifications Apply Over The Operating Temperature Range

Symbol	Parameter	Condition	SSS725 Min.	SSS725 Max.	SSS725E Min.	SSS725E Max.	SSS725B Min.	SSS725B Max.	Units
V_{os}	Input Offset Voltage (Without external trim)	$R_s \leq 20k\Omega$		0.7		0.6		1.0	mV
	Average Input Offset Voltage Drift (Without external trim) (Note 4)	R_s = 50Ω		2.0		2.0 (Note 3)		2.8 (Note 3)	μV/°C
	Average Input Offset Voltage Drift (With external trim) (Note 4)	R_s = 50Ω		1.0		0.6		1.0 (Note 3)	μV/°C
I_{os}	Input Offset Current	T_A MAX. T_A MIN.		4.0 18.0		5.0 7.0		5.0 14.0	nA nA
	Average Input Offset Current Drift			90		40 (Note 3)		90 (Note 3)	pA/°C
I_B	Input Bias Current	T_A MAX. T_A MIN.		70 180		80 100		80 150	nA nA
CMRR	Common Mode Rejection Ratio	$R_s \leq 20k\Omega$	110		115		106		dB
PSRR	Power Supply Rejection Ratio	$R_s \leq 20k\Omega$		8.0		7.0		8.0	μV/V
A_{vo}	Large Signal Voltage Gain	V_o = ±10V; T_A MAX. $R_L \geq 2k\Omega$; T_A MIN.	1,000,000 500,000		1,000,000 800,000		1,000,000 500,000		
V_{om}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	±12.0		±12.0		±12.0		V

Notes 1. Derate at 6.8mW/°C for operation at ambient temperatures above 75°C.
2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. Parameter is not 100% tested. 90% of all units meet these specifications.
4. Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent the realization of the performance indicated if both sides of the contacts are not kept at approximately the same temperature. Therefore, the device ambient temperature should not be altered without simultaneously changing the contact temperature.

MAXIMUM RATINGS HIGH-PERFORMANCE FREQUENCY COMPENSATED OP AMP SSS741/741C

Supply Voltage	
SSS741	±22V
SSS741C	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Voltage between Offset Null and V⁻	±0.5V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
SSS741	−55°C to +125°C
SSS741C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

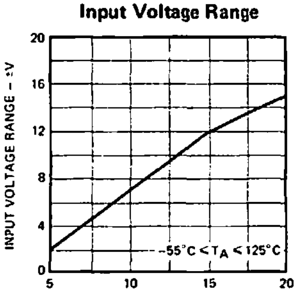
ELECTRICAL CHARACTERISTICS (T_A = 25°C) (Note 4)

Symbol	Parameter	Conditions	SSS741 Min.	SSS741 Max.	SSS741C Min.	SSS741C Max.	Units
V_{os}	Input Offset Voltage	$R_s < 50k\Omega$		2.0		5.0	mV
I_{os}	Input Offset Current			5.0		20	nA
I_B	Input Bias Current			50		100	nA
R_{in}	Input Resistance		2.0		1.0		MΩ
A_{vo}	Large-Signal Voltage Gain	$V_s = \pm15V$, $R_L > 2k\Omega$ $V_{out} = \pm10V$	100		50		V/mV
V_{om}	Output Voltage Swing	$V_s = \pm15V$, $R_L > 10k\Omega$ $R_L > 2k\Omega$	±12 ±10		±12 ±10		V V
CMVR	Input Voltage Range	$V_s = \pm15V$ $V_s = \pm20V$	±12 ±15		±12		V
CMRR	Common Mode Rejection Ratio	$R_s < 50k\Omega$	80		70		dB
PSRR	Power Supply Rejection Ratio	$R_s < 50k\Omega$		100		150	μV/V
P_d	Power Consumption	$V_s < \pm15V$		85		85	mW
The Following Specifications Apply Over the Operating Temperature Range							
V_{os}	Input Offset Voltage	$R_s < 50k\Omega$		3.0		6.0	mV
I_{os}	Input Offset Current			10		50	nA
I_B	Input Bias Current			100		200	nA
A_{vo}	Large-Signal Voltage Gain	$V_s = \pm15V$, $R_L > 2k\Omega$ $V_{out} = \pm10V$	25		25		V/mV
V_{om}	Output Voltage Swing	$V_s = \pm15V$, $R_L > 10k\Omega$ $R_L > 2k\Omega$	±12 ±10		±12 ±10		V V
CMVR	Input Voltage Range	$V_s = \pm20V$	±15				V
CMRR	Common Mode Rejection Ratio	$R_s < 50k\Omega$	80		70		dB
PSRR	Power Supply Rejection Ratio	$R_s < 50k\Omega$		100		150	μV/V

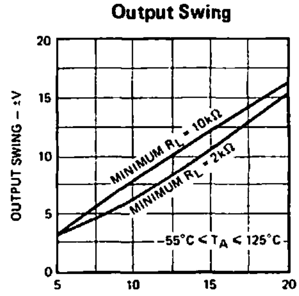
Notes 1. *Derate metal can package at 6.8mW/°C for operation at ambient temperatures above 75°C.*
2. For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
4. The SSS741 specifications apply for ±5V ≤ V_s ≤ ±20V. The SSS741C specifications apply for V_s = ±15V.

GUARANTEED PERFORMANCE

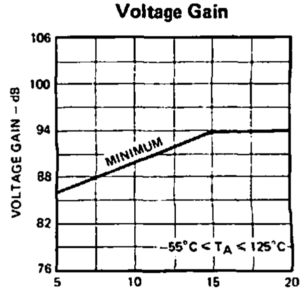
Input Voltage Range



Output Swing



Voltage Gain



LIC-751

MAXIMUM RATINGS HIGH-PERFORMANCE DUAL FREQUENCY COMPENSATED OP AMP SSS747/747C

Supply Voltage	
SSS747	±22V
SSS747C	±18V
Internal Power Dissipation (Note 1)	
DIP, Metal Can	800mW
Flat Package	500mW
Differential Input Voltage	±30V
Voltage between Offset Null and V^-	±0.5V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
SSS747	−55°C to +125°C
SSS747C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C) (Note 4)

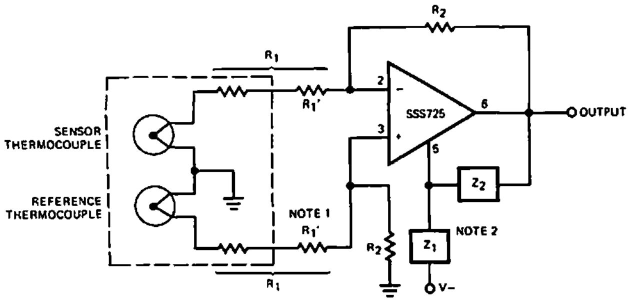
Symbol	Parameter	Conditions	SSS747 Min.	SSS747 Max.	SSS747C Min.	SSS747C Max.	Units
V_{os}	Input Offset Voltage	$R_s \le 50k\Omega$		2.0		5.0	mV
I_{os}	Input Offset Current			5.0		20	nA
I_B	Input Bias Current			50		100	nA
R_{in}	Input Resistance		2.0		1.0		MΩ
A_{vo}	Large Signal Voltage Gain	$R_L > 2k\Omega$, $V_s = \pm15V$, $V_{out} = \pm10V$	100		50		V/mV
V_{om}	Output Voltage Swing	$V_s = \pm15V$, $R_L > 10k\Omega$ $R_L > 2k\Omega$	±12 ±10		±12 ±10		V V
CMVR	Input Voltage Range	$V_s = \pm15V$ $V_s = \pm20V$	 ±15		±12 		V V
CMRR	Common Mode Rejection Ratio	$R_s < 50k\Omega$	80		70		dB
PSRR	Power Supply Rejection Ratio	$R_s < 50k\Omega$		100		150	μV/V
P_d	Power Dissipation	$V_s < \pm15V$		85		85	mW
CS	Channel Separation		100				dB
The Following Specifications Apply Over The Operating Temperature Ranges							
V_{os}	Input Offset Voltage	$R_s < 50k\Omega$		3.0		6.0	mV
I_{os}	Input Offset Current			10		50	nA
I_B	Input Bias Current			100		150	nA
A_{vo}	Large Signal Voltage Gain	$V_s = \pm15V$, $V_O = \pm10V$, $R_L > 2k\Omega$	25		25		V/mV
V_{om}	Output Voltage Swing	$V_s = \pm15V$, $R_L > 10k\Omega$ $R_L > 2k\Omega$	±12 ±10		±12 ±10		V V
CMVR	Input Voltage Range	$V_s = \pm20V$	±15				V
CMRR	Common Mode Rejection Ratio	$R_s < 50k\Omega$	80		70		dB
PSRR	Power Supply Rejection Ratio	$R_s < 50k\Omega$		100		150	μV/V

Notes 1. Derate metal can package at 6.8 mW/°C for operation at ambient temperatures above 30°C, the dual-in-line package at 9 mW/°C for operation at ambient temperatures above 60°C, and the Flat package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be ground or either supply. Rating applies to 125°C case temperature or +60°C ambient temperature for each side.
4. The SSS747 specifications apply for ±5V < V_s < ±20V, unless otherwise noted. The SSS747C specifications apply for ±5V < V_S < ±15V, unless otherwise noted..

TYPICAL APPLICATIONS

SSS725

Thermocouple Amplifier

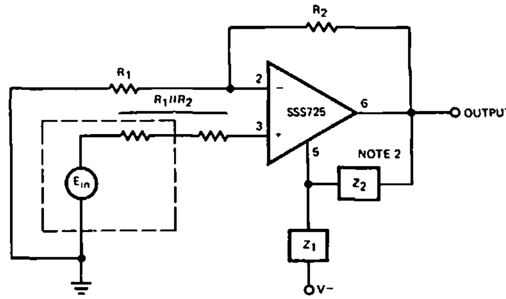


$$A_V = \frac{-R_2}{R_1 + \frac{R_1}{A_{VO}} + \frac{R_2}{A_{VO}}}$$

Notes:
(1) R_1' is adjusted so that the sum of R_1' and the thermocouple circuit resistance equals the correct value for R_1.
(2) See Frequency Compensation Circuit.

LIC-752

High Gain Non-Inverting Amplifier



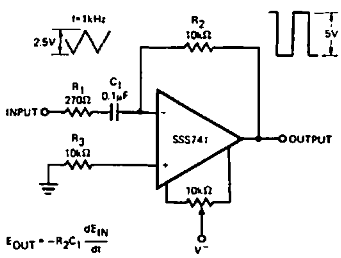
$$A_V = \frac{R_1 + R_2}{R_1 + \frac{R_1}{A_{VO}} + \frac{R_2}{A_{VO}}}$$

For ideal resistors and open loop gain greater than 10^6, in a +1000 gain configuration, the gain error will be less than 0.1% and input impedance will be greater than 700MΩ.

LIC-753

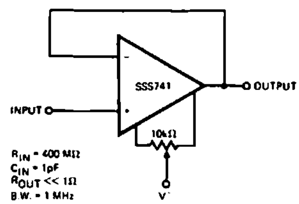
SSS741

Differentiator



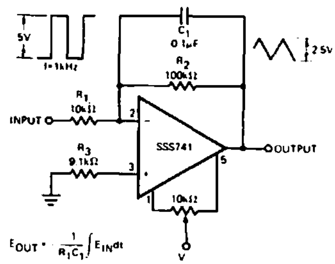
LIC-754

Unity Gain Voltage Follower



LIC-755

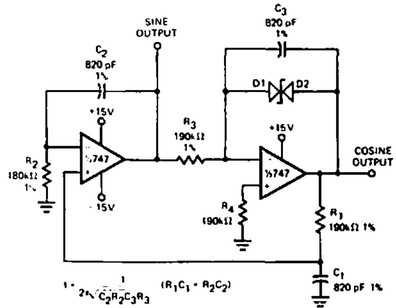
Integrator



LIC-756

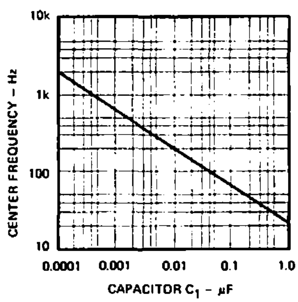
SSS747

Quadrature Oscillator



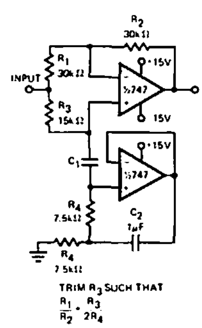
LIC-757

Notch Frequency as a Function of C_1



LIC-758

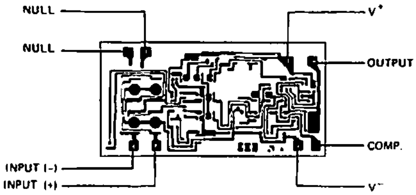
Notch Filter Using the 747 as a Gyrator



LIC-759

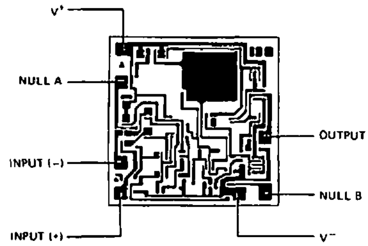
Metallization and Pad Layouts

SSS725



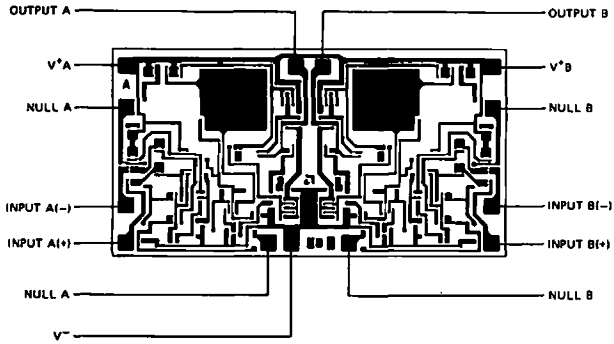
50 X 95 Mils

SSS741



56 X 56 Mils

SSS747



56 X 106 Mils

Am741/741C/741A/741E

Frequency-Compensated Operational Amplifier

Description:

The Am741 Series Frequency Compensated Operational Amplifiers are functionally, electrically, and pin-for-pin equivalent to the Fairchild μ741 series. The are available in the hermetic metal can, flat package, and dual-in-line packages as well as plastic dual-in-line.

The Am741A and Am741E are tested to the electrical characteristics of the current revision of MIL-M-38510/10101.

Distinctive Characteristics:

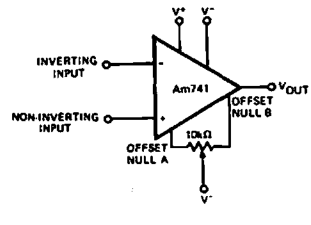
100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL-STD-883.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am741 series are differential input, class AB output amplifiers intended for general purpose applications. They are protected against faults at input and output, and require no external components for frequency compensation.

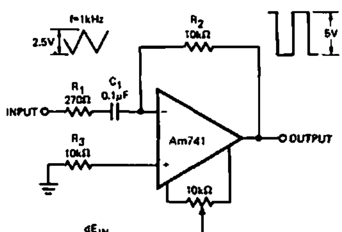
FUNCTIONAL DIAGRAM



LIC-760

APPLICATIONS

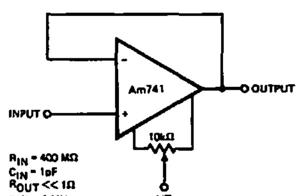
DIFFERENTIATOR



$E_{OUT} = -R_2C_1\frac{dE_{IN}}{dt}$

LIC-761

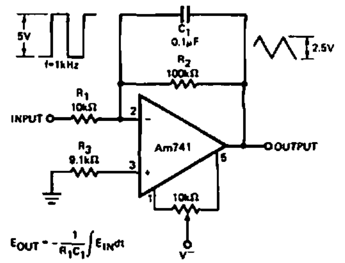
UNITY GAIN VOLTAGE FOLLOWER



$R_{IN} = 400\ M\Omega$
$C_{IN} = 1pF$
$R_{OUT} << 1\Omega$
B.W. = 1 MHz

LIC-762

INTEGRATOR



$E_{OUT} = -\frac{1}{R_1C_1}\int E_{IN}dt$

LIC-763

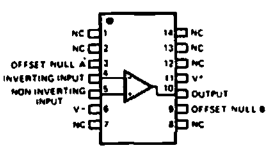
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am741C	Metal Can	0°C to +70°C	741HC
	Hermetic DIP	0°C to +70°C	741DC
	Dice	0°C to +70°C	741XC
Am741	Metal Can	−55°C to +125°C	741HM
	Hermetic DIP	−55°C to +125°C	741DM
	Flat Pack	−55°C to +125°C	741FM
	Dice	−55°C to +125°C	741XM
Am741E	Metal Can	0°C to +70°C	741EHC
	Hermetic DIP	0°C to +70°C	741EDC
Am741A	Metal Can	−55°C to +125°C	741AHM
	Hermetic DIP	−55°C to +125°C	741ADM
	Flat Pack	−55°C to +125°C	741AFM

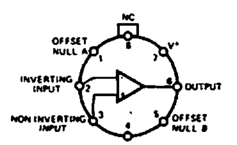
CONNECTION DIAGRAMS

Top Views

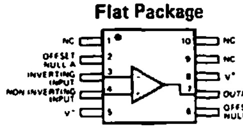
Dual-In-Line



Metal Can



Flat Package



Notes:

1. On DIP, pin 6 is connected to bottom of package.
2. On Flat Package, pin 5 is connected to bottom of package.

LIC-764

MAXIMUM RATINGS

Supply Voltage	
Am741/741A/741E	±22 V
Am741C	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Voltage between Offset Null and V^-	±0.5 V
Input Voltage (Note 2)	±15 V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
Am741/741A	−55°C to +125°C
Am741C/741E	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

Parameter (see definitions)	Conditions	Am741C Min.	Am741C Typ.	Am741C Max.	Am741 Min.	Am741 Typ.	Am741 Max.	Units
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0		1.0	5.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Input Capacitance			1.4			1.4		pF
Offset Voltage Adjustment Range			±15			±15		mV
Input Voltage Range		±12	±13		±12	±13		V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	20	200		50	200		V/mV
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Current			1.7	2.8		1.7	2.8	mA
Power Consumption			50	85		50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF							
Risetime			0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate	$R_L \geq 2$ kΩ	0.3	0.4		0.3	0.4		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5			6.0	mV
Input Offset Current	$T_{A(max)}$		9.0	300		7.0	200	nA
	$T_{A(min)}$		35	300		85	500	nA
Input Bias Current	$T_{A(max)}$		0.04	0.8		0.03	0.5	μA
	$T_{A(min)}$		0.13	0.8		0.3	1.5	μA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15			25			V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Supply Current	$T_{A(max)}$		1.6	3.3		1.5	2.5	mA
	$T_{A(min)}$		1.8	3.3		2.0	3.3	mA
Power Consumption	$T_{A(max)}$		48	100		45	75	mW
	$T_{A(min)}$		54	100		60	100	mW

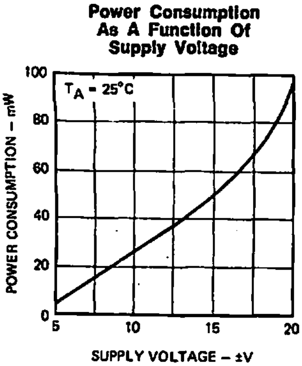
Notes: 1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C, the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

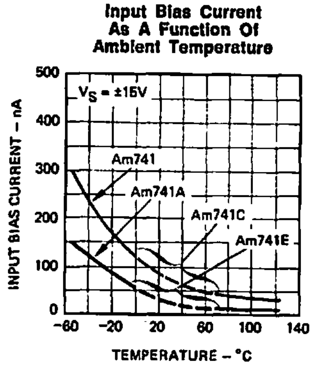
ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified) Am741A/741E

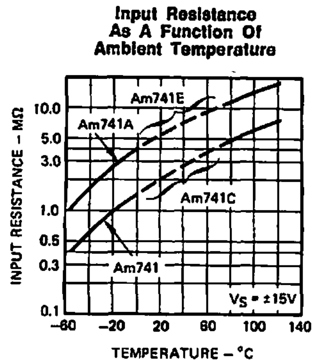
Parameters (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 50\Omega$		0.8	3.0	mV
Input Offset Current			3.0	30	nA
Input Bias Current (Note 5)			30	110	nA
Power Supply Rejection Ratio (Note 6)	V_S = +10, −20; V_S = +20, −10V, R_S = 50Ω		15	50	μV/V
Common Mode Rejection	V_{CM} = ±15V	80			dB
Output Short Circuit Current	$\pm V_{CC}$ = ±15V, V_O = ±15V Short to Other Supply	9		40	mA
Power Dissipation		10		150	mW
Large Signal Voltage Gain	$\pm V_{CC}$ = ±20V; R_L = 2kΩ, 10kΩ; V_O = ±15V	50			V/mV
	$\pm V_{CC}$ = ±5V; R_L = 2kΩ, 10kΩ; V_O = ±2V	10			V/mV
Transient Response (unity gain)					
Rise Time			0.30	0.8	μs
Overshoot			5.0	20	%
Adjustment for Input Offset Voltage	(Note 7)	7.5			mV
Large Signal Voltage Swing	R_L = 10kΩ	32			Volts
	R_L = 2kΩ	30			Volts
Slew Rate (unity gain)	V_{IN} = ±10V	0.3	0.42		V/μs
Noise	Bandwidth = 5kHz			15	μV RMS
	Bandwidth = 5kHz			40	μV Peak
The Following Specifications Apply for Min $\leq T_A \leq$ Max					
Input Offset Voltage				4.0	mV
Average Input Offset Voltage Drift				15	μV/°C
Input Offset Current	$T_{A(max)}$			30	nA
	$T_{A(min)}$			70	nA
Average Input Offset Current Drift	25°C ≤ T_A ≤ Max			200	pA/°C
	Min ≤ T_A ≤ 25°C			500	pA/°C
Input Bias Current (Note 5)	$T_{A(max)}$	1.0		110	nA
	$T_{A(min)}$	1.0		265	nA
Output Short Circuit Current	$T_{A(max)}$	9.0		40	mA
	$T_{A(min)}$	9.0		55	mA
Power Dissipation	$T_{A(max)}$			135	mW
	$T_{A(min)}$			165	mW
Large Signal Voltage Swing	R_L = 10kΩ	32			Volts
	R_L = 2kΩ	30			Volts
Large Signal Voltage Gain	$\pm V_{CC}$ = ±20V; R_L = 2kΩ, 10kΩ; V_O = ±15V	32			V/mV
	$\pm V_{CC}$ = ±5V; R_L = 2kΩ, 10kΩ; V_O = ±2V	10			V/mV

Notes:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for the metal can, 8.3mW/°C for the DIP and 7.1mW/°C for the Flatpak.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 75°C ambient temperature.
4. $T_{A(min)}$ for 741A is −55°C and for 741E is 0°C. $T_{A(max)}$ for 741A is +125°C and for 741E is +70°C.
5. Input bias currents are measured individually to specified limits.
6. PSRR measured separately for positive and negative supply to specified limits.
7. V_{OS} adjust is measured in both positive and negative direction to the specified limit.

PERFORMANCE CURVES

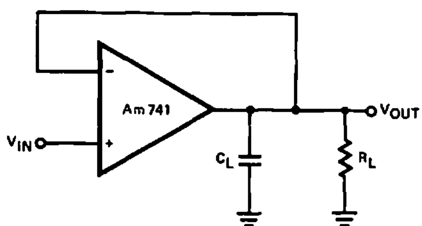






LIC-765

Slew Rate and Transient Response Test Circuit



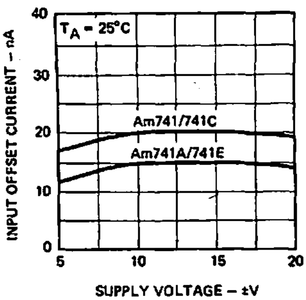
$C_L \leq 100$ pF
$R_L = 2$ kΩ

LIC-766

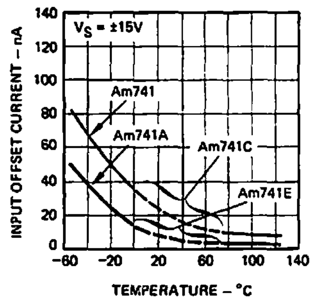
6

PERFORMANCE CURVES (Cont.)

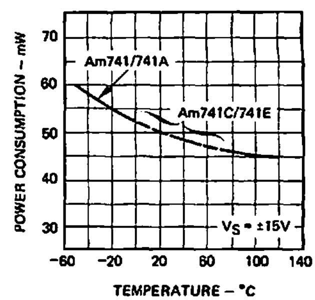
Input Offset Current As A Function Of Supply Voltage



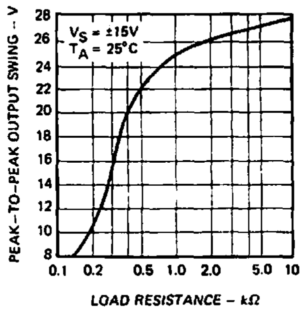
Input Offset Current As A Function Of Ambient Temperature



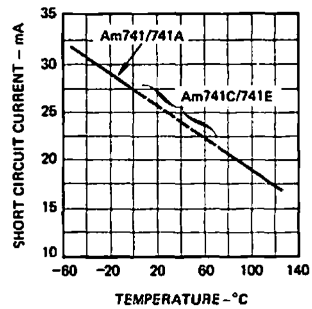
Power Consumption As A Function Of Ambient Temperature



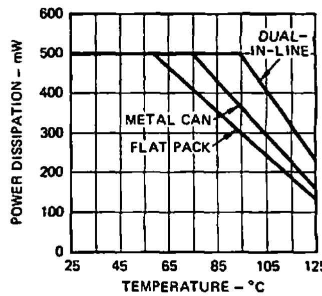
Output Voltage Swing As A Function Of Load Resistance



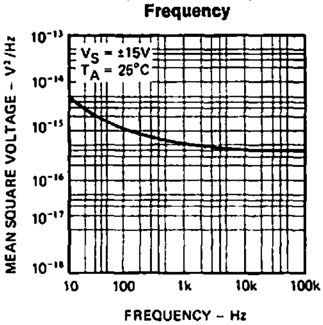
Output Short-Circuit Current As A Function Of Ambient Temperature



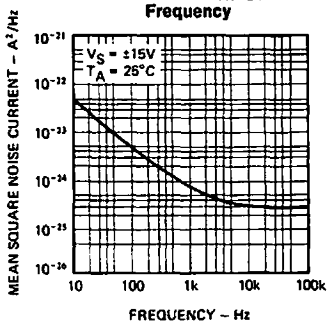
Absolute Maximum Power Dissipation As A Function Of Ambient Temperature



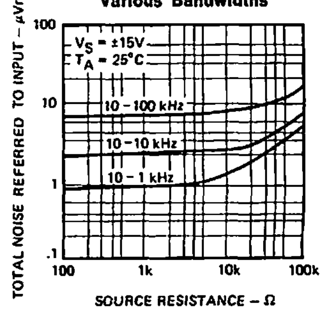
Input Noise Voltage As A Function Of Frequency



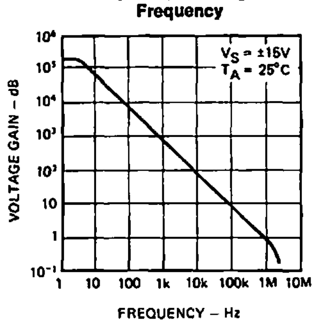
Input Noise Current As A Function Of Frequency



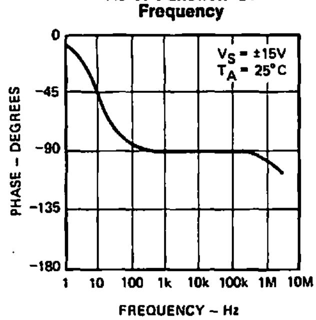
Broadband Noise For Various Bandwidths



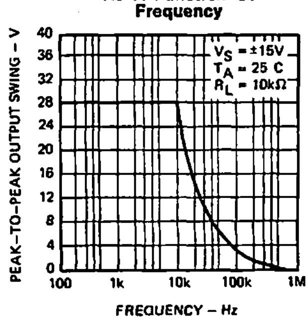
Open Loop Voltage Gain As A Function Of Frequency



Open Loop Phase Response As A Function Of Frequency



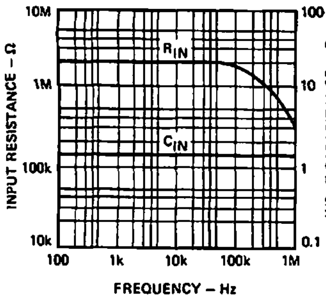
Output Voltage Swing As A Function Of Frequency



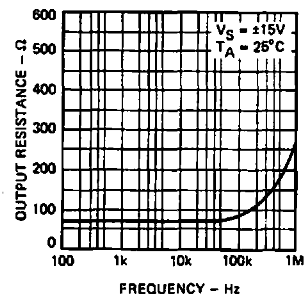
LIC-767

PERFORMANCE CURVES (Cont.)

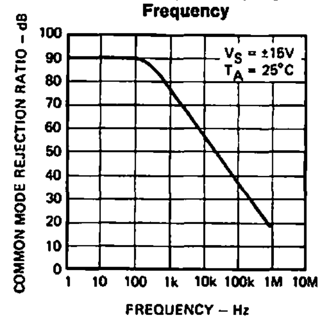
Input Resistance And Input Capacitance As A Function Of Frequency



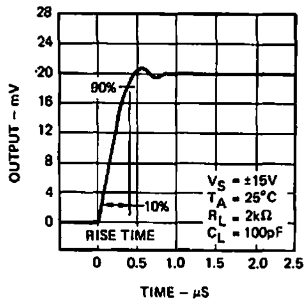
Output Resistance As A Function Of Frequency



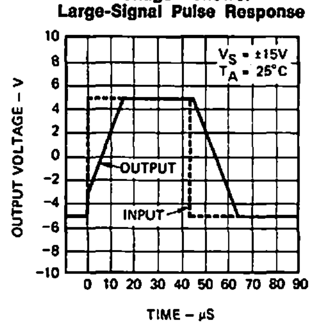
Common Mode Rejection Ratio As A Function Of Frequency



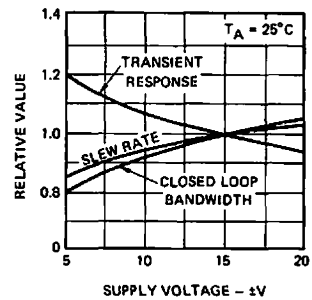
Transient Response



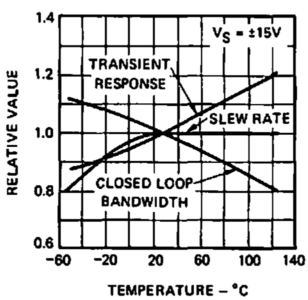
Voltage Follower Large-Signal Pulse Response



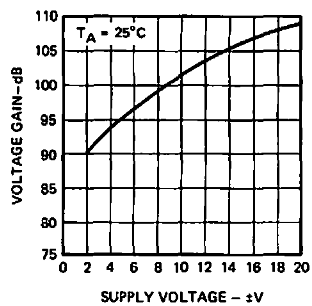
Frequency Characteristics As A Function Of Supply Voltage



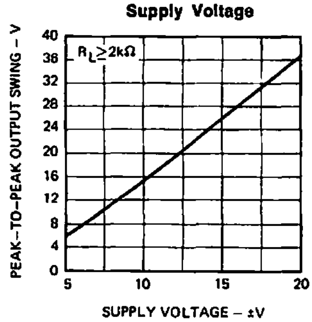
Frequency Characteristics As A Function Of Ambient Temperature



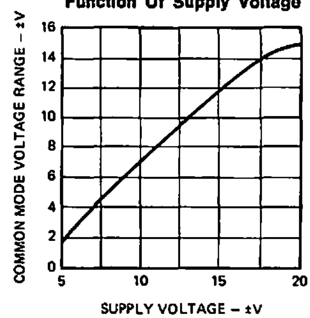
Open Loop Voltage Gain As A Function Of Supply Voltage



Output Voltage Swing As A Function Of Supply Voltage



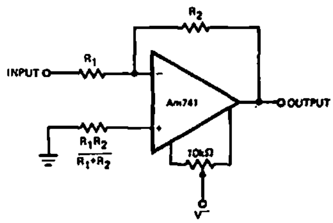
Input Common Mode Voltage Range As A Function Of Supply Voltage



LIC-768

6

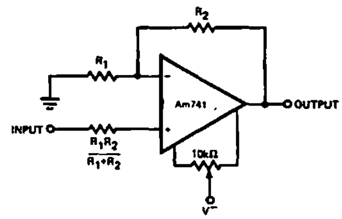
INVERTING AMPLIFIER



LIC-769

GAIN	R_1	R_2	B.W.	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

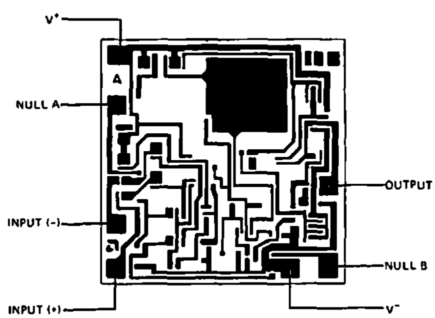
NON-INVERTING AMPLIFIER



LIC-770

GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

Metallization and Pad Layout



56 X 56 Mils

Am747/747C/747A/747E

Dual Frequency-Compensated Operational Amplifiers

Description:

The Am747 Series Dual Frequency-Compensated Operational Amplifiers are functionally, electrically, and pin-for pin equivalent to the Fairchild µA747 series. They are available in the hermetic metal can, dual-in-line and flat packages as well as plastic dual-in-line.

The Am747A and Am747E are tested to the electrical characteristics of the current revision of MIL-M-38510/10102.

Distinctive Characteristics:

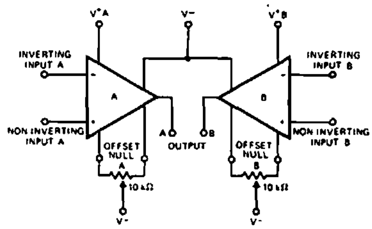
100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL-STD-883.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am747 is a dual Am741 internally compensated operational amplifier. The Am747 Series are differential input, class AB output amplifiers intended for general purpose applications. They are protected against faults at input and output, and require no external components for frequency compensation.

FUNCTIONAL DIAGRAM

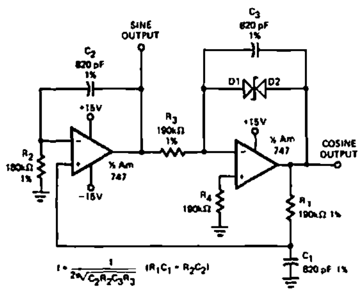


Note: V+A and V+B connected internally. For separate V+ pins order as 747-1.

LIC-771

APPLICATIONS

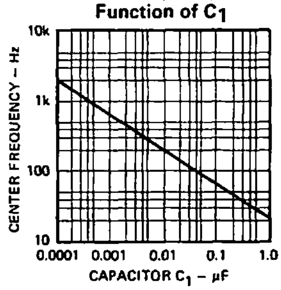
QUADRATURE OSCILLATOR



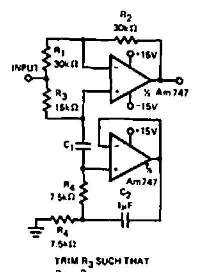
LIC-772

NOTCH FILTER USING THE Am747 AS A GYRATOR

Notch Frequency as a Function of C_1



LIC-773



LIC-774

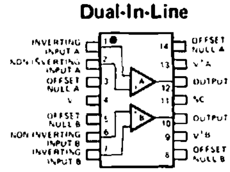
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am747C	Hermetic DIP	0°C to +70°C	747DC
	Metal Can	0°C to +70°C	747HC
	Molded DIP	0°C to +70°C	747PC
	Dice	0°C to +70°C	747XC
Am747	Hermetic DIP	−55°C to +125°C	747DM
	Metal Can	−55°C to +125°C	747HM
	Flat Pak	−55°C to +125°C	747FM
	Dice	−55°C to +125°C	747XM
Am747E	Hermetic DIP	0°C to +70°C	747EDC
	Metal Can	0°C to +70°C	747EHC
Am747A	Hermetic DIP	−55°C to +125°C	747ADM
	Metal Can	−55°C to +125°C	747AHM
	Flat Pak	−55°C to +125°C	747AFM

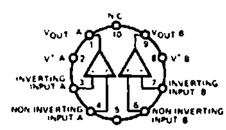
CONNECTION DIAGRAMS

Top Views

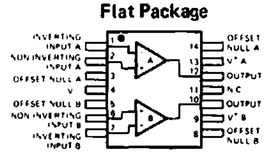
Dual-In-Line



Metal Can



Flat Package



Notes:
1. On Metal Can, pin 5 is connected to case.
2. On DIP, pin 4 is connected to bottom of package.
3. On Flat Package, pin 4 is connected to bottom of package.
4. V+A and V+B are connected internally.

LIC-775

6

MAXIMUM RATINGS

Supply Voltage	
Am747, Am747A, Am747E	±22 V
Am747C	±18 V
Internal Power Dissipation (Note 1)	
DIP, Metal Can	800 mW
Flat Package	500 mW
Differential Input Voltage	±30 V
Voltage between Offset Null and V⁻	±0.5 V
Input Voltage (Note 2)	±15 V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
Am747, Am747A	−55°C to +125°C
Am747C, Am747E	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS—Each Amplifier ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

Parameter (see definitions)	Conditions	Am747C Min.	Am747C Typ.	Am747C Max.	Am747 Min.	Am747 Typ.	Am747 Max.	Units
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0		1.0	5.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Input Capacitance			1.4			1.4		pF
Offset Voltage Adjustment Range			±15			±15		mV
Input Voltage Range		±12	±13		±12	±13		V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25	200		50	200		V/mV
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Current			1.7	2.8		1.7	2.8	mA
Power Consumption			50	85		50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF							
Risetime			0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate	$R_L \geq 2$ kΩ	0.3	0.4		0.3	0.4		V/μs
Channel Separation	$R_S = 50$ Ω, $R_L \geq 10$ kΩ		120			120		dB
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5			6.0	mV
Input Offset Current	$T_{A(max)}$		9.0	300		7.0	200	nA
	$T_{A(min)}$		35	300		85	500	nA
Input Bias Current	$T_{A(max)}$		0.04	0.8		0.03	0.5	μA
	$T_{A(min)}$		0.13	0.8		0.3	1.5	μA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15			25			V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Supply Current	$T_{A(max)}$		1.6	3.3		1.5	2.5	mA
	$T_{A(min)}$		1.8	3.3		2.0	3.3	mA
Power Consumption	$T_{A(max)}$		48	100		45	75	mW
	$T_{A(min)}$		54	100		60	100	mW

Notes: 1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 30°C, the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 60°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be ground or either supply. Rating applies to 125°C case temperature or +60°C ambient temperature for each side.

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified) Am747A/747E

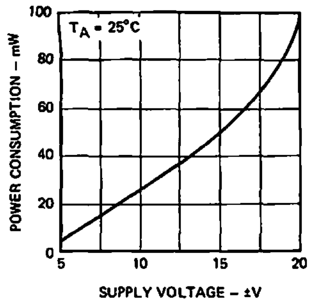
Parameters (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	R_S ≤ 50Ω		0.8	3.0	mV
Input Offset Current			3.0	30	nA
Input Bias Current (Note 5)			30	110	nA
Power Supply Rejection Ratio (Note 6)	V_S = +10, −20; V_S = +20, −10V, R_S = 50Ω		15	50	µV/V
Common Mode Rejection	V_{CM} = ±15V	80			dB
Output Short Circuit Current	$\pm V_{CC}$ = ±15V, V_O = ±15V Short to Other Supply	9		40	mA
Power Dissipation		10		150	mW
Large Signal Voltage Gain	$\pm V_{CC}$ = ±20V; R_L = 2kΩ 10kΩ; V_O = ±15V	50			V/mV
	$\pm V_{CC}$ = ±5V; R_L = 2kΩ 10kΩ; V_O = ±2V	10			V/mV
Transient Response (unity gain)					
Rise Time			0.30	0.8	µs
Overshoot			5.0	20	%
Adjustment for Input Offset Voltage	(Note 7)	7.5			mV
Large Signal Voltage Swing	R_L = 10kΩ	32			Volts
	R_L = 2kΩ	30			Volts
Slew Rate (unity gain)	V_{IN} = ±10V	0.3	0.42		V/µs
Noise	Bandwidth = 5kHz			15	µV RMS
	Bandwidth = 5kHz			40	µV Peak
The Following Specifications Apply for Min ≤ T_A ≤ Max					
Input Offset Voltage				4.0	mV
Average Input Offset Voltage Drift				15	µV/°C
Input Offset Current	$T_{A(max)}$			30	nA
	$T_{A(min)}$			70	nA
Average Input Offset Current Drift	25°C < T_A < Max			200	pA/°C
	Min < T_A < 25°C			500	pA/°C
Input Bias Current (Note 5)	$T_{A(max)}$	1.0		110	nA
	$T_{A(min)}$	1.0		265	nA
Output Short Circuit Current	$T_{A(max)}$	9.0		40	mA
	$T_{A(min)}$	9.0		55	mA
Power Dissipation	$T_{A(max)}$			135	mW
	$T_{A(min)}$			165	mW
Large Signal Voltage Swing	R_L = 10kΩ	32			Volts
	R_L = 2kΩ	30			Volts
Large Signal Voltage Gain	$\pm V_{CC}$ = ±20V; R_L = 2kΩ, 10kΩ; V_O = ±15V	32			V/mV
	$\pm V_{CC}$ = ±5V; R_L = 2kΩ, 10kΩ; V_O = ±2V	10			V/mV

Notes:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for the metal can, 8.3mW/°C for the DIP and 7.1mW/°C for the Flatpak.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 75°C ambient temperature.
4. $T_{A(min)}$ for 741A is −55°C and for 741E is 0°C. $T_{A(max)}$ for 741A is +125°C and for 741E is +70°C.
5. Input bias currents are measured individually to specified limits.
6. PSRR measured separately for positive and negative supply to specified limits.
7. V_{OS} adjust is measured in both positive and negative direction to the specified limit.

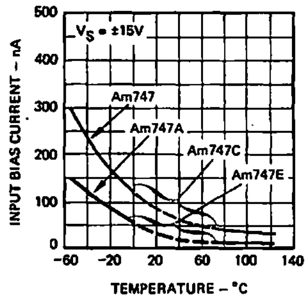
6

PERFORMANCE CURVES
(Each Amplifier)

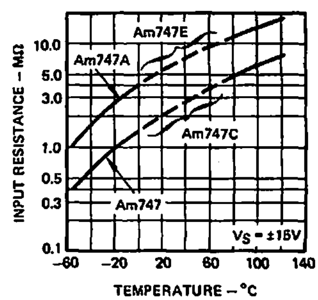
Power Consumption As A Function Of Supply Voltage



Input Bias Current As A Function Of Ambient Temperature

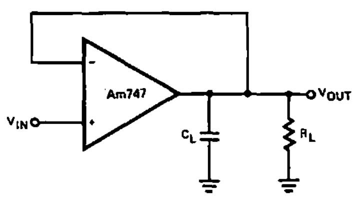


Input Resistance As A Function Of Ambient Temperature



LIC-776

Transient Response Test Circuit



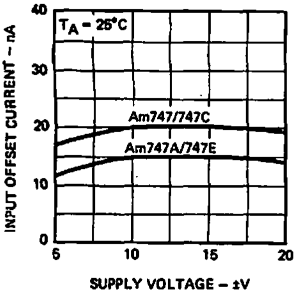
LIC-777

$C_L \leq 100$ pF
$R_L = 2$ kΩ

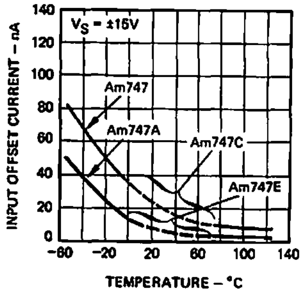
PERFORMANCE CURVES (Cont.)

(Each Amplifier)

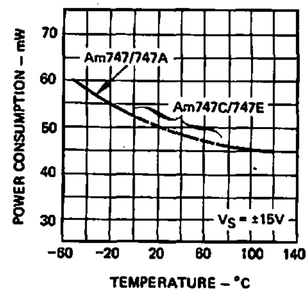
Input Offset Current As A Function Of Supply Voltage



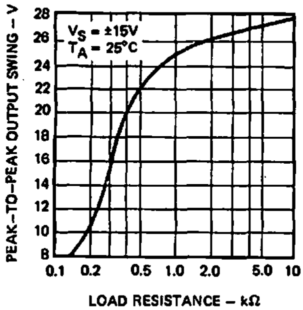
Input Offset Current As A Function Of Ambient Temperature



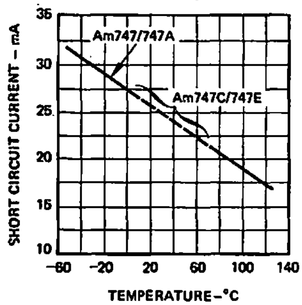
Power Consumption As A Function Of Ambient Temperature



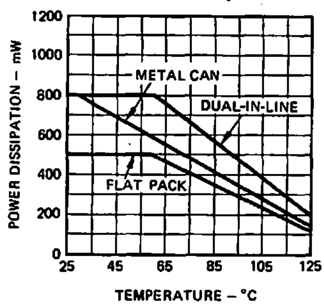
Output Voltage Swing As A Function Of Load Resistance



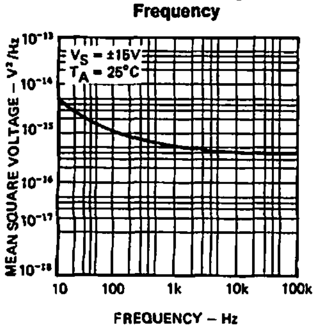
Output Short-Circuit Current As A Function Of Ambient Temperature



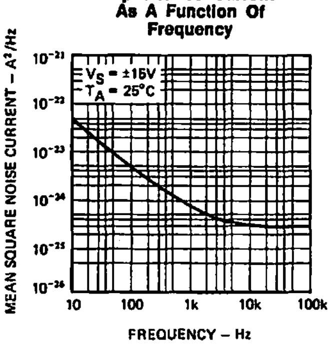
Absolute Maximum Power Dissipation As A Function Of Ambient Temperature



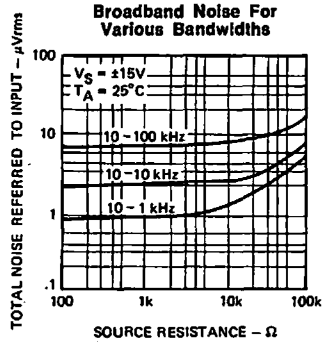
Input Noise Voltage As A Function Of Frequency



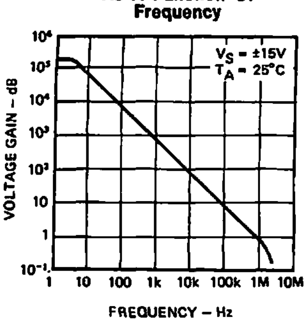
Input Noise Current As A Function Of Frequency



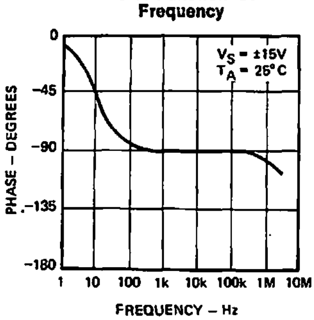
Broadband Noise For Various Bandwidths



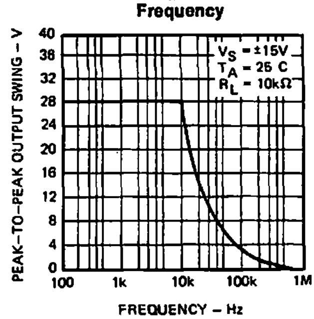
Open Loop Voltage Gain As A Function Of Frequency



Open Loop Phase Response As A Function Of Frequency



Output Voltage Swing As A Function Of Frequency

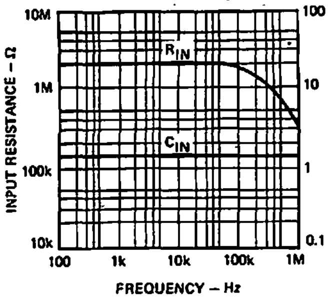


LIC-778

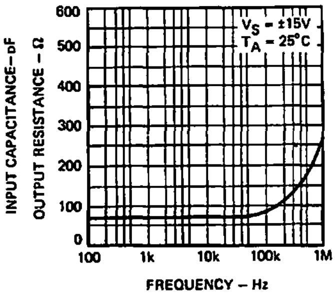
PERFORMANCE CURVES (Cont.)

(Each Amplifier)

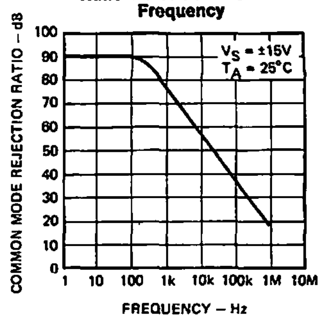
Input Resistance And Input Capacitance As A Function Of Frequency



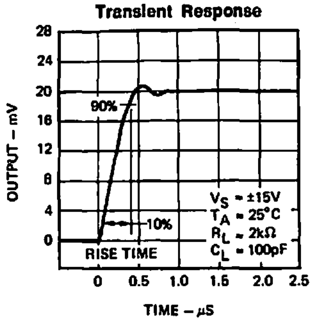
Output Resistance As A Function Of Frequency



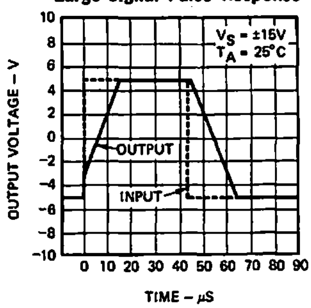
Common Mode Rejection Ratio As A Function Of Frequency



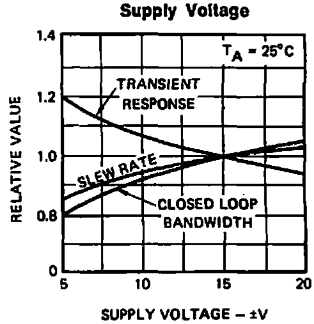
Transient Response



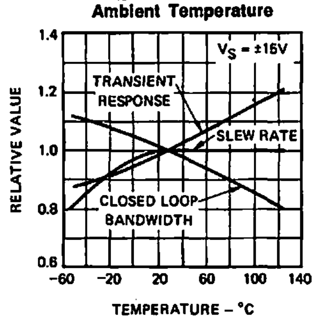
Voltage Follower Large-Signal Pulse Response



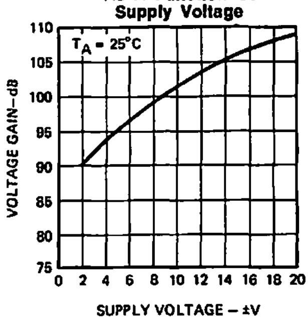
Frequency Characteristics As A Function Of Supply Voltage



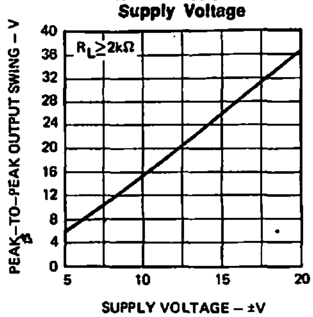
Frequency Characteristics As A Function Of Ambient Temperature



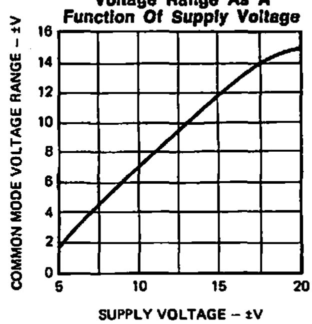
Open Loop Voltage Gain As A Function Of Supply Voltage



Output Voltage Swing As A Function Of Supply Voltage



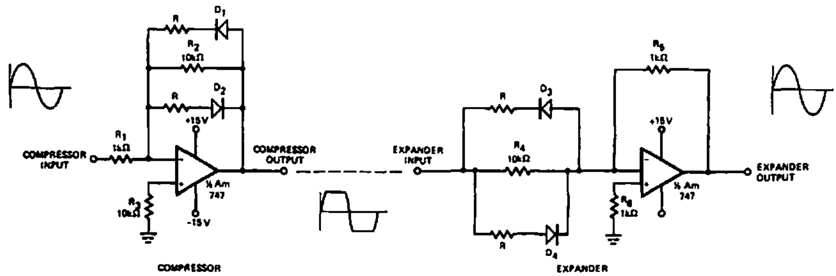
Input Common Mode Voltage Range As A Function Of Supply Voltage



LIC-779

ADDITIONAL APPLICATIONS

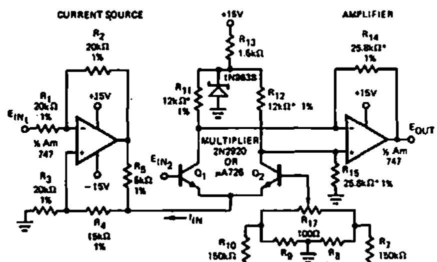
COMPRESSOR/EXPANDER AMPLIFIERS



MAXIMUM COMPRESSION/EXPANSION RATIO = R_1/R (10 kΩ > R ≥ 0)
DIODES D_1 THROUGH D_4 ARE MATCHED FD6666 OR EQUIVALENT

LIC-780

ANALOG MULTIPLIER

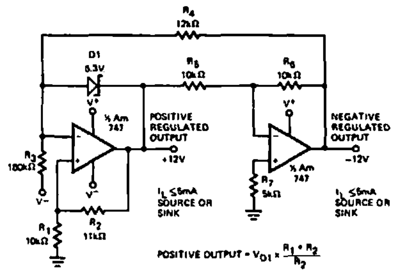


*MATCHED TO 0.1%

$E_{OUT} = 100\,E_{IN_1} \times E_{IN_2}$

LIC-781

TRACKING POSITIVE AND NEGATIVE VOLTAGE REFERENCES

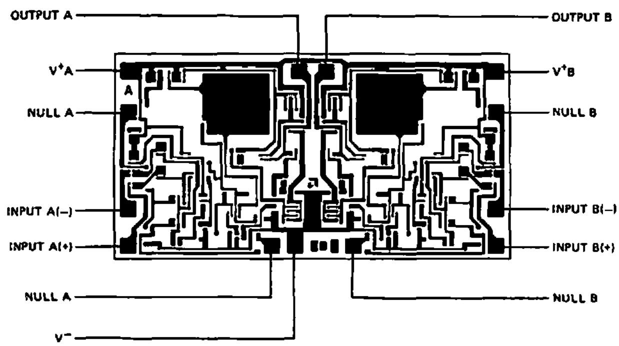


POSITIVE OUTPUT = $V_{Q1} \times \frac{R_1 + R_2}{R_2}$

NEGATIVE OUTPUT = −POSITIVE OUTPUT × $\frac{R_6}{R_5}$

LIC-782

Metallization and Pad Layout



56 x 106 Mils

Am748/748C

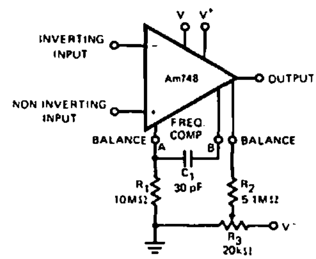
Operational Amplifier

Description: The Am748/748C Monolithic Operational Amplifiers are functionally, electrically, and pin-for-pin equivalent to the Fairchild μA748 and μA748C. Both are available in the hermetic metal can, dual-in-line, and flat packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883 Class B.
Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION:
The Am748 and Am748C are differential input class AB output amplifiers intended for general-purpose application. They are protected against faults at input and output, and may be frequency compensated with an external 30 pF capacitor.

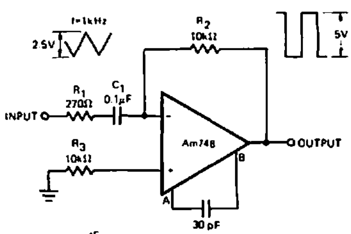
FUNCTIONAL DIAGRAM



LIC-783

APPLICATIONS

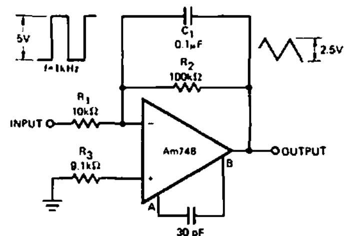
DIFFERENTIATOR



$E_{OUT} = -R_2C_1\frac{dE_{IN}}{dt}$

LIC-784

INTEGRATOR



$E_{OUT} = -\frac{1}{R_1C_1}\int E_{IN}dt$

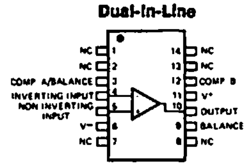
LIC-785

ORDERING INFORMATION

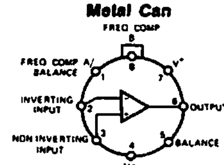
Part Number	Package Type	Temperature Range	Order Number
	Metal Can	0°C to +70°C	748HC
Am748C	Hermetic DIP	0°C to +70°C	748DC
	Dice	0°C to +70°C	748XC
	Metal Can	–55°C to +125°C	748HM
Am748	Hermetic DIP	–55°C to +125°C	748DM
	Dice	–55°C to +125°C	748XM

CONNECTION DIAGRAMS
Top Views

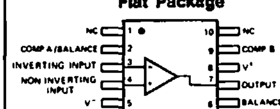
Dual-In-Line



Metal Can



Flat Package



LIC-786

NOTES:
(1) On Metal Can, pin 4 is connected to case.
(2) On DIP, pin 6 is connected to bottom of package.
(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage Am748 Am748C	 ±22 V ±18 V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range Am748 Am748C	 −55°C to +125°C 0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

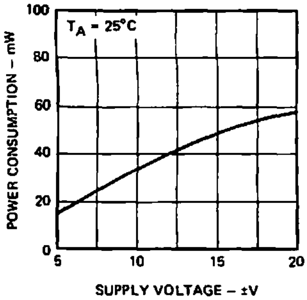
Parameter (see definitions)	Conditions	Am748C Min.	Am748C Typ.	Am748C Max.	Am748 Min.	Am748 Typ.	Am748 Max.	Units
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0		1.0	5.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Input Capacitance			1.4			1.4		pF
Offset Voltage Adjustment Range			±15			±15		mV
Input Voltage Range		±12	±13		±12	±13		V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	50	200		50	200		V/mV
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Current			1.7	2.8		1.7	2.8	mA
Power Consumption			50	85		50	85	mW
Transient Response (unity gain) Risetime Overshoot	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF		 0.3 5.0			 0.3 5.0		 μs %
Slew Rate	$R_L \geq 2$ kΩ	0.2	0.5		0.2	0.5		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5			6.0	mV
Input Offset Current	$T_{A(max)}$ $T_{A(min)}$		9.0 35	300 300		7.0 85	200 500	nA nA
Input Bias Current	$T_{A(max)}$ $T_{A(min)}$		0.04 0.13	0.8 0.8		0.03 0.3	0.5 1.5	μA μA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25			25			V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ $R_L \geq 2$ kΩ	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Supply Current	$T_{A(max)}$ $T_{A(min)}$		1.6 1.8	3.3 3.3		1.5 2.0	2.5 3.3	mA mA
Power Consumption	$T_{A(max)}$ $T_{A(min)}$		48 54	100 100		45 60	75 100	mW mW

Notes: 1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C.
2. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

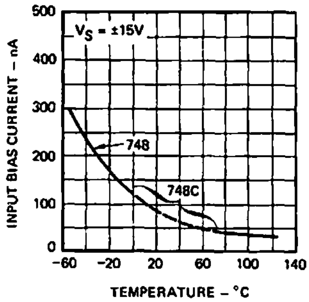
6

PERFORMANCE CURVES

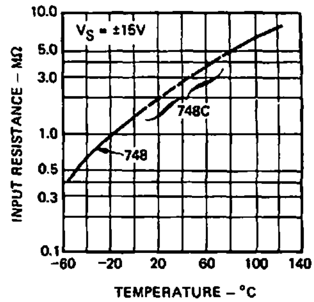
Power Consumption As A Function Of Supply Voltage



Input Bias Current As A Function Of Ambient Temperature

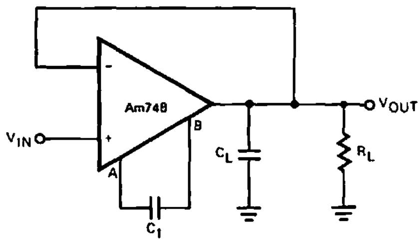


Input Resistance As A Function Of Ambient Temperature



LIC-787

TRANSIENT RESPONSE TEST CIRCUIT

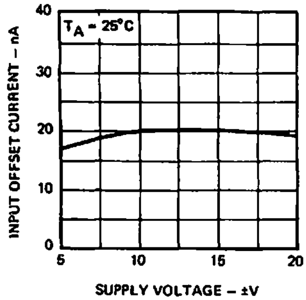


LIC-788

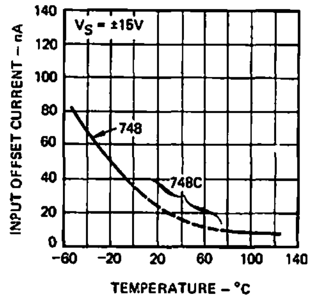
$C_L \leq 100$ pF
$R_L = 2$ kΩ

PERFORMANCE CURVES

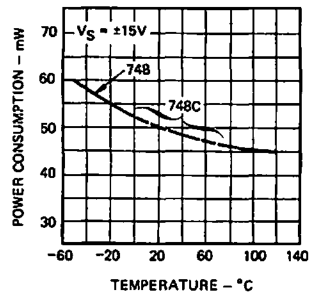
Input Offset Current As A Function Of Supply Voltage



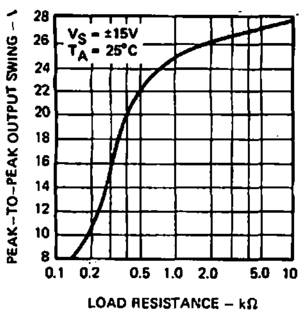
Input Offset Current As A Function Of Ambient Temperature



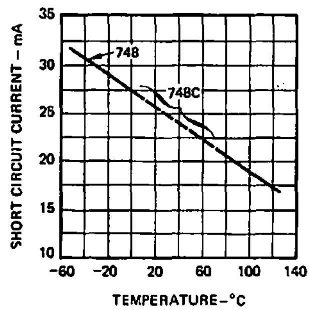
Power Consumption As A Function Of Ambient Temperature



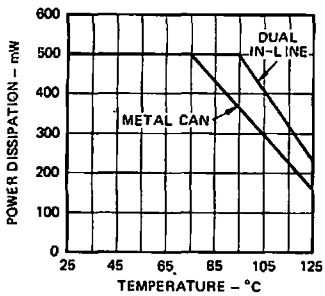
Output Voltage Swing As A Function Of Load Resistance



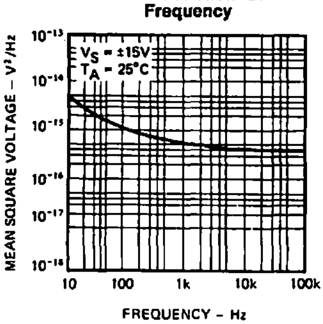
Output Short-Circuit Current As A Function Of Ambient Temperature



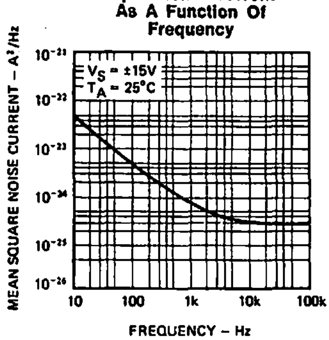
Absolute Maximum Power Dissipation As A Function Of Ambient Temperature



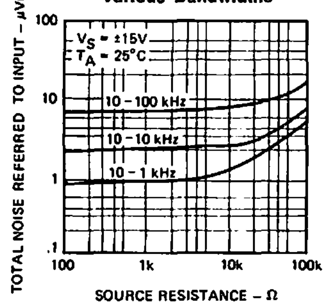
Input Noise Voltage As A Function Of Frequency



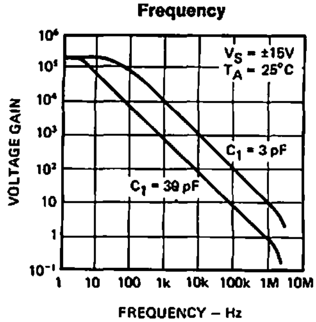
Input Noise Current As A Function Of Frequency



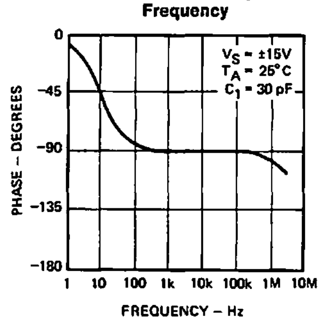
Broadband Noise For Various Bandwidths



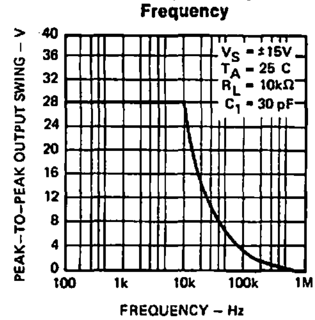
Open Loop Voltage Gain As A Function Of Frequency



Open Loop Phase Response As A Function Of Frequency



Output Voltage Swing As A Function Of Frequency

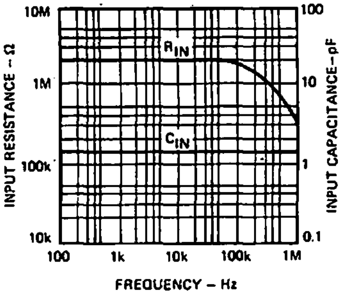


LIC-789

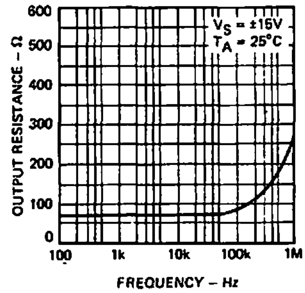
6

PERFORMANCE CURVES

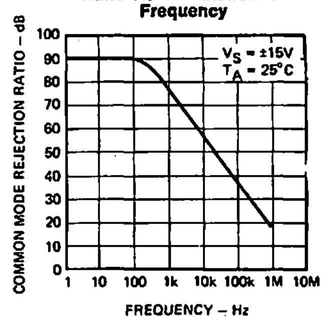
Input Resistance And Input Capacitance As A Function Of Frequency



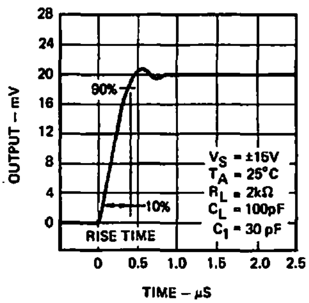
Output Resistance As A Function Of Frequency



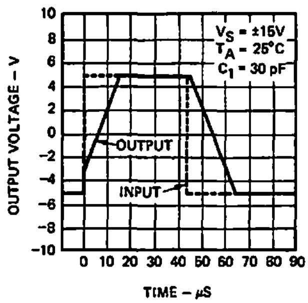
Common Mode Rejection Ratio As A Function Of Frequency



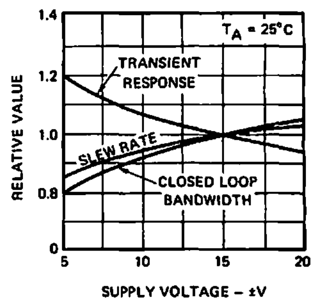
Transient Response



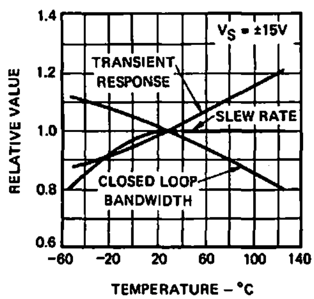
Voltage Follower Large-Signal Pulse Response



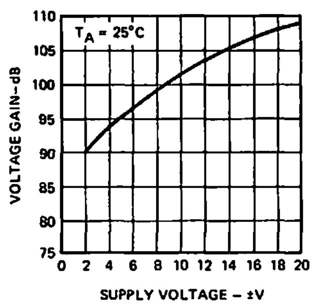
Frequency Characteristics As A Function Of Supply Voltage



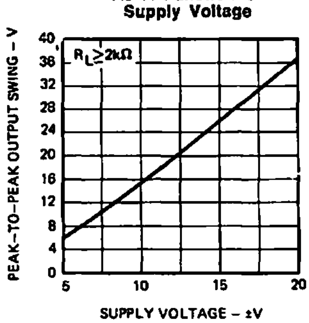
Frequency Characteristics As A Function Of Ambient Temperature



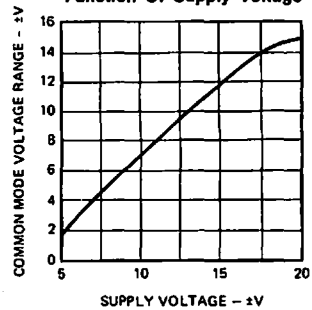
Open Loop Voltage Gain As A Function Of Supply Voltage



Output Voltage Swing As A Function Of Supply Voltage



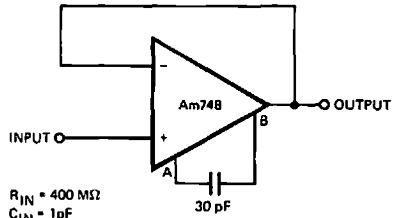
Input Common Mode Voltage Range As A Function Of Supply Voltage



LIC-790

BASIC Am748 AMPLIFIER APPLICATIONS

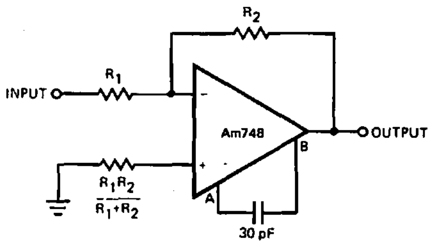
UNITY GAIN VOLTAGE FOLLOWER



R_{IN} = 400 MΩ
C_{IN} = 1pF
R_{OUT} << 1Ω
B.W. = 1 MHz

LIC-791

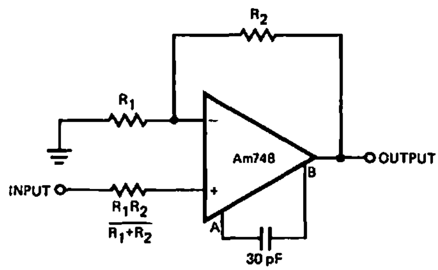
INVERTING AMPLIFIER



GAIN	R_1	R_2	B.W.	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

LIC-792

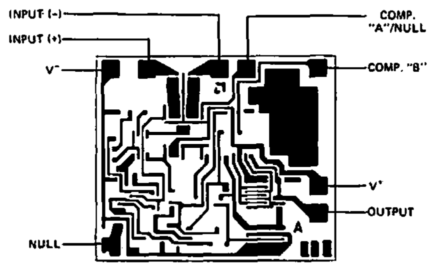
NON-INVERTING AMPLIFIER



GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

LIC-793

Metallization and Pad Layout



49 x 56 Mils

Am1501

Dual Operational Amplifiers

Distinctive Characteristics

- Low offset voltage
- Low offset current
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

FUNCTIONAL DESCRIPTION

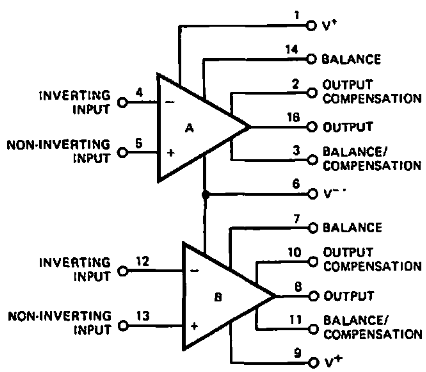
The Am1501 series are differential input, class AB output operational amplifiers. The inputs and outputs are protected against overload and the amplifiers may be frequency compensated with an external 30pF capacitor. The combination of low-input currents, low-offset voltage, low noise, and versatility of compensation classify the Am1501 series amplifiers for low level and general purpose applications.

DESCRIPTION

The Am1501 series of dual operational amplifiers are two LM101A type op amps in a single hermetic package. They are functionally, electrically and pin-for-pin equivalent to the National LH2101A series. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost, and smaller size than two singles.

The Am1501M is specified for operation over the −55°C to +125°C military temperature range. The Am1501L is specified for operation over the −25°C to +85°C temperature range. The Am1501C is specified for operation over the 0°C to +70°C temperature range.

FUNCTIONAL DIAGRAM

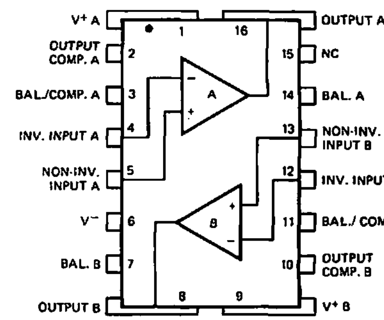


LIC-794

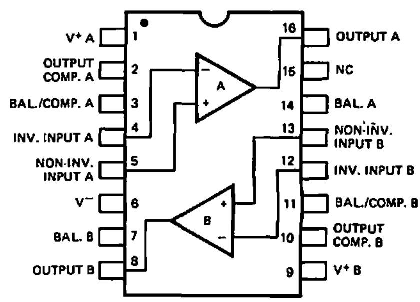
CONNECTION DIAGRAMS

Top Views

Dual-In-Line



Flat Package



Note: Pin 1 is marked for orientation.

LIC-795

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am1501C	Hermetic Dip	0°C to +70°C	AM1501DC
	Flat Pak	0°C to +70°C	AM1501FC
Am1501L	Hermetic Dip	−25°C to +85°C	AM1501DL
	Flat Pak	−25°C to +85°C	AM1501FL
Am1501M	Hermetic Dip	−55°C to +125°C	AM1501DM
	Flat Pak	−55°C to +125°C	AM1501FM

MAXIMUM RATINGS

Supply Voltage	
Am1501M, Am1501L	±22V
Am1501C	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am1501M	−55°C to +125°C
Am1501L	−25°C to + 85°C
Am1501C	0°C to + 85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

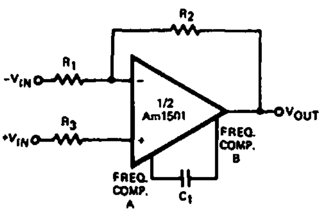
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 3) (EACH AMPLIFIER)

Parameter (see definitions)	Conditions	Am1501C Min.	Am1501C Typ.	Am1501C Max.	Am1501M Am1501L Min.	Am1501M Am1501L Typ.	Am1501M Am1501L Max.	Units
Input Offset Voltage	R_S < 50kΩ		2.0	7.5		0.7	2.0	mV
Input Offset Current			3.0	50		1.5	10	nA
Input Bias Current			70	250		30	75	nA
Input Resistance		0.5	2.0		1.5	4.0		MΩ
Supply Current (Total Both Amplifiers)	V_S = ±20V					3.6	6.0	mA
	V_S = ±15V		3.6	6.0				mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, R_L > 2.0kΩ	25	160		50	160		V/mV
Slew Rate	V_S = ±20V, A_V = +1.0	0.2	0.5		0.2	0.5		V/µs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	R_S < 50kΩ			10			3.0	mV
Input Offset Current				70			20	nA
Average Temperature Coefficient of Input Offset Voltage	$T_{A(min.)} < T_A < T_{A(max.)}$		6.0	30		3.0	15	µV/°C
Average Temperature Coefficient of Input Offset Current	25°C < T_A < $T_{A(max.)}$		0.01	0.3		0.01	0.1	nA/°C
	$T_{A(min.)}$ < T_A < 25°C		0.02	0.6		0.02	0.2	nA/°C
Input Bias Current				300			100	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, R_L > 2.0kΩ	25			25			V/mV
Input Voltage Range	V_S = ±20V				±15			V
	V_S = ±15V	+15,−12						V
Common Mode Rejection Ratio	R_S < 50kΩ	70	90		80	96		dB
Supply Voltage Rejection Ratio	R_S < 50kΩ	70	96		80	96		dB
Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±12	±14		±12	±14		V
	R_L = 2.0kΩ	±10	±13		±10	±13		V
Supply Current (Total Both Amplifiers)	T_A = +125°C, V_S = ±20V					2.4	5.0	mA

Notes:
1. The maximum junction temperature of the Am1501M is 150°C, while that of the Am1501L and Am1501C is 100°C. For operating temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. These specifications apply for ±5V ≤ V_S ≤ ±20V and −55°C ≤ T_A ≤ +125°C, unless otherwise specified. With the Am1501L, however, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C. For the Am1501C these specifications apply for 0°C ≤ T_A ≤ +70°C, ±5V and ≤ V_S ≤ ±15V. Supply current and input voltage range are specified as V_S = ±15V for the Am1501C. C_1 = 30pF unless otherwise specified.

FREQUENCY COMPENSATION CIRCUITS

Single Pole Compensation

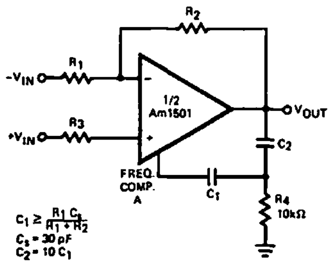


$C_1 \geq \frac{R_1 C_s}{R_1 + R_2}$
$C_s = 30\,pF$

Figure 1

LIC-796

Two Pole Compensation

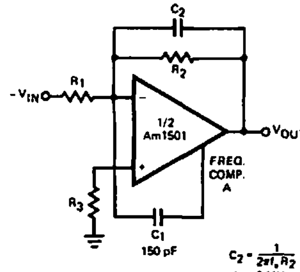


$C_1 \geq \frac{R_1 C_s}{R_1 + R_2}$
$C_s = 30\,pF$
$C_2 = 10\,C_1$

Figure 2

LIC-797

Feedforward Compensation



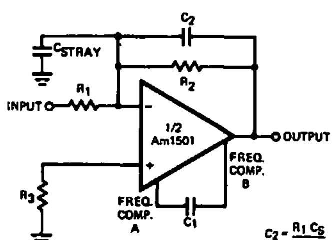
$C_2 = \frac{1}{2\pi f_o R_2}$
$f_o = 3\,MHz$

Figure 3

LIC-798

Power supplies should be bypassed to ground at one point, minimum, on each card. More bypass points should be considered for five or more amplifiers on a single card. For applications using feed-forward compensation, the power supply leads of each amplifier should be bypassed with low inductance capacitors.

Compensating for
Stray Input Capacitance/Large
Feedback Resistance



$C_2 = \frac{R_1 C_S}{R_2}$

Figure 4

LIC-799

Isolating Large Capacitive Loads

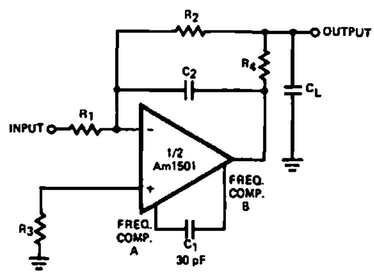


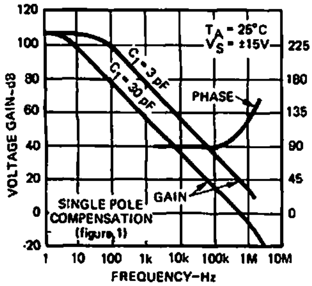
Figure 5

LIC-800

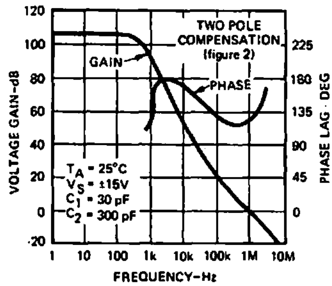
The values given for the frequency compensation capacitor guarantee stability only for source resistances less than 10kΩ, stray capacitances on the summing junction less than 5pF and capacitive loads smaller than 100pF. If any of these conditions is not met, it is necessary to use a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors, or an RC network can be added to isolate capacitive loads.

PERFORMANCE CURVES (Note 3)

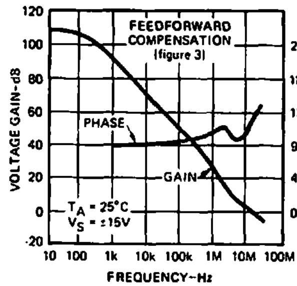
Open Loop Frequency Response



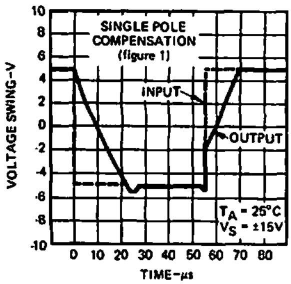
Open Loop Frequency Response



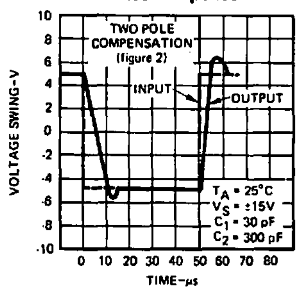
Open Loop Frequency Response



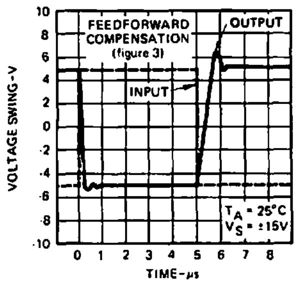
Voltage Follower Pulse Response



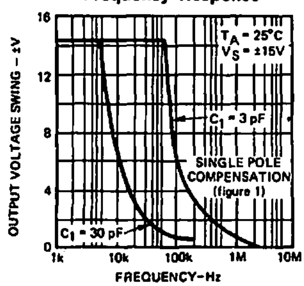
Voltage Follower Pulse Response



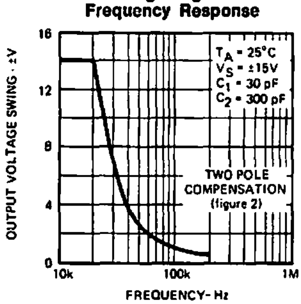
Inverter Pulse Response



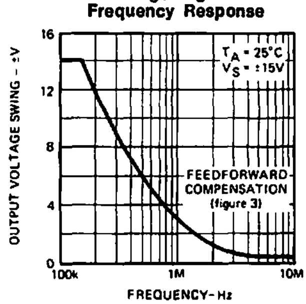
Large Signal Frequency Response



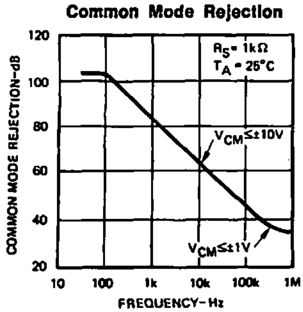
Large Signal Frequency Response



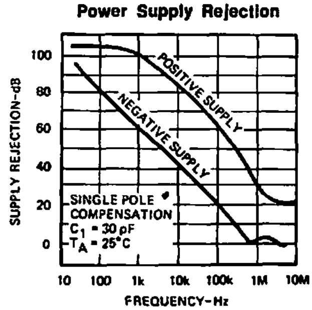
Large Signal Frequency Response



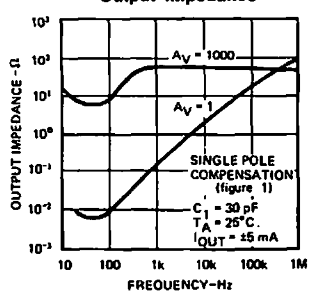
Common Mode Rejection



Power Supply Rejection



Closed Loop Output Impedance

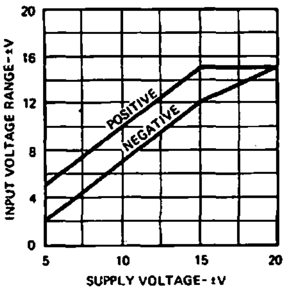


LIC-801

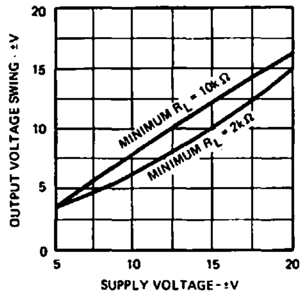
GUARANTEED PERFORMANCE CURVES (Note 3)

(Curves apply over the Operating Temperature Ranges)

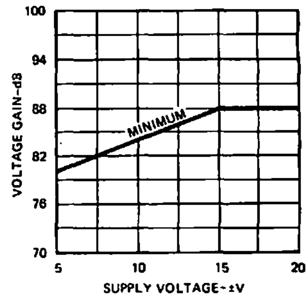
Input Voltage Range



Output Swing

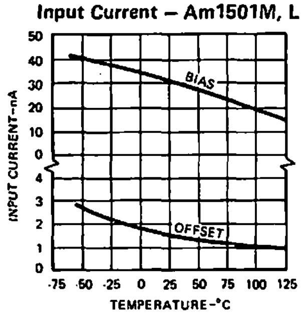


Voltage Gain

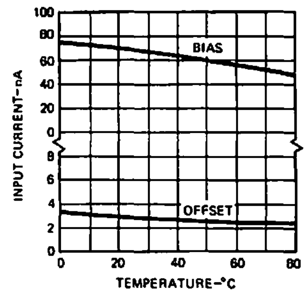


PERFORMANCE CURVES (Note 3)

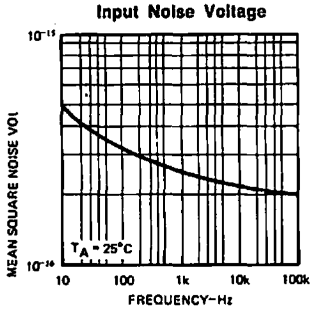
Input Current – Am1501M, L



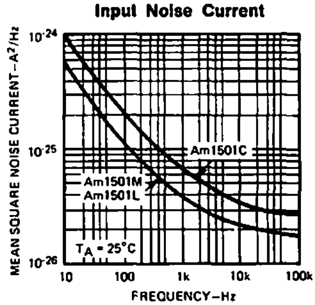
Input Current – Am1501C



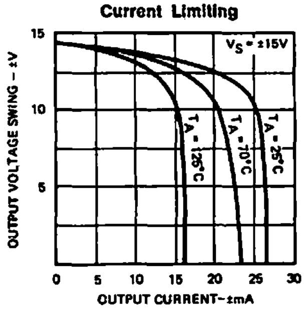
Input Noise Voltage



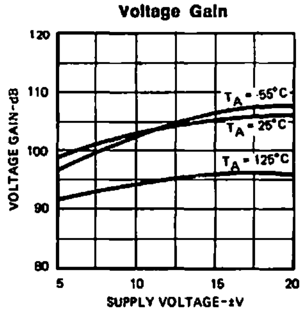
Input Noise Current



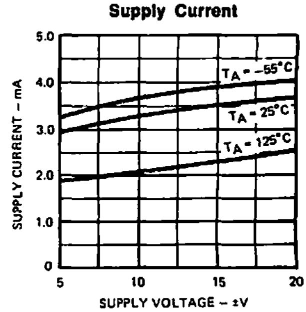
Current Limiting



Voltage Gain



Supply Current



LIC-802

Am1558/1458

Dual Frequency Compensated Operational Amplifiers

Description

The Am1558 and Am1458 Dual Frequency Compensated Operational Amplifiers are functionally, electrically, and pin-for-pin equivalent to the Motorola MC1558 and MC1438. Both are available in the hermetic metal can package.

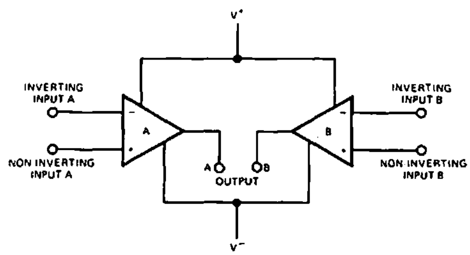
Distinctive Characteristics

- 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL-STD-883
- Electrically tested and optically inspected dice for the assemblers of hybrid circuits

FUNCTIONAL DESCRIPTION

The Am1558 is a dual 741 internally compensated operational amplifier. The Am1558 and Am1458 are differential input, class AB output amplifiers intended for general purpose applications. They are protected against faults at input and output, and require no external components for frequency compensation.

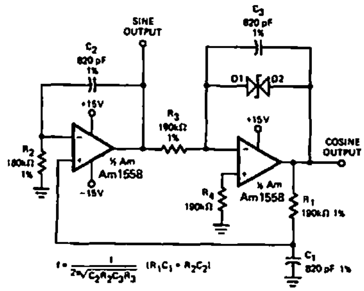
FUNCTIONAL DIAGRAM



LIC-803

APPLICATIONS

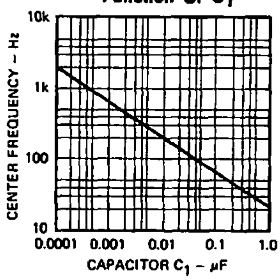
QUADRATURE OSCILLATOR



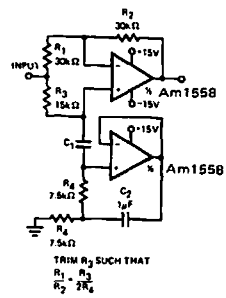
LIC-804

NOTCH FILTER USING THE 1558 AS A GYRATOR

Notch Frequency As A Function Of C_1



LIC-805



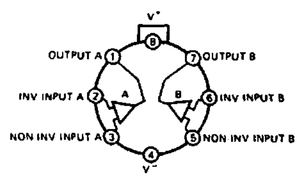
LIC-806

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am1458	Metal Can	0°C to +70°C	AM1458H
	Dice	0°C to +70°C	LD1458
Am1558	Metal Can	−55°C to +125°C	AM1558H
	Dice	−55°C to +125°C	LD1558

See Am747 for dice layout

CONNECTION DIAGRAM
Top View



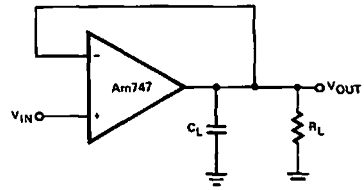
Note: Pin 4 Connected to Case.

LIC-807

MAXIMUM RATINGS

Supply Voltage	
Am1558	±22V
Am1458	±18V
Internal Power Dissipation (Note 1)	
Metal Can	800mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
Am1558	−55°C to +125°C
Am1458	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

Transient Response Test Circuit



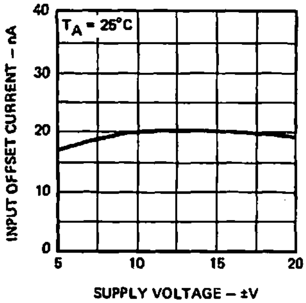
ELECTRICAL CHARACTERISTICS–Each Amplifier (V_S = ±15V, T_A = 25°C unless otherwise specified)

Parameter (see definitions)	Conditions	Am1458 Min.	Am1458 Typ.	Am1458 Max.	Am1558 Min.	Am1558 Typ.	Am1558 Max.	Units
Input Offset Voltage	R_S < 10kΩ		2.0	6.0		1.0	5.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Input Capacitance			1.4			1.4		pF
Offset Voltage Adjustment Range			±15			±15		mV
Input Voltage Range		±12	±13		±12	±13		V
Large-Signal Voltage Gain	R_L > 2.0kΩ, V_{OUT} = ±10V	20	100		50	200		V/mV
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Voltage Rejection Ratio	R_S < 10kΩ		30	150		30	150	μV/V
Common Mode Rejection Ratio	R_S < 10kΩ	70	90		70	90		dB
Supply Current (Both Amplifiers)			3.4	5.6		3.4	5.6	mA
Power Consumption (Both Amplifiers)			100	170		100	170	mW
Transient Response (Unity Gain) Risetime / Overshoot	V_{IN} = 20mV, R_L = 2.0kΩ, C_L < 100pF		0.3 / 5.0			0.3 / 5.0		μs / %
Slew Rate	R_L > 2.0kΩ	0.3	0.5		0.3	0.5		V/μs
Channel Separation	R_S = 50Ω, R_L' > 10kΩ		120			120		dB
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	R_S < 10kΩ			7.5			6.0	mV
Input Offset Current	T_A MAX. / T_A MIN.		9.0 / 35	300 / 300		7.0 / 85	200 / 500	nA
Input Bias Current	T_A MAX. / T_A MIN.		0.04 / 0.13	0.8 / 0.8		0.03 / 0.3	0.5 / 1.5	μA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	R_S < 10kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	R_S < 10kΩ		30	150		30	150	μV/V
Large-Signal Voltage Gain	R_L > 2.0kΩ, V_{OUT} = ±10V	15			25			V/mV
Output Voltage Swing	R_L > 10kΩ / R_L > 2.0kΩ	±12 / ±10	±14 / ±13		±12 / ±10	±14 / ±13		V
Supply Current (Both Amplifiers)	T_A MAX. / T_A MIN.		1.6 / 1.8	3.3 / 3.3		3.0 / 4.0	5.0 / 6.6	mA
Power Consumption (Both Amplifiers)	T_A MAX. / T_A MIN.		100 / 110	170 / 200		90 / 120	150 / 200	mW

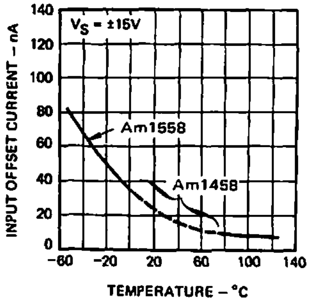
Notes: 1. Derate Metal Can package at 6.8mW/°C for operation at ambient temperatures above 30°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be ground or either supply. Rating applies to +125°C case temperature or +60°C ambient temperature for each side.

PERFORMANCE CURVES
(Each Amplifier)

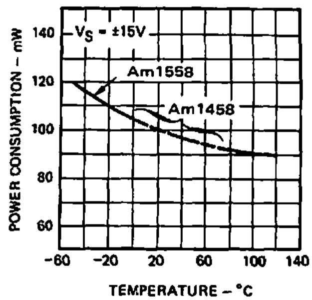
Input Offset Current As A Function Of Supply Voltage



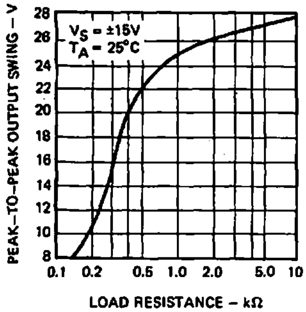
Input Offset Current As A Function Of Ambient Temperature



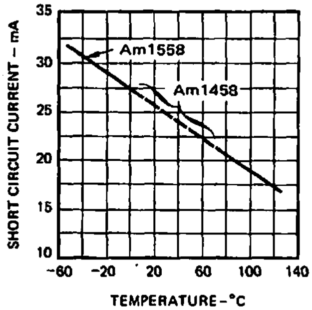
Power Consumption As A Function Of Ambient Temperature



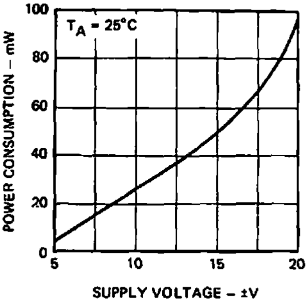
Output Voltage Swing As A Function Of Load Resistance



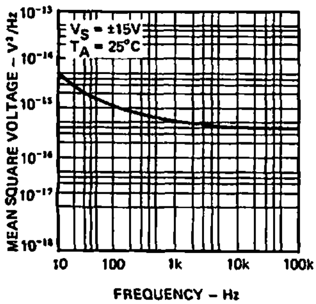
Output Short-Circuit Current As A Function Of Ambient Temperature



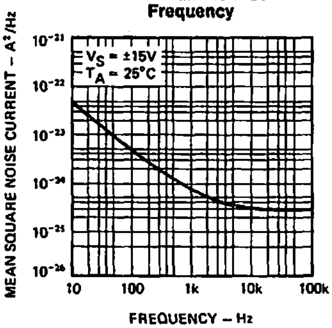
Power Consumption As A Function Of Supply Voltage



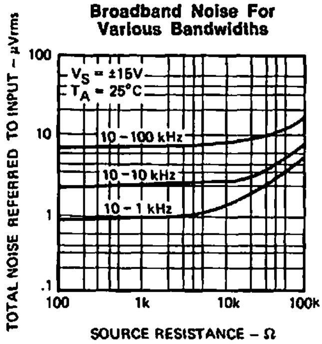
Input Noise Voltage As A Function Of Frequency



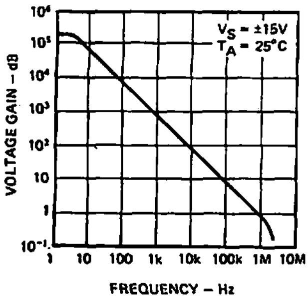
Input Noise Current As A Function Of Frequency



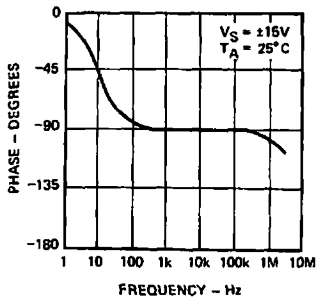
Broadband Noise For Various Bandwidths



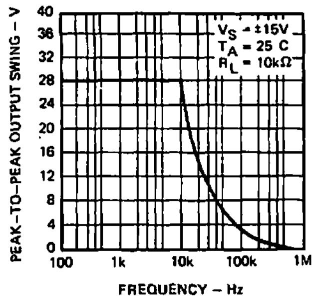
Open Loop Voltage Gain As A Function Of Frequency



Open Loop Phase Response As A Function Of Frequency



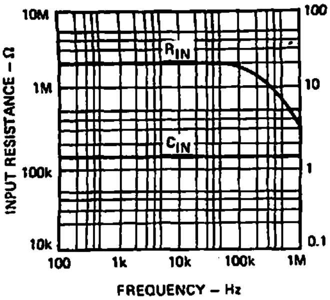
Output Voltage Swing As A Function Of Frequency



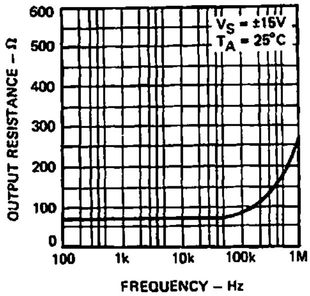
LIC-809

PERFORMANCE CURVES
(Each Amplifier)

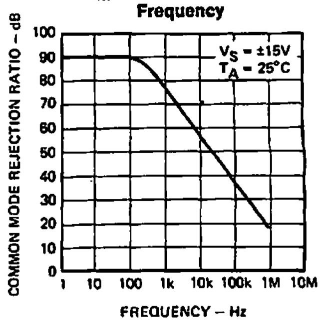
Input Resistance And Input Capacitance As A Function Of Frequency



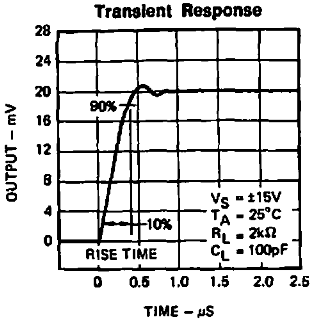
Output Resistance As A Function Of Frequency



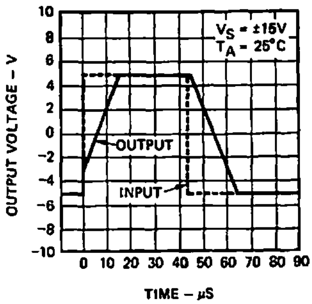
Common Mode Rejection Ratio As A Function Of Frequency



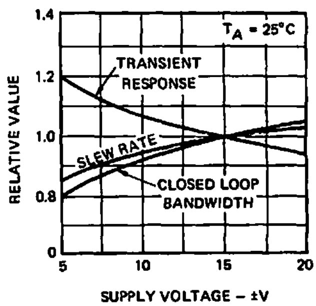
Transient Response



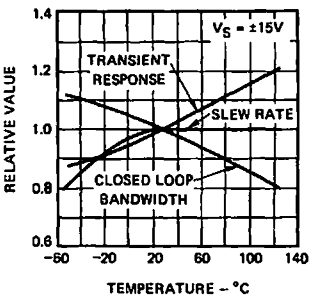
Voltage Follower Large-Signal Pulse Response



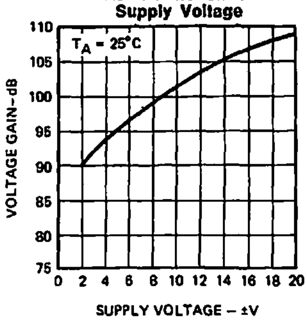
Frequency Characteristics As A Function Of Supply Voltage



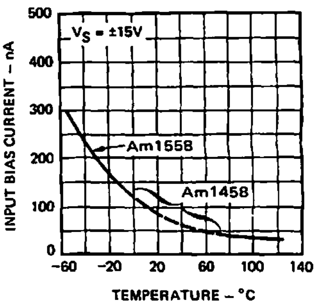
Frequency Characteristics As A Function Of Ambient Temperature



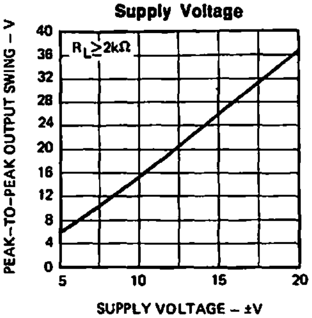
Open Loop Voltage Gain As A Function Of Supply Voltage



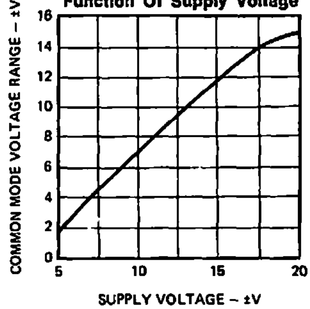
Input Bias Current As A Function Of Ambient Temperature



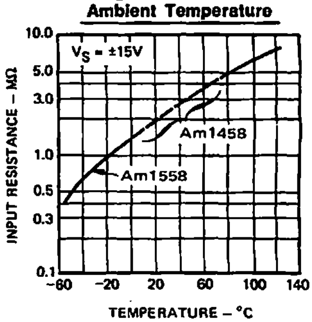
Output Voltage Swing As A Function Of Supply Voltage



Input Common Mode Voltage Range As A Function Of Supply Voltage



Input Resistance As A Function Of Ambient Temperature



LIC-810

LH2101A/LH2201A/LH2301A

Dual Operational Amplifiers

Distinctive Characteristics

- Low offset voltage
- Low offset current
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

FUNCTIONAL DESCRIPTION

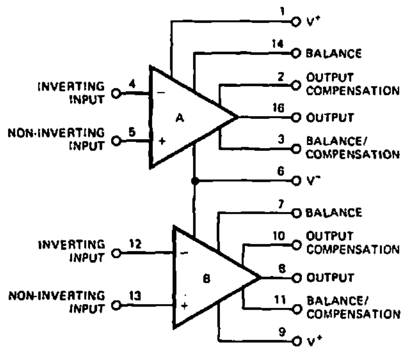
The LH2101A series are differential input, class AB output operational amplifiers. The inputs and outputs are protected against overload and the amplifiers may be frequency compensated with an external 30pF capacitor. The combination of low-input currents, low-offset voltage, low noise, and versatility of compensation classify the LH2101A series amplifiers for low level and general purpose applications.

DESCRIPTION

The LH2101A series of dual operational amplifiers are two LM101A type op amps in a single hermetic package. They are functionally electrically and pin for pin equivalent to the National LH2101A series. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost, and smaller size than two singles.

The LH2101A is specified for operation over the −55°C to +125°C military temperature range. The LH2201A is specified for operation over the −25°C to +85°C temperature range. The LH2301A is specified for operation over the 0°C to +70°C temperature range.

FUNCTIONAL DIAGRAM



LIC-811

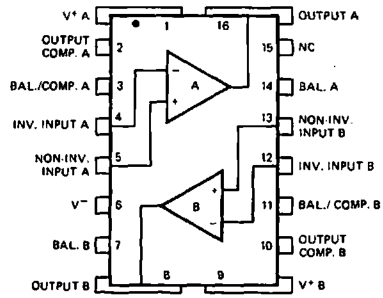
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
LH2301A	DIP	0°C to +70°C	LH2301AD
	Flat Pak	0°C to +70°C	LH2301AF
LH2201A	DIP	-25°C to +85°C	LH2201AD
	Flat Pak	-25°C to +85°C	LH2201AF
LH2101A	DIP	-55°C to +125°C	LH2101AD
	Flat Pak	-55°C to +125°C	LH2101AF

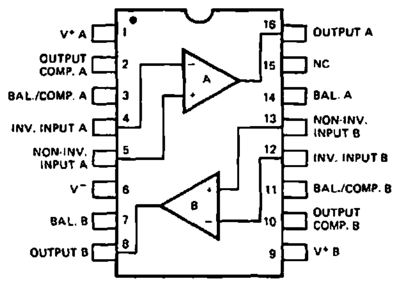
CONNECTION DIAGRAMS

Top Views

Dual-In-Line



Flat Package



Note: Pin 1 is marked for orientation.

LIC-812

6

MAXIMUM RATINGS

Supply Voltage	
LH2101A, LH2201A	±22V
LH2301A	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
LH2101A	−55°C to +125°C
LH2201A	−25°C to +85°C
LH2301A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 3)

(Each Amplifier)

Parameter (see definitions)	Conditions	LH2301A Min.	LH2301A Typ.	LH2301A Max.	LH2101A LH2201A Min.	LH2101A LH2201A Typ.	LH2101A LH2201A Max.	Units
Input Offset Voltage	$R_S < 50k\Omega$		2.0	7.5		0.7	2.0	mV
Input Offset Current			3.0	50		1.5	10	nA
Input Bias Current			70	250		30	75	nA
Input Resistance		0.5	2.0		1.5	4.0		MΩ
Supply Current (Total Both Amplifiers)	$V_S = \pm 20V$					3.6	6.0	mA
	$V_S = \pm 15V$		3.6	6.0				
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L > 2k\Omega$	25	160		50	160		V/mV
Slew Rate	$V_S = \pm 20V$, $A_V = +1$	0.2	0.5		0.2	0.5		V/µs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 50k\Omega$			10			3.0	mV
Input Offset Current				70			20	nA
Average Temperature Coefficient of Input Offset Voltage	$T_{A(MIN)} \leq T_A \leq T_{A(MAX)}$		6.0	30		3.0	15	µV/°C
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{A(MAX)}$		0.01	0.3		0.01	0.1	nA/°C
	$T_{A(MIN)} \leq T_A \leq 25°C$		0.02	0.6		0.02	0.2	
Input Bias Current				300			100	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L > 2k\Omega$	25			25			V/mV
Input Voltage Range	$V_S = \pm 20V$				±15			Volts
	$V_S = \pm 15V$	+15,−12						
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	70	90		80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 50k\Omega$	70	96		80	96		dB
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	±12	±14		±12	±14		Volts
	$R_L = 2k\Omega$	±10	±13		±10	±13		
Supply Current (Total Both Amplifiers)	$T_A = +125°C$, $V_S = \pm 20V$					2.4	5.0	mA

Notes: 1. The maximum junction temperature of the LH2101A is 150°C, while that of the LH2201A and LH2301A is 100°C. For operating temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

3. These specifications apply for $\pm 5V \leq V_S \leq +20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LH2201A, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$. For the LH2301A these specifications apply for $0°C \leq T_A \leq 70°C$, ±5V and $\leq V_S \leq \pm 15V$. Supply current and input voltage range are specified as $V_S = \pm 5V$ for the LH2301A. C_1 = 30pF unless otherwise specified.

FREQUENCY COMPENSATION CIRCUITS

Single Pole Compensation

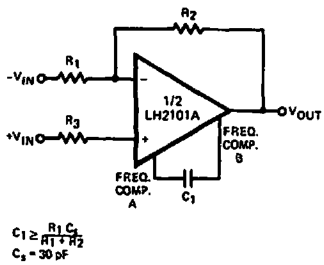


Figure 1

LIC-813

Two Pole Compensation

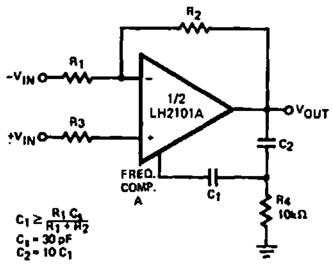


Figure 2

LIC-814

Feedforward Compensation

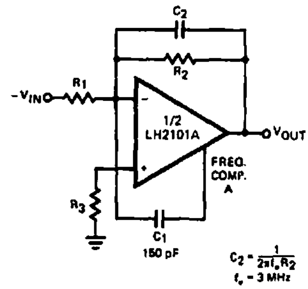
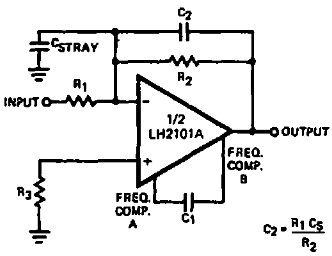


Figure 3

LIC-815

Power supplies should be bypassed to ground at one point, minimum, on each card. More bypass points should be considered for five or more amplifiers on a single card. For applications using feed-forward compensation, the power supply leads of each amplifier should be bypassed with low inductance capacitors.

Compensating for Stray Input Capacitance/Large Feedback Resistance



LIC-816

Figure 4

Isolating Large Capacitive Loads

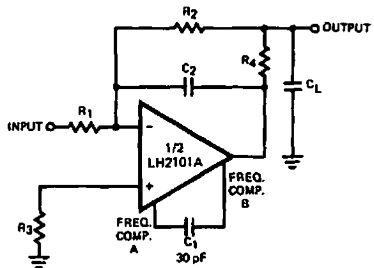
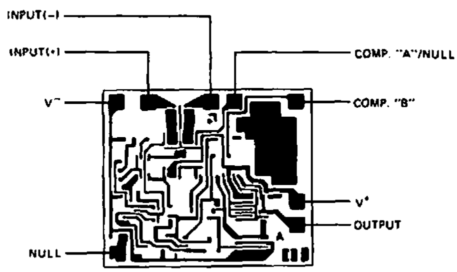


Figure 5

LIC-817

The values given for the frequency compensation capacitor guarantee stability only for source resistances less than 10kΩ, stray capacitances on the summing junction less than 5pF and capacitive loads smaller than 100pF. If any of these conditions is not met, it is necessary to use a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors, or an RC network can be added to isolate capacitive loads.

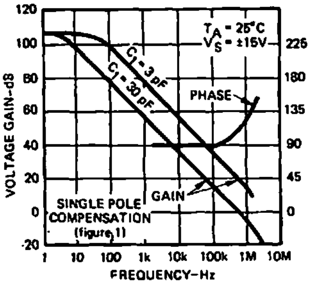
Metallization and Pad Layout



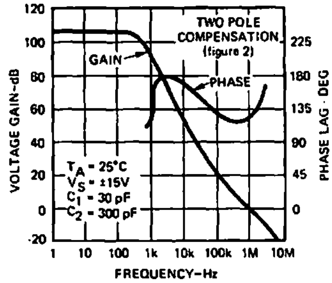
49 X 56 Mils

PERFORMANCE CURVES (Note 3)

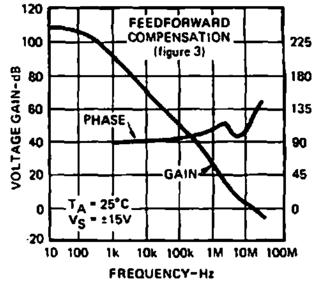
Open Loop Frequency Response



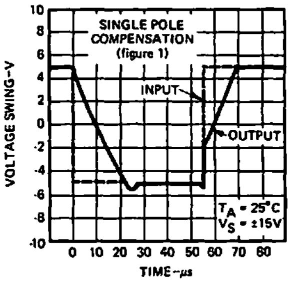
Open Loop Frequency Response



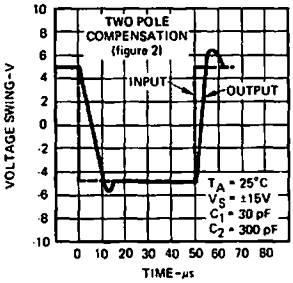
Open Loop Frequency Response



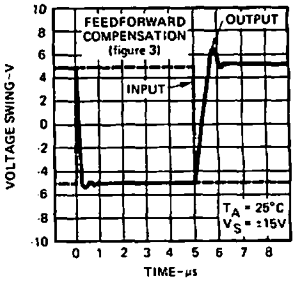
Voltage Follower Pulse Response



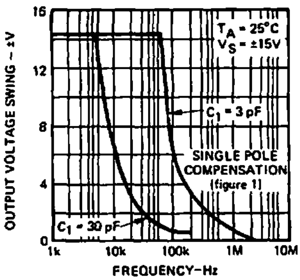
Voltage Follower Pulse Response



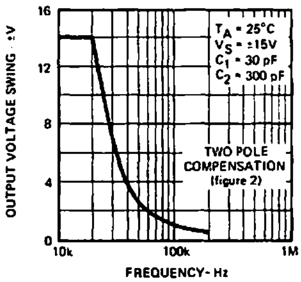
Inverter Pulse Response



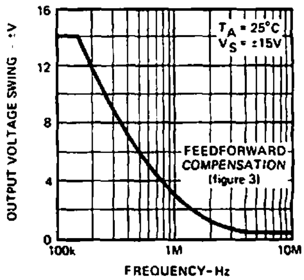
Large Signal Frequency Response



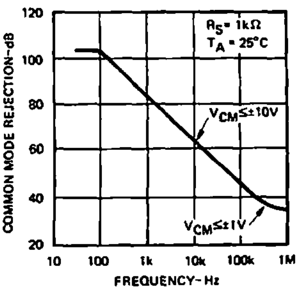
Large Signal Frequency Response



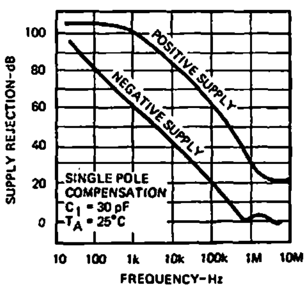
Large Signal Frequency Response



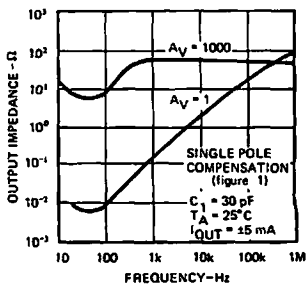
Common Mode Rejection



Power Supply Rejection



Closed Loop Output Impedance

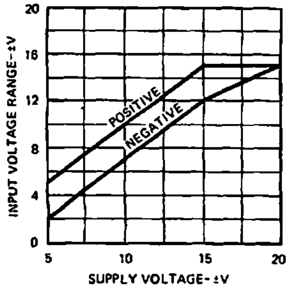


LIC-818

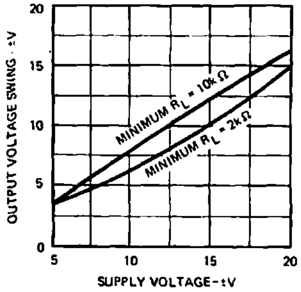
GUARANTEED PERFORMANCE CURVES (Note 3)

(Curves apply over the Operating Temperature Ranges)

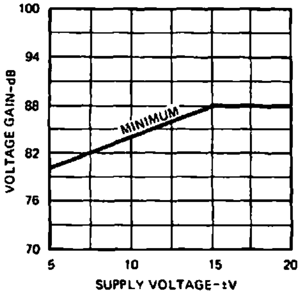
Input Voltage Range



Output Swing

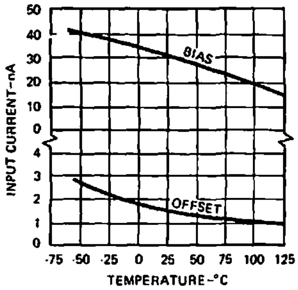


Voltage Gain

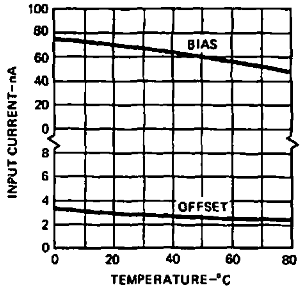


PERFORMANCE CURVES (Note 3)

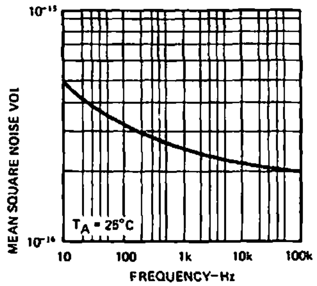
Input Current – LH2101A, LH2201A



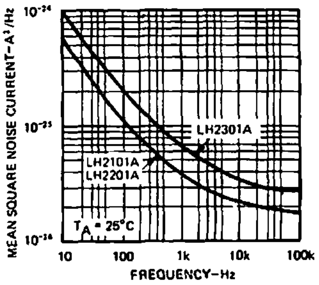
Input Current – LH2301A



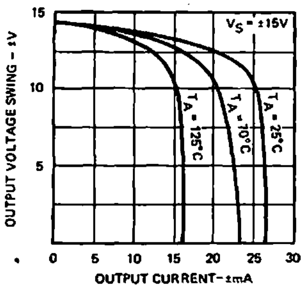
Input Noise Voltage



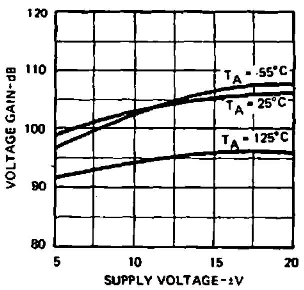
Input Noise Current



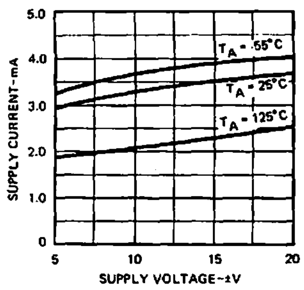
Current Limiting



Voltage Gain



Supply Current



LIC-619

6

Special Functions – Section VII

Am592

Differential Video Amplifier

PRELIMINARY DATA

Distinctive Characteristics

- The Am592 and Am592C differential video amplifiers are functionally, electrically and pin-for-pin equivalent to the Signetics SE592 and NE592.
- Bandwidths: 40 to 120 MHz
- Rise times: 2.5 to 10 ns
- Propagation delay: 3.6 to 10 ns
- 100% reliability assurance testing in compliance with MIL-STD-883A
- Electrically tested and optically inspected dice for hybrid manufacturers
- 120 MHz bandwidth
- Adjustable gains from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Available in metal can, hermetic dual-in-line or plastic dual-in-line packages

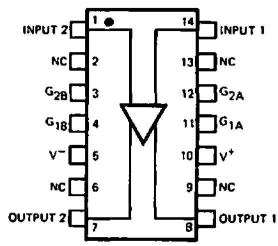
FUNCTIONAL DESCRIPTION

The Am592/Am592C is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems.

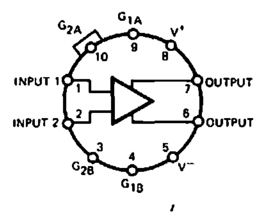
CONNECTION DIAGRAMS

Top Views

Dual-In-Line



Metal Can



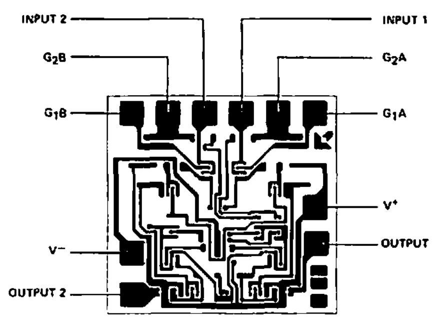
Note: On Metal Can, pin 5 is conneted to case.

LIC-820

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am592C	TO-100	0°C to +70°C	AM592HC
	DIP	0°C to +70°C	AM592DC
	Molded DIP	0°C to +70°C	AM592PC
	Dice	0°C to +70°C	LD592C
Am592	TO-100	−55°C to +125°C	AM592HM
	DIP	−55°C to +125°C	AM592DM
	Dice	−55°C to +125°C	LD592

Metallization and Pad Layout



DIE SIZE 41 X 41 mils

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8V
Differential Input Voltage	±5V
Common Mode Input Voltage	±6V
Output Current	10mA
Operating Temperature Range Am592 Am592C	 –55°C to +125°C 0°C to + 70°C
Storage Temperature Range	–65°C to +150°C

ELECTRICAL CHARACTERISTICS Standard Conditions (T_A = +25°C, V_S = ±6V, V_{CM} = 0 unless otherwise specified)

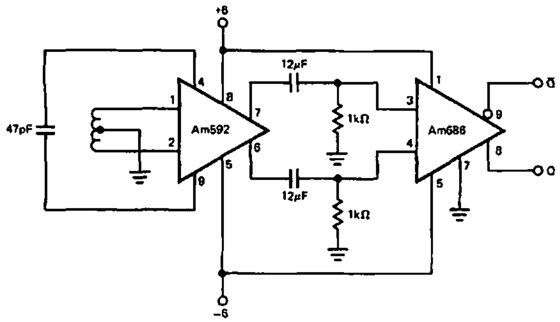
Parameter			Conditions	Am592C Min.	Am592C Typ.	Am592C Max.	Am592 * Min.	Am592 * Typ.	Am592 * Max.	Units
Differential Voltage Gain	Gain 1	Note 1	R_L = 2kΩ, V_{OUT} = 3V p-p	250	400	600	300	400	500	
	Gain 2	Note 2		80	100	120	90	100	110	
Bandwidth	Gain 1	Note 1			40			40		MHz
	Gain 2	Note 2			90			90		
Rise Time	Gain 1	Note 1	V_{OUT} = 1V p-p		11			11		ns
	Gain 2	Note 2			6.0	12		6.0	10	
Propagation Delay	Gain 1	Note 1	V_{OUT} = 1V p-p		7.5			7.5		ns
	Gain 2	Note 2			6.0	10		6.0	10	
Input Resistance	Gain 1	Note 1			4.0			4.0		kΩ
	Gain 2	Note 2		10	30		20	30		
Input Capacitance	Gain 2	Note 2			2.0			2.0		pF
Input Offset Current					0.4	5.0		0.4	3.0	µA
Input Bias Current					9.0	30		9.0	20	µA
Input Noise Voltage			BW 1kHz to 10kHz		12			12		µV rms
Input Voltage Range						±1.0			±1.0	Volts
Common Mode Rejection Ratio	Gain 2		VCM ± 1V, F <100kHz	60	86		60	86		dB
	Gain 2		VCM ± 1V, F = 5MHz		60			60		
Supply Voltage Rejection Ratio	Gain 2		ΔVS = ±0.5V	50	80		50	80		dB
Output Offset Voltage	Gain 3		Note 3 R_L = ∞		0.2	0.75		0.2	0.75	Volts
Output Common Mode Voltage			R_L = ∞	2.4	2.9	3.4	2.4	2.9	3.4	Volts
Output Voltage Swing			R_L = 2kΩ, Single Ended	3.0	3.9		3.0	3.9		Volts
Output Resistance					20			20		Ω
Power Supply Current			R_L = ∞		16	24		16	24	mA

Recommended Operating Supply Voltage (V_S = ±6.0V)

Notes:
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

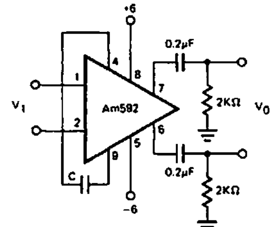
TYPICAL APPLICATIONS

DISC/TAPE PHASE MODULATED READBACK SYSTEMS



LIC-821

DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION

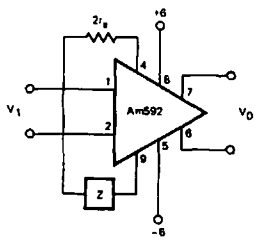


FOR FREQUENCY $F_1 < 1/2\,\pi\,(32)\,C$

$v_0 \geq 1.4 \times 10^4 C \frac{dvi}{dT}$

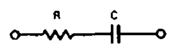
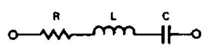
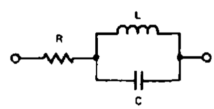
LIC-822

FILTER NETWORKS



$$\frac{v_0(s)}{v_1(s)} \geq \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

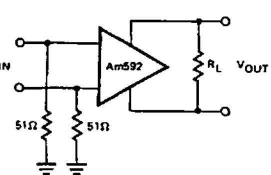
$$\geq \frac{1.4 \times 10^4}{Z(s) + 32}$$

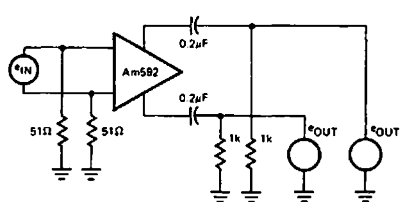
Z NETWORK	FILTER TYPE	$\frac{V_0\ (s)}{V_1\ (s)}$ TRANSFER FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/Ls + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

Note: In the networks above, the value used is assumed to include $2\,r_e$, or approximately 32 ohms.

LIC-823

TEST CIRCUITS
(T$_A$ = 25°C Unless Otherwise Noted)





LIC-824

LIC-825

Am733/733C

Differential Video Amplifier

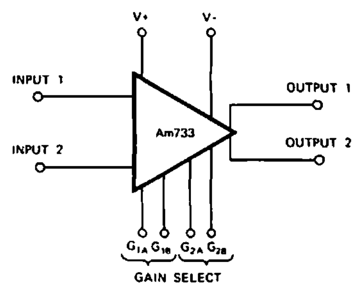
Distinctive Characteristics

- The Am733 and Am733C differential video amplifiers are functionally, electrically and pin-for-pin equivalent to the Fairchild μA733 and 733C.
- Bandwidths: 40 to 120 MHz
- Rise Times: 2.5 to 10 ns
- Propagation Delay: 3.6 to 10 ns
- 100% reliability assurance testing in compliance with MIL STD 883.
- Electrically tested and optically inspected dice for hybrid manufacturers.
- Available in metal can, hermetic dual-in-line or hermetic flat packages.

FUNCTIONAL DESCRIPTION

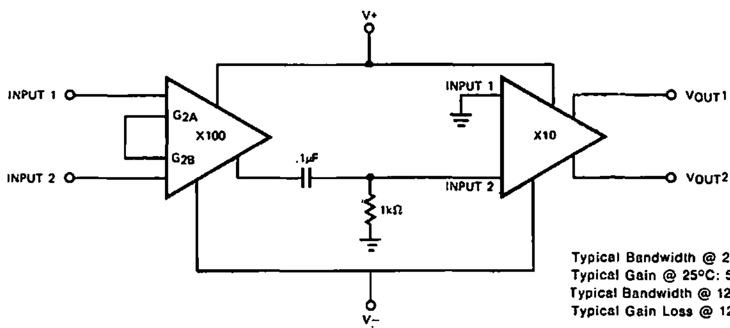
The Am733 is a monolithic two-stage differential input, emitter follower differential output video amplifier. Internal series-shunt feedback is used to obtain fixed gains of 10, 100 or 400, and adjustable gains from 10 to 400 by the use of an external resistor.

FUNCTIONAL DIAGRAM



LIC-826

TYPICAL APPLICATION
HIGH-GAIN WIDEBAND AMPLIFIER



Typical Bandwidth @ 25°C: 65 MHz
Typical Gain @ 25°C: 54 dB
Typical Bandwidth @ 125°C: 57 MHz
Typical Gain Loss @ 125°C: 1 dB

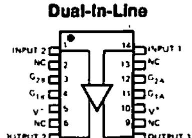
LIC-827

ORDERING INFORMATION

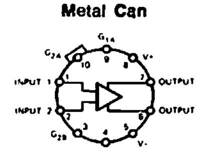
Part Number	Package Type	Temperature Range	Order Number
Am733C	TO-99	0°C to +70°C	733HC
	DIP	0°C to +70°C	733DC
	Dice	0°C to +70°C	733XC
Am733	TO-99	–55°C to +125°C	733HM
	DIP	–55°C to +125°C	733DM
	Flat Pak	–55°C to +125°C	733FM
	Dice	–55°C to +125°C	733XM

CONNECTION DIAGRAMS
Top Views

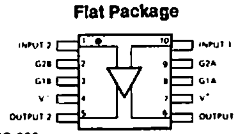
Dual-In-Line



Metal Can



Flat Package



LIC-828

NOTES:
(1) On Metal Can, pin 5 is connected to case.
(2) On DIP, pin 5 is connected to bottom of package.
(3) On Flat Package, pin 4 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage	±8 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	±6 V
Output Current	10 mA
Internal Power Dissipation (Note 1)	500 mW
Operating Temperature Range	
Am733C	0°C to +70°C
Am733	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_S = ±6.0$ V unless otherwise specified)

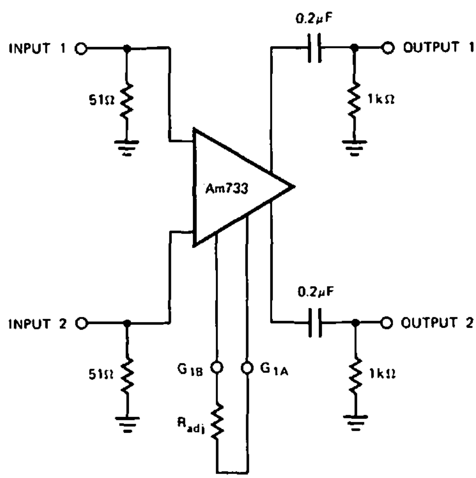
Parameter (see definitions)	Conditions	Am733C Min.	Am733C Typ.	Am733C Max.	Am733 Min.	Am733 Typ.	Am733 Max.	Units
Differential Voltage Gain								
Gain 1 (Note 2)		250	400	600	300	400	500	
Gain 2 (Note 3)		80	100	120	90	100	110	
Gain 3 (Note 4)		8.0	10	12	9.0	10	11	
Bandwidth	$R_S = 50\ \Omega$							
Gain 1			40			40		MHz
Gain 2			90			90		MHz
Gain 3			120			120		MHz
Risetime	$R_S = 50\ \Omega$, $V_{out} = 1$ Vpp							
Gain 1			10.5			10.5		ns
Gain 2			4.5	12		4.5	10	ns
Gain 3			2.5			2.5		ns
Propagation Delay	$R_S = 50\ \Omega$, $V_{out} = 1$ Vpp							
Gain 1			7.5			7.5		ns
Gain 2			6.0	10		6.0	10	ns
Gain 3			3.6			3.6		ns
Input Resistance								
Gain 1			4.0			4.0		kΩ
Gain 2		10	30		20	30		kΩ
Gain 3			250			250		kΩ
Input Capacitance	Gain 2		2.0			2.0		pF
Input Offset Current			0.4	5.0		0.4	3.0	μA
Input Bias Current			9.0	30		9.0	20	μA
Input Noise Voltage	$R_S = 50\ \Omega$, BW = 1 kHz to 10 MHz		12			12		μVrms
Input Voltage Range		±1.0			±1.0			V
Common Mode Rejection Ratio								
Gain 2	$V_{cm} = ±1$ V, f ≤ 100 kHz	60	86		60	86		dB
Gain 2	$V_{cm} = ±1$ V, f = 5 MHz		60			60		dB
Supply Voltage Rejection Ratio								
Gain 2	$\Delta V_S = ±0.5$ V	50	70		50	70		dB
Output Offset Voltage								
Gain 1			0.6	1.5		0.6	1.5	V
Gain 2 and Gain 3			0.35	1.5		0.35	1.0	V
Output Common Mode Voltage		2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing	Single Ended	3.0	4.0		3.0	4.0		Vpp
Output Sink Current		2.5	3.6		2.5	3.6		mA
Output Resistance			20			20		Ω
Power Supply Current			18	24		18	24	mA
The Following Specifications Apply Over The Operating Temperature Ranges								
Differential Voltage Gain								
Gain 1 (Note 2)		250	400	600	200	400	600	
Gain 2 (Note 3)		80	100	120	80	100	120	
Gain 3 (Note 4)		8.0	10	12	8.0	10	12	
Input Resistance								
Gain 1			4.0			4.0		kΩ
Gain 2		8.0	30		8.0	30		kΩ
Gain 3			250			250		kΩ
Input Offset Current			0.4	6.0		0.4	5.0	μA
Input Bias Current			9.0	40		9.0	40	μA
Input Voltage Range		±1.0			±1.0			V

7

Parameter (see definitions)	Conditions	Am733C Min.	Am733C Typ.	Am733C Max.	Am733 Min.	Am733 Typ.	Am733 Max.	Units
The Following Specifications Apply Over The Operating Temperature Ranges								
Common Mode Rejection Ratio Gain 2	$V_{cm} = \pm 1$ V, $f \leq 100$ kHz	50	86		50	86		dB
Supply Voltage Rejection Ratio Gain 2	$\Delta V_S = \pm 0.5$ V	50	70		50	70		dB
Output Offset Voltage Gain 1 Gain 2 and Gain 3			0.6 0.35	1.5 1.5		0.6 0.35	1.5 1.2	V V
Output Voltage Swing	Single Ended	2.8	4.0		2.5	4.0		Vpp
Output Sink Current		2.5	3.6		2.2	3.6		mA
Power Supply Current				27			27	mA

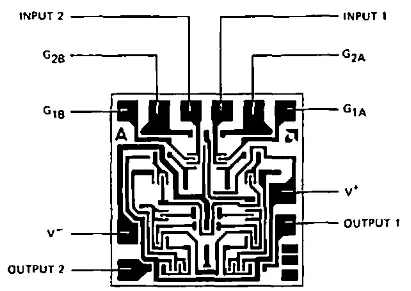
Notes: 1. Derate metal can package at 6.8 mW/°C for operation at ambient temperatures above 85°C and Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 100°C.
2. Gain Select pins G_{1A} and G_{1B} connected together.
3. Gain Select pins G_{2A} and G_{2B} connected together.
4. All Gain Select pins open.

VOLTAGE GAIN ADJUST CIRCUIT



LIC-829

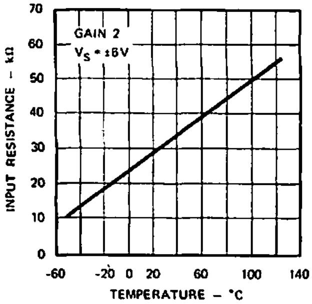
Metallization and Pad Layout



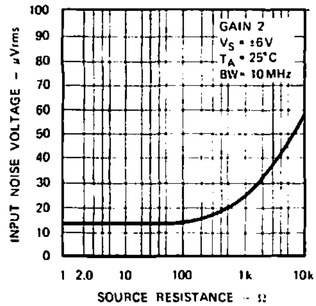
41 X 41 Mils

PERFORMANCE CURVES

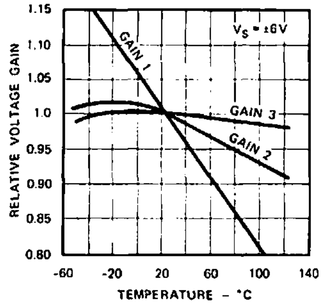
Input Resistance Vs. Temperature



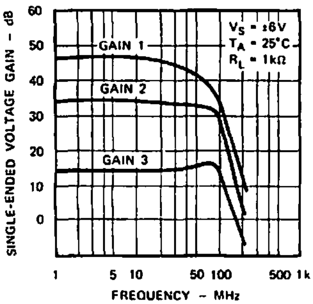
Input Noise Voltage



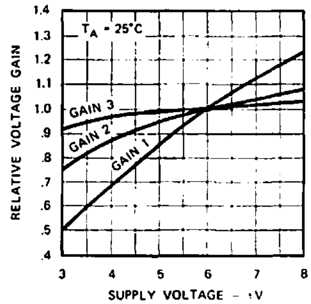
Gain Vs. Temperature



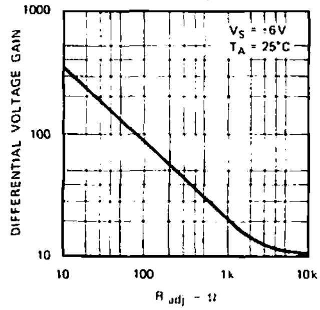
Gain Vs. Frequency



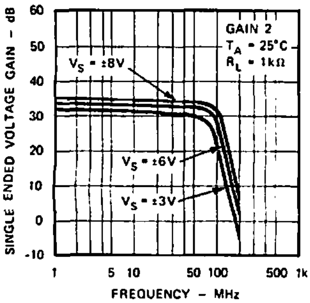
Gain Vs. Supply Voltage



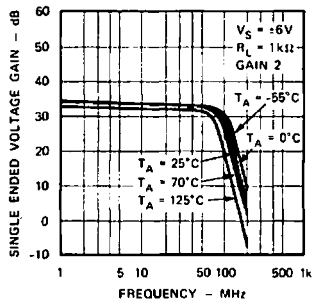
Gain Vs. R_{Adjust}



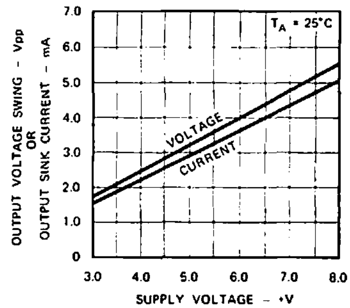
Gain Vs. Frequency and Supply Voltage



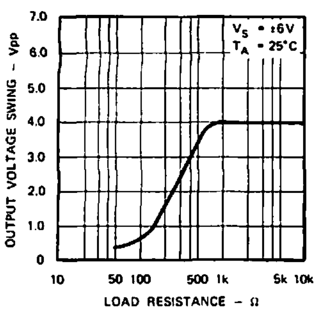
Gain Vs. Frequency and Temperature



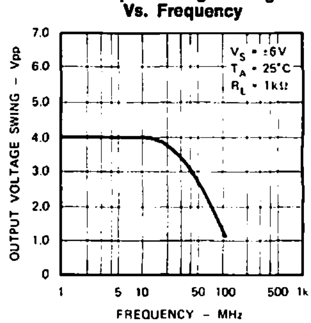
Output Voltage Swing And Sink Current Vs. Supply Voltage



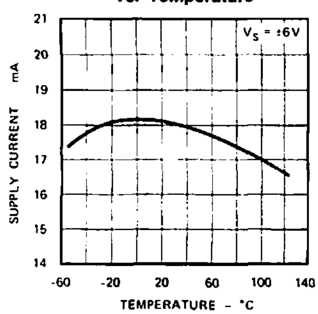
Output Voltage Swing Vs. Load Resistance



Output Voltage Swing Vs. Frequency



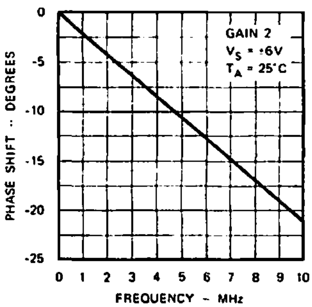
Supply Current Vs. Temperature



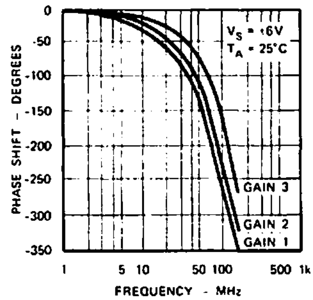
LIC-830

PERFORMANCE CURVES

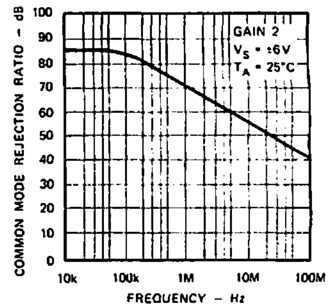
Phase Shift Vs. Frequency



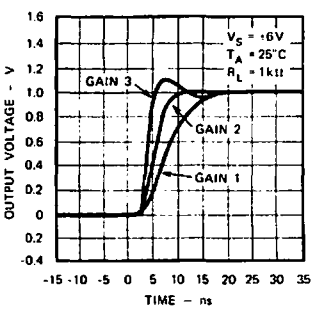
Phase Shift Vs. Frequency



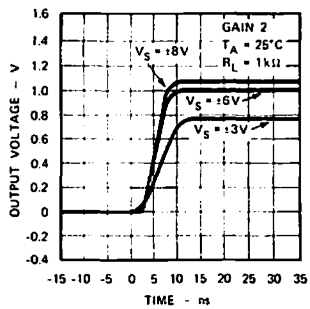
Common Mode Rejection Ratio



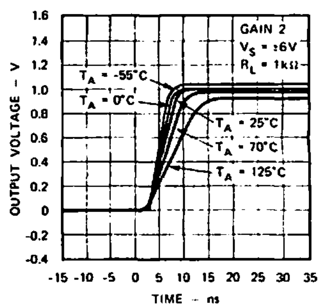
Pulse Response Vs. Gain



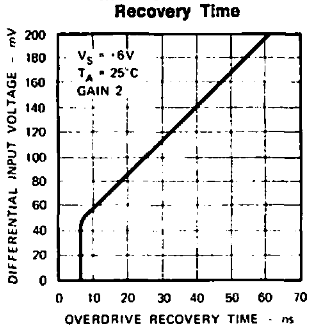
Pulse Response Vs. Supply Voltage



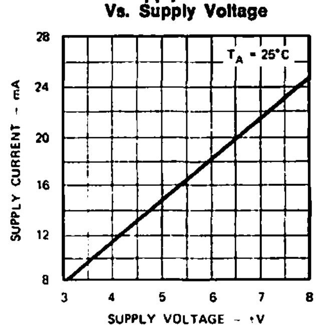
Pulse Response Vs. Temperature



Differential Overdrive Recovery Time



Supply Current Vs. Supply Voltage



LIC-831

Voltage Regulators – Section VIII

Am105/205/305/305A

Voltage Regulator

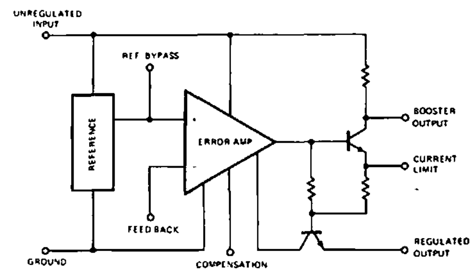
Distinctive Characteristics

- The Am105/205/305/305A are functionally, electrically, and pin-for-pin equivalent to the National LM 105/205/305/305A.
- Output voltage adjustable from 4.5V to 40V.
- Output currents in excess of 10A possible by adding external transistors.
- 100% reliability assurance testing in compliance with MIL STD 883.
- Electrically tested and optically inspected die for assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am105/205/305/305A is a positive voltage regulator which can be used in the series, shunt, linear or switching modes of operation. The circuits feature low stand-by current drain, operation under minimum load conditions and an output current capability of up to 20 mA.

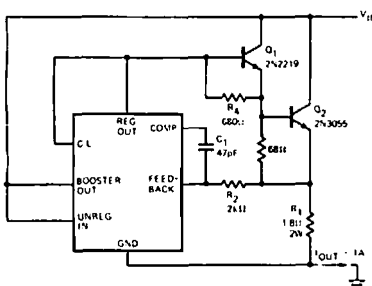
FUNCTIONAL DIAGRAM



LIC-632

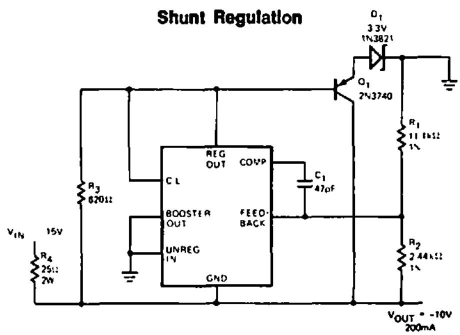
TYPICAL APPLICATIONS

Current Regulator



LIC-833

Shunt Regulation



LIC-834

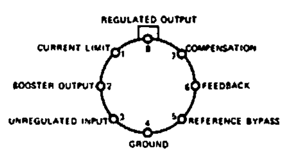
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am305A	TO-99	0°C to +70°C	LM305AH
Am305	TO-99 Dice	0°C to +70°C 0°C to +70°C	LM305H LD305
Am205	TO-99	–25°C to +85°C	LM205H
Am105	TO-99 Dice	–55°C to +125°C –55°C to +125°C	LM105H LD105

CONNECTION DIAGRAM

Top View

Metal Can



NOTES: (1) On Metal Can, pin 4 is connected to case.

LIC-835

8

MAXIMUM RATINGS

Input Voltage Range	Am105/205/305A Am305	50 V 40 V
Input-Output Voltage Differential		40 V
Internal Power Dissipation (Note 1) Metal Can (Similar to TO-99)		 500 mW 800 mW
Operating Temperature Range Am105 Am205 Am305/305A		 −55°C to +125°C −25°C to +85°C 0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)		300°C

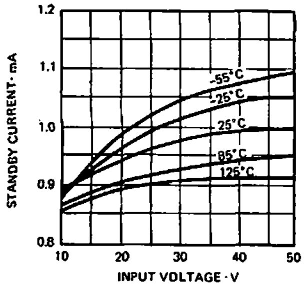
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 2)

Parameter (see definitions)	Conditions	Am305 Min	Am305 Typ	Am305 Max	Am305A Min	Am305A Typ	Am305A Max	Am105 Am205 Min	Am105 Am205 Typ	Am105 Am205 Max	Units
Input Voltage Range		8.5		40	8.5		50	8.5		50	V
Output Voltage Range		4.5		30	4.5		40	4.5		40	V
Input-Output Voltage Differential		3.0		30	3.0		30	3.0		30	V
Line Regulation (Note 3)	$V_{in} - V_{out} \leq 5$ V		0.025	0.06		0.025	0.06		0.025	0.06	%/V
	$V_{in} - V_{out} \geq 5$ V		0.015	0.03		0.015	0.03		0.015	0.03	%/V
Load Regulation (Note 3)	$0 \leq I_O \leq 12$ mA										
	$R_{SC} = 18\,\Omega$, $T_A = 25°C$		0.02	0.05					0.02	0.05	%
	$R_{SC} = 15\,\Omega$, $T_A = T_A(max)$		0.03	0.1							%
	$R_{SC} = 10\,\Omega$, $T_A = T_A(max)$								0.03	0.1	%
	$R_{SC} = 18\,\Omega$, $T_A = T_A(min)$		0.03	0.1					0.03	0.1	%
	$0 \leq I_O \leq 45$ mA										
	$R_{SC} = 0\,\Omega$, $T_A = 25°C$					0.02	0.2				%
	$R_{SC} = 0\,\Omega$, $T_A = T_A$ (max)					0.03	0.4				%
	$R_{SC} = 0\,\Omega$, $T_A = T_A$ (min)					0.03	0.4				%
Feedback Sense Voltage		1.63	1.70	1.81	1.55	1.70	1.85	1.63	1.70	1.81	V
Ripple Rejection	$C_{REF} = 10\,\mu f$, f = 120 Hz		0.003	0.01		0.003			0.003	0.01	%/V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz										
	$C_{REF} = 0$		0.005			0.005			0.005		%
	$C_{REF} > 0.1\,\mu f$		0.002			0.002			0.002		%
Standby Current Drain	$V_{in} = 40$ V		0.8	2.0							
	$V_{in} = 50$ V					0.8	2.0		0.8	2.0	mA
Long Term Stability			0.1	1.0		0.1	1.0		0.1	1.0	%
Temperature Stability			0.3	1.0		0.3	1.0		0.3	1.0	%
Current Limit Sense Voltage (Note 4)	$R_{SC} = 10\,\Omega$, $T_A = 25°C$ $V_{out} = 0$ V	225	300	375	225	300	375	225	300	375	mV

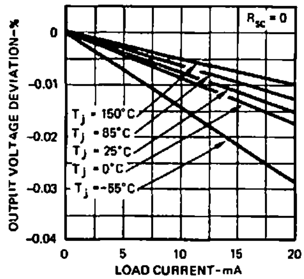
Notes: 1. Derate Metal Can package at 6.8mW/°C for operation at ambient temperatures above 25°C.
2. These specifications apply over the operating temperature range, for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of 2kΩ, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.
3. The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.
4. With no external pass transistor.
5. Connect booster output to unregulated input when no external pass transistor is used.

PERFORMANCE CURVES

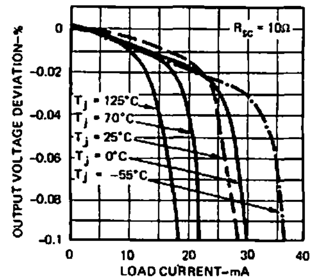
Standby Current Drain As A Function Of Input Voltage



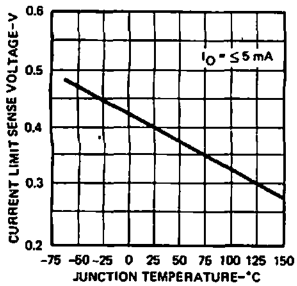
Load Regulation



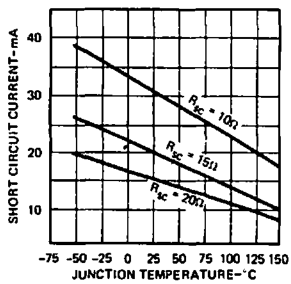
Load Regulation Characteristics With Current Limiting



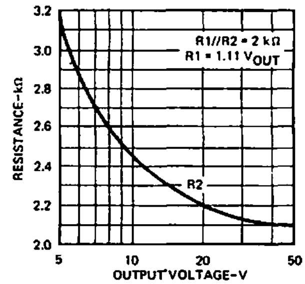
Current Limiting Sense Voltage As A Function of Junction Temperature



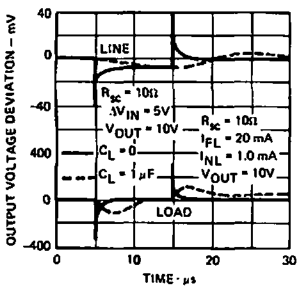
Short Circuit Current



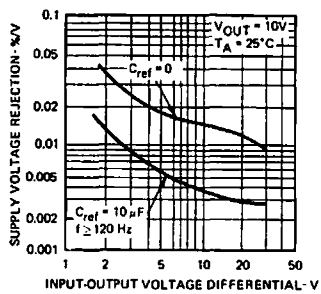
Optimum Divider Resistance Values



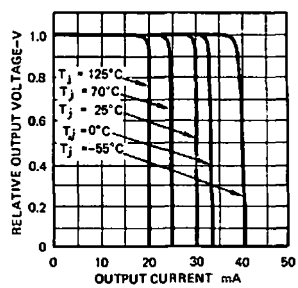
Transient Response



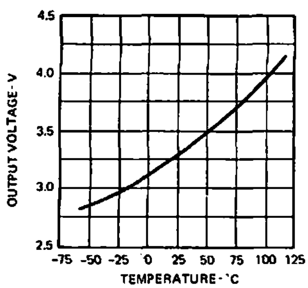
Supply Voltage Rejection



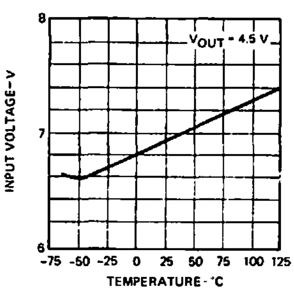
Current Limiting Characteristics



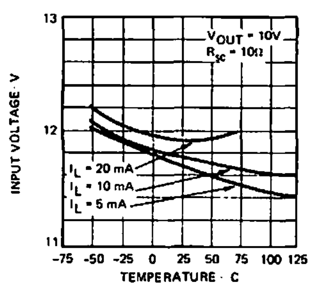
Minimum Output Voltage



Minimum Input Voltage



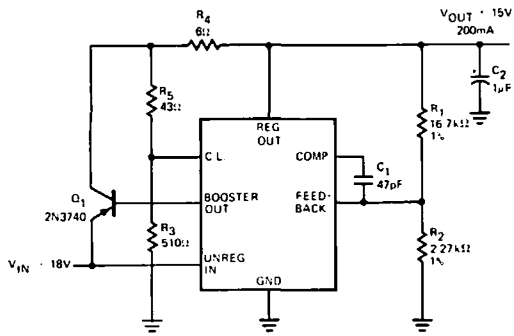
Regulator Dropout Voltage



LIC-836

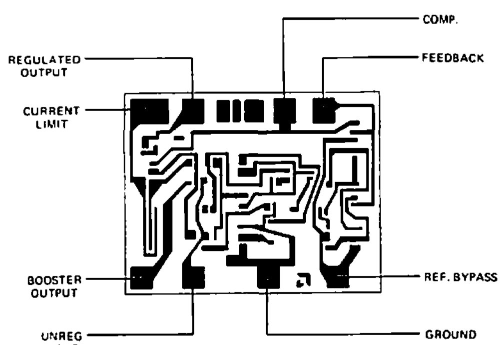
ADDITIONAL APPLICATIONS

Linear Regulator with Foldback Current Limiting



LIC-837

Metallization and Pad Layout



38 x 48 Mils

Am723/723C

Voltage Regulator

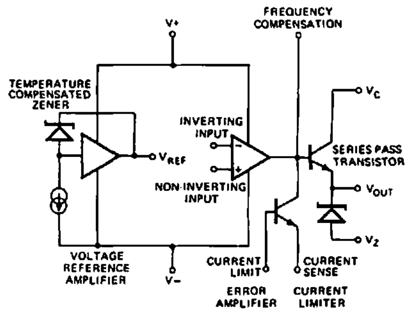
Description: The Am723 and Am723C monolithic voltage *regulators* are functionally and electrically equivalent to the Fairchild μA723 and μA723C. Both are available in the hermetic dual-in-line and metal can packages and are pin for pin replacements for the Fairchild μA723 and μA723C.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL-STD-883.
Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am723 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. It is applicable to remote shutdown and current limiting operations and will accept either PNP or NPN external pass elements to increase output current capability.

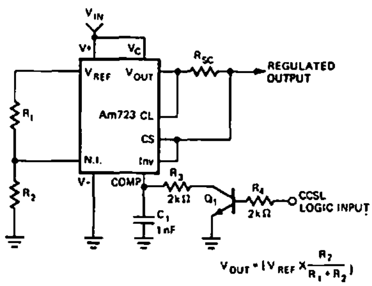
FUNCTIONAL DIAGRAM



LIC-838

APPLICATIONS

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING (V_{out} = 2 to 7 Volts)



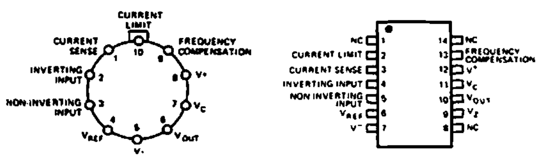
LIC-839

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am723C	DIP	0°C to +70°C	723DC
	Metal Can	0°C to +70°C	723HC
	Molded DIP	0°C to +70°C	723PC
	Dice	0°C to +70°C	723XC
Am723	DIP	−55°C to +125°C	723DM
	Metal Can	−55°C to +125°C	723HM
	Dice	−55°C to +125°C	723XM

CONNECTION DIAGRAMS
Top Views

Metal Can **Dual-In-Line**



NOTES: (1) On Metal Can, pin 5 is connected to case.
(2) On DIP, pin 7 is connected to case.

LIC-840

MAXIMUM RATINGS

Pulse Voltage from V^+ to V^- (50 msec)	50 V
Continuous Voltage from V^+ to V^-	40 V
Input-Output Voltage Differential	40 V
Maximum Output Current	150 mA
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation (Note 1)	
Metal Can	850 mW
DIP	900 mW
Operating Temperature Range	
Am723C	0°C to +70°C
Am723	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

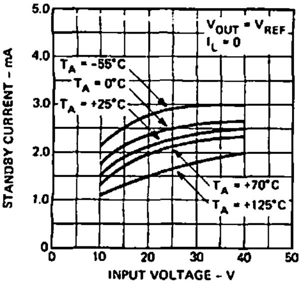
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 2)

Parameter (see definitions)	Conditions	Am723C Min	Am723C Typ	Am723C Max	Am723 Min	Am723 Typ	Am723 Max	Units
Line Regulation (Note 3)	V_{IN} = 12 V to V_{IN} = 15 V		0.01	0.1		0.01	0.1	% V_{OUT}
	V_{IN} = 12 V to V_{IN} = 40 V		0.1	0.5		0.02	0.2	% V_{OUT}
Load Regulation (Note 3)	I_L = 1 mA to I_L = 50 mA		0.03	0.2		0.03	0.15	% V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74			74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF		86			86		dB
Short Circuit Current Limit	R_{SC} = 10 Ω, V_{OUT} = 0		65			65		mA
Reference Voltage		6.80	7.15	7.50	6.95	7.15	7.35	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20			20		μV_{rms}
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF		2.5			2.5		μV_{rms}
Long Term Stability			0.1			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 30 V		2.3	4.0		2.3	3.5	mA
Input Voltage Range		9.5		40	9.5		40	V
Output Voltage Range		2.0		37	2.0		37	V
Input-Output Voltage Differential		3.0		38	3.0		38	V
The Following Specifications Apply Over The Operating Temperature Ranges								
Line Regulation	V_{IN} = 12 V to V_{IN} = 15 V			0.3			0.3	% V_{OUT}
Load Regulation	I_L = 1 mA to I_L = 50 mA			0.6			0.6	% V_{OUT}
Average Temperature Coefficient of Output Voltage			0.003	0.015		0.002	0.015	%/°C

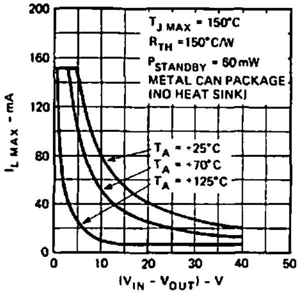
Notes: 1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 25°C and Dual-In-Line package at 9 mW/°C for operation at ambient temperatures above 50°C.
2. Unless otherwise specified, T_A = 25°C, V_{IN} = V+ = V_C = 12 V, V− = 0 V, V_{out} = 5 V, I_L = 1 mA, R_{SC} = 0, C_1 = 100 pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤10 kΩ when connected as shown in Fig. 3.
3. The load & line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

PERFORMANCE CURVES

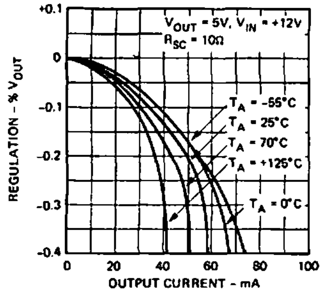
Standby Current Drain As A Function Of Input Voltage



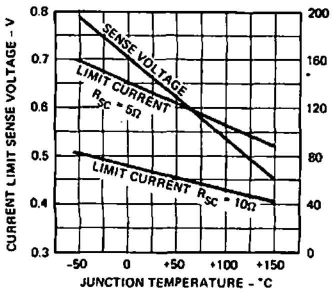
Maximum Load Current As A Function Of Input-Output Voltage Differential



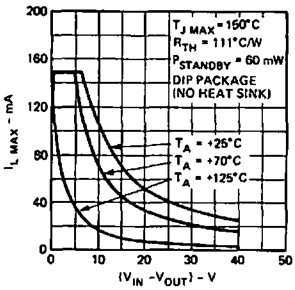
Load Regulation Characteristics With Current Limiting



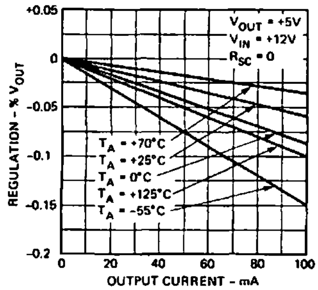
Current Limiting Characteristics As A Function of Junction Temperature



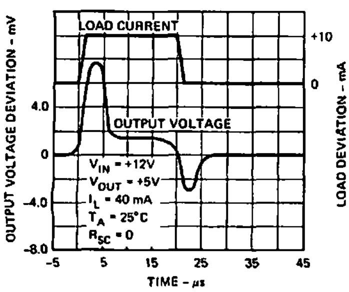
Maximum Load Current As A Function Of Input-Output Voltage Differential



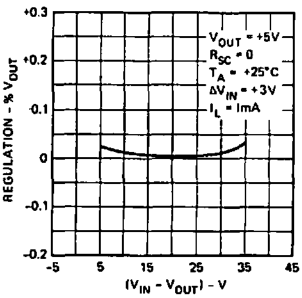
Load Regulation Characteristics Without Current Limiting



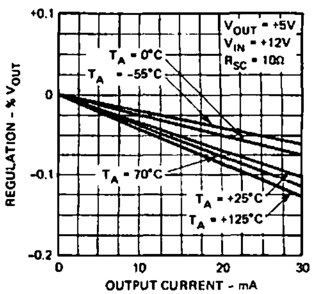
Load Transient Response



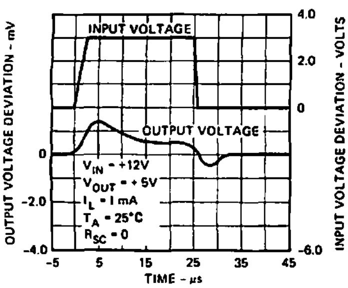
Line Regulation As A Function Of Input-Output Voltage Differential



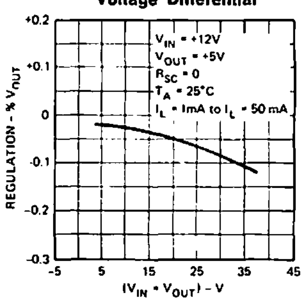
Load Regulation Characteristics With Current Limiting



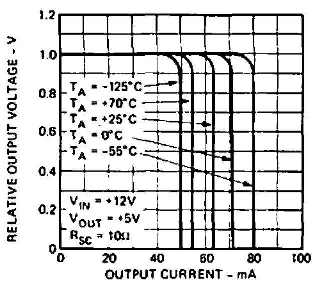
Line Transient Response



Load Regulation As A Function Of Input-Output Voltage Differential



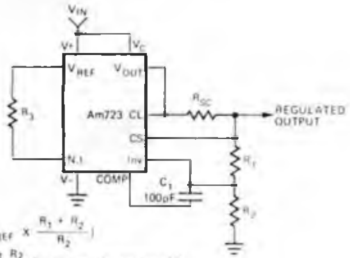
Current Limiting Characteristics



LIC-841

APPLICATIONS

HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)



$V_{OUT} = (V_{REF} \times \frac{R_1 + R_2}{R_2})$

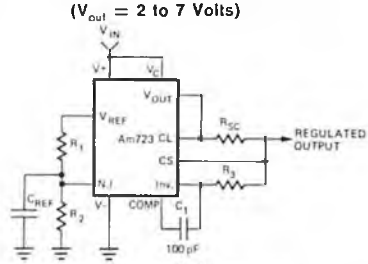
$R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift

R_3 may be eliminated for minimum component count

LIC-842

Figure 1

LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)

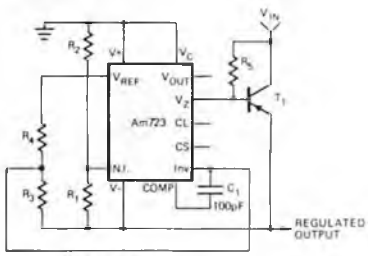


$V_{OUT} = (V_{REF} \times \frac{R_2}{R_1 + R_2})$; $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift

Figure 3

LIC-844

NEGATIVE VOLTAGE REGULATOR

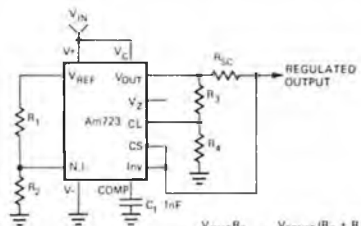


$V_{OUT} = (\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1})$; $R_3 = R_4$

LIC-843

Figure 2

FOLDBACK CURRENT LIMITING REGULATOR



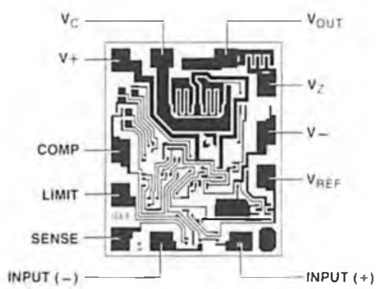
$I_{KNEE} = (\frac{V_{OUT} R_3}{R_{SC} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{SC} R_4})$

$V_{OUT} = (V_{REF} \times \frac{R_2}{R_1 + R_2})$; $I_{SHORT\ CKT} = (\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4})$

Figure 4

LIC-845

Metallization and Pad Layout



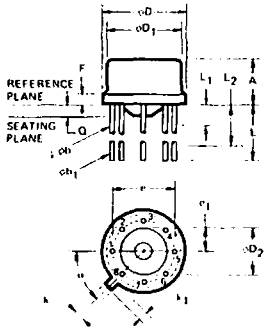
45 x 53 Mils

Section IX

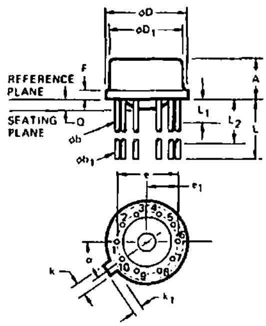
PACKAGE OUTLINES

METAL CAN PACKAGES

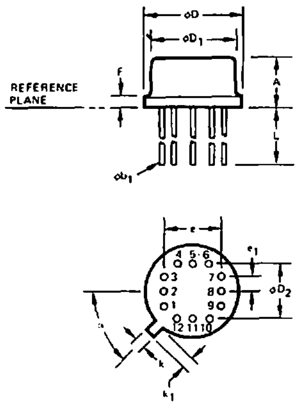
H-8-1



H-10-1



G-12-1

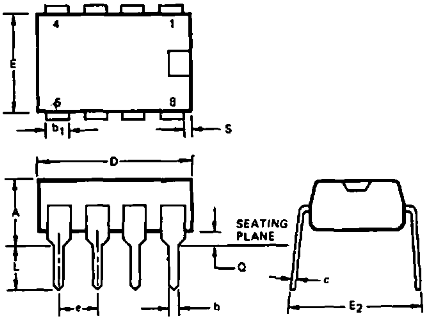


Parameters	H-8-1		H-10-1		G-12-1	
	Min.	Max.	Min.	Max.	Min.	Max.
A	.165	.185	.165	.185	.155	.180
e	.185	.215	.215	.245	.390	.410
e_1	.090	.110	.105	.125	.090	.110
F	.013	.033	.013	.033	.020	.030
k	.027	.034	.027	.034	.024	.034
k_1	.027	.045	.027	.045	.024	.038
L	.500	.570	.500	.610	.500	.600
L_1		.050		.050		
L_2	.250		.250			
α	45° BSC		36° BSC		45°	
ϕb	.016	.019	.016	.019		
ϕb_1	.016	.021	.016	.021	.016	.021
ϕD	.350	.370	.350	.370	.590	.610
ϕD_1	.305	.335	.305	.335	.540	.560
ϕD_2	.120	.160	.120	.160	.390	.410
Q	.015	.045	.015	.045		

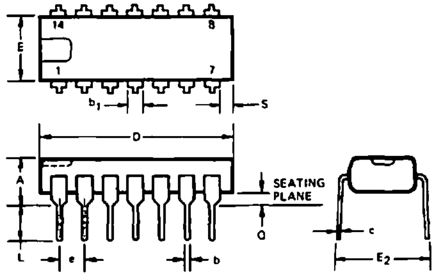
Notes: 1. Standard lead finish is bright acid tin plate or gold plate.
2. ϕb applies between L_1 and L_2. ϕb_1 applies between L_1 and 0.500" beyond reference plane.

PACKAGE OUTLINES (Cont.)

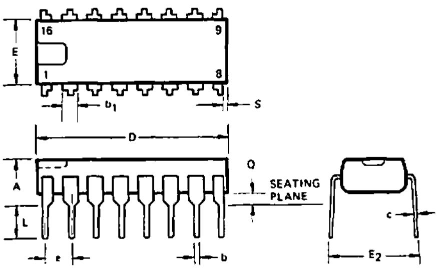
P-8-1
8-LEAD MOLDED DUAL-IN-LINE



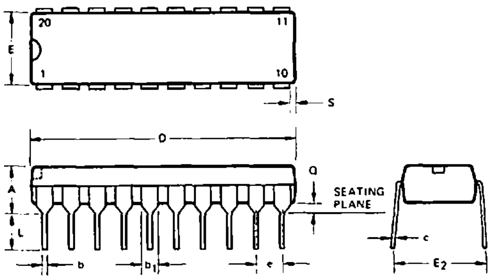
P-14-1
14-LEAD MOLDED DUAL-IN-LINE
(TO-116)



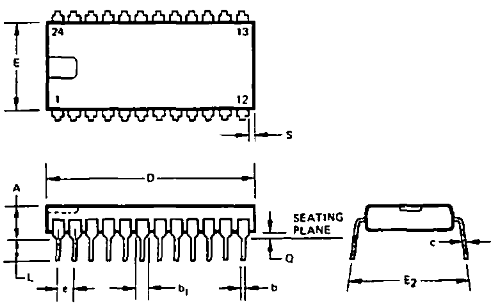
P-16-1
16-LEAD MOLDED DUAL-IN-LINE



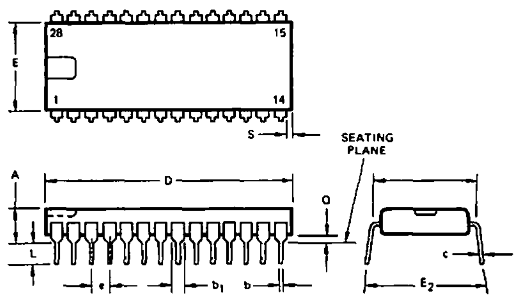
P-20-1
20-LEAD MOLDED DUAL-IN-LINE



P-24-1
24-LEAD MOLDED DUAL-IN-LINE



P-28-1
28-LEAD MOLDED DUAL-IN-LINE

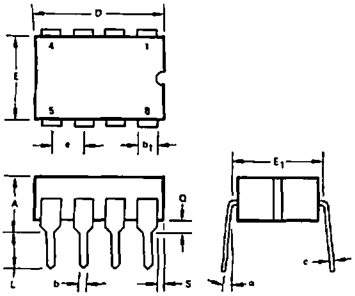


DIMENSIONS (inches)

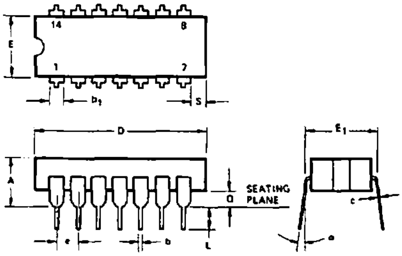
Parameters	P-8-1		P-14-1		P-16-1		P-20-1		P-24-1		P-28-1	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.150	.200	.150	.200	.150	.200	.150	.200	.170	.215	.150	.200
b	.015	.022	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020
b_1	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065
c	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011
D	.375	.395	.745	.775	.745	.775	1.010	1.050	1.240	1.270	1.450	1.480
E	.240	.260	.240	.260	.240	.260	.250	.290	.515	.540	.530	.550
E_2	.310	.385	.310	.385	.310	.385	.310	.385	.585	.700	.585	.700
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.150	.125	.150	.125	.150	.125	.160	.125	.160
Q	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060
S_1	.010	.030	.040	.065	.010	.040	.025	.055	.035	.065	.040	.070

PACKAGE OUTLINES (Cont.)

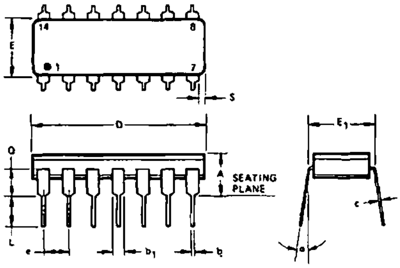
D-8-1
8-LEAD HERMETIC DUAL-IN-LINE



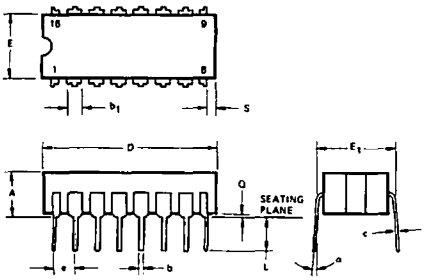
D-14-1
14-LEAD HERMETIC DUAL-IN-LINE



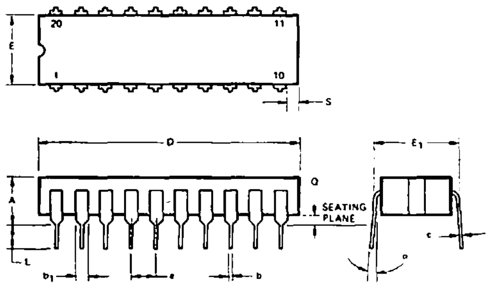
†D-14-3
14-LEAD METAL HERMETIC DUAL-IN-LINE



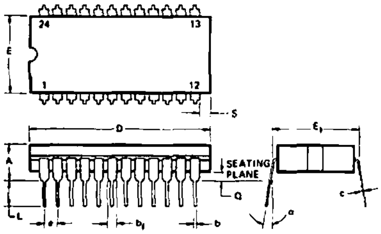
D-16-1
16-LEAD HERMETIC DUAL-IN-LINE



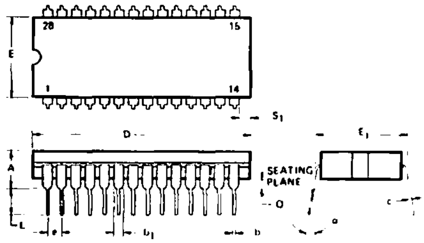
D-20-1
20-LEAD HERMETIC DUAL-IN-LINE



D-24-1
24-LEAD HERMETIC DUAL-IN-LINE



D-28-1
28-LEAD HERMETIC DUAL-IN-LINE



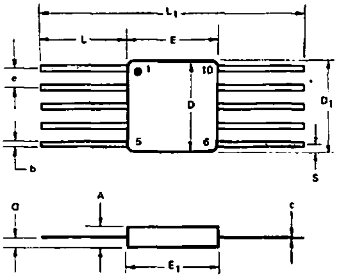
DIMENSIONS (Inches)

Parameters	D-8-1		D-14-1		D-14-3 (Note 2)		D-16-1		D-20-1		D-24-1		D-28-1	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.130	.200	.130	.200	.100	.200	.130	.200	.140	.220	.150	.225	.150	.225
b	.016	.020	.016	.020	.015	.023	.016	.020	.016	.020	.016	.020	.016	.020
b_1	.050	.070	.050	.070	.030	.070	.050	.070	.050	.070	.045	.065	.045	.065
c	.009	.011	.009	.011	.008	.011	.009	.011	.009	.011	.009	.011	.009	.012
D	.370	.400	.745	.785	.660	.785	.745	.785	.935	.970	1.230	1.285	1.440	1.490
E	.240	.285	.240	.285	.230	.265	.240	.310	.245	.285	.510	.545	.510	.545
E_1	.300	.320	.290	.320	.290	.310	.290	.320	.290	.320	.600	.620	.600	.620
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.150	.100	.150	.125	.150	.125	.150	.120	.150	.125	.150
Q	.015	.060	.015	.060	.020	.080	.015	.060	.015	.060	.015	.060	.015	.060
S_1	.004		.010		.020		.005		.005		.010		.010	
α	3°	13°	3°	13°	3°	13°	3°	13°	3°	13°	3°	13°	3°	13°

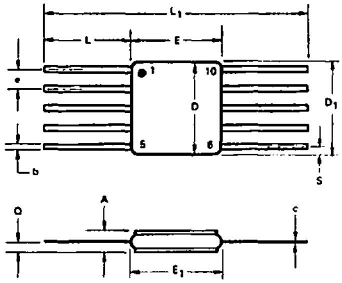
9

PACKAGE OUTLINES (Cont.)

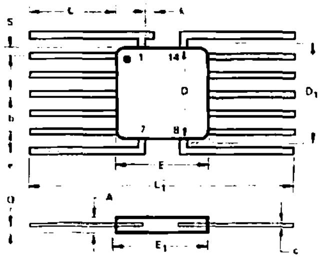
F-10-1
10-LEAD CERPAK



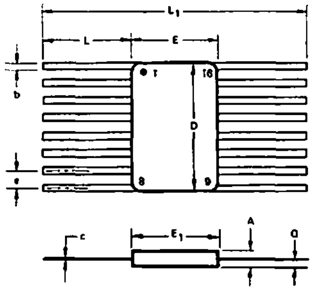
†F-10-2
10-LEAD FLAT PACKAGE



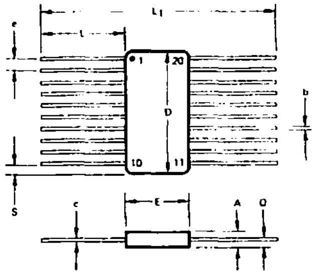
F-14-1
14-LEAD CERPAK



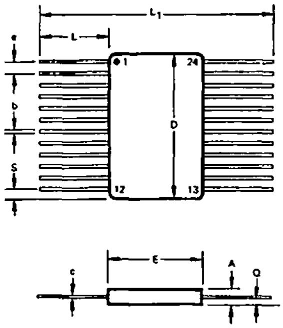
F-16-1
16-LEAD CERPAK



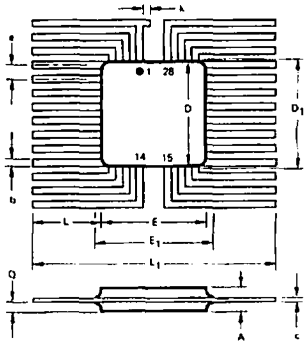
F-20-1
20-LEAD CERPAK



F-24-1
24-LEAD CERPAK



F-28-2
28-LEAD FLAT PACKAGE



DIMENSIONS (inches)

Parameters	F-10-1		F-10-2		F-14-1		F-16-1		F-20-1		F-24-1		F-28-1	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.045	.080	.045	.080	.045	.080	.045	.085	.045	.085	.050	.090	.045	.080
b	.015	.019	.012	.019	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
c	.004	.006	.003	.006	.004	.006	.004	.006	.004	.006	.004	.006	.003	.006
D	.230	.255	.235	.275	.230	.255	.370	.425	.490	.520	.580	.620	.360	.410
D_1				.275										.410
E	.240	.260	.240	.260	.240	.260	.245	.285	.245	.285	.360	.385	.360	.410
E_1		.275		.280		.275		.290		.290		.410		.410
e	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055
L	.300	.370	.300	.370	.300	.370	.300	.370	.300	.370	.265	.320	.270	.320
L_1	.920	.980	.920	.980	.920	.980	.920	.980	.920	.980	.920	.980	.955	1.000
Q	.010	.040	.010	.040	.010	.040	.020	.040	.020	.040	.020	.040	.010	.040
S_1	.005		.005		.005		.005		.005		.005		0	

GLOSSARY

$\Delta I_{OS}/\Delta T_A$ — **Average Temperature Coefficient of Input Offset Current** – The ratio of the change in input offset current, over the operating temperature range, to the operating temperature range. (pA/°C)

$\Delta V_{OS}/\Delta T_A$ — **Average Temperature Coefficient of Input Offset Voltage** – The ratio of the change in input offset voltage, over the operating temperature range, to the operating temperature range. (μV/°C)

BW — **Bandwidth** – The frequency at which the gain of the device is 3 dB below its low frequency value.

CS — **Channel Separation** – The log of the ratio of the input of an undriven amplifier to the output of an adjacent driven amplifier. (dB)

V_{OHC} — **Clamped Output High Voltage** – The voltage potential necessary to turn on (forward bias) the clamping diode on the output pin. (V)

V_{OLC} — **Clamped Output Low Voltage** – The voltage potential necessary to turn off (reverse bias) the clamping diode on the output pin. (V)

f_{clock} — **Clock Frequency** – The reciprocal of the clock period; the clock repetition rate.

Clock Input, Amplitude – The peak amplitude of the clock signal.

t_{PW} — **Clock Input, Width** – The time duration of the clock pulse.

Common Mode Gain – The ratio of the output voltage change to the input common mode voltage producing that change.

Common Mode Input Overload Recovery Time – The time delay between removal of an input common mode voltage outside the input common mode range, and resumption of normal device operation. (ns)

Common Mode Input Resistance – The value of resistance with respect to a common mode signal, seen when looking into both inputs. (Ω)

Common Mode Input Voltage Swing – The peak value of the common mode input voltage at which the device will operate in a linear fashion. (V)

Common Mode Output Voltage – The output voltage resulting from the application of a voltage common to both inputs and the average of the two output voltages of a differential output amplifier. (V)

CMRR — **Common Mode Rejection Ratio** – The ratio of the change in input offset voltage to the total change in common mode voltage producing it. (dB)

V_{CM} — **Common Mode Voltage** – The arithmetic mean of the voltage present at the differential inputs with respect to the device ground reference. (V)

t_d — **Delay Time** – See Propagation Delay. (ns)

Differential Input Bias Current – The current required in the differential input stage to bias the stage into operation.

Differential Input Capacitance – The effective capacitance between the two inputs, operating open loop.

Differential Input Impedance – The impedance seen looking between the input terminals.

Differential Input Offset Current – The difference in currents required by the transistors in the input stage to bias the input stage to its quiescent operation point.

Differential Input Overload Recovery Time – The time delay between removal of a differential input voltage that exceeds the differential input voltage operating range, and resumption of normal device operation.

Differential Input Resistance – The effective resistance between the two inputs, operating open loop.

Differential Input Threshold Voltage – The voltage difference between the + and – inputs required to guarantee the output logic state.

Differential Input Voltage Range – The range of voltage applied between the input terminals for which operation remains within specifications.

Differential Load Rejection – The ratio of the change in input offset voltage to the change in differential load current.

Differential Output Resistance – The resistance measured between the two output terminals.

Differential Output Voltage Swing – The peak differential output voltage that can be obtained without clipping the output voltage waveform.

Differential Voltage Gain – The ratio of the change in differential output voltage to the change in differential input voltage.

V_{DO} — **Dropout Voltage** – The input-output voltage differential that causes the output voltage to decrease by 5% of its initial value. (V)

9

GLOSSARY (Cont.)

t_{ZH}	**Enable HIGH** – The delay time from a control input change to the three-state output high-impedance to HIGH-level transition.
t_{ZL}	**Enable LOW** – The delay time from a control input change to the three-state output high-impedance to LOW-level transition.
i_n	**Equivalent Input Noise Current** – The input noise current that would reproduce the noise seen at the output if all amplifier noise sources were set to zero and the source impedances were large compared to the optimum source impedance. ($pA/\sqrt{Hz}$)
e_n	**Equivalent Input Noise Voltage** – The input noise voltage that would reproduce the noise seen at the output if all amplifier noise sources and the source resistances were set to zero. ($nV/\sqrt{Hz}$)
t_f	**Fall Time** – The time required for the signal to fall from 90% to 10% of its output value into a specified load network. (ns)
	Feedback Capacitance – The effective value of the capacitive coupling from output to input.
V_{sense}	**Feedback Sense Voltage** – The voltage measured on the feedback terminal of the regulator, with respect to ground, when the device is operating in regulation. (V)
	Frequency Response – The frequency at which the output drops to 0.707 of its low frequency value.
f_t	**Gain Bandwidth Product** – The frequency at which the small signal ac gain of the device reduces to unity. (MHz)
H	**HIGH** – Applying to a HIGH voltage level.
h_{fe}	**High Frequency Current Gain** – The small signal ac current gain at a specified frequency.
t_{HZ}	**HIGH to Disable** – The delay time from a control input change to the three-state output HIGH-level to high-impedance transition (measured at 0.5V change).
t_h	**Hold Time** – The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.
ΔV_{TH}	**Hysteresis** – The voltage difference between the switching points of the device. See Lower Input Threshold Voltage and Upper Input Threshold Voltage.
I	**Input.**
I_{BIAS}	**Input Bias Current** – The average of the two input currents with no signal applied. (nA or pA)
	Input Bias Current Drift – The change in input bias current with temperature supply voltage, or time. ($\Delta I_{BIAS}/\Delta T, \Delta V_S, \Delta t$)
C_{IN}	**Input Capacitance** – The equivalent capacitance of either input with the other input grounded. (pF)
V_{IH}	**Input HIGH Voltage** – The range of input voltages that represents a logic HIGH in the system.
V_C	**Input Clamp Diode Voltage** – The most negative voltage at an input when 18 mA is forced out of that input terminal. This parameter guarantees the integrity of the input diode which is intended to clamp negative ringing at the input terminal.
CMVR	**Input Common Mode Voltage Range** – The range of common mode input voltage over which the device will operate within specifications. (V)
I_{IN}	**Input Current** – The current flowing into the input with a specified voltage applied to the input.
	Input Current at Maximum Input Voltage – The current into a TTL or DTL input with the absolute maximum allowed input voltage applied to the input.
I_F	**Input Forward Current** – See Input LOW Current.
I_{IH}	**Input HIGH Current** – The current flowing out of an input when a specified LOW voltage is applied.
V_{IH}	**Input HIGH Voltage** – The range of input voltages that represents a logic HIGH in the system.
	Input Latch Voltage – See Input Clamp Diode Voltage.
I_{IL}	**Input LOW Current** – The current flowing out of an input when a specified LOW voltage is applied.
V_{IL}	**Input LOW Voltage** – The range of input voltages that represents a logic LOW in the system.
	Input Noise Voltage – The rms noise voltage present at the amplifier output divided by the gain of the amplifier, measured with the inputs connected to ground through a low resistance. (e_n)
I_{OS}	**Input Offset Current** – The difference in current into the two input terminals with the output voltage at zero. In a comparator, it is the difference between the two input currents with the output at the logic threshold voltage. Also, it is defined as the difference in input currents required to give equal output currents from a matched pair of devices. (nA or pA)
$\Delta I_{OS}/\Delta T$ $\Delta V, \Delta t$	**Input Offset Current Drift** – The change in input offset current produced with time, voltage or temperature. $\Delta V, \Delta t$ ($pA/^\circ C$, V, s)
V_{OS}	**Input Offset Voltage** – The voltage applied between the input terminals to obtain zero output voltage. In Compar-

GLOSSARY (Cont.)

ators, it is the voltage applied to the input terminals to give the logic threshold voltage at the output. It is also defined as the input voltage differential required to give equal output currents from a matched pair of devices. (mV)

$\Delta V_{OS}/\Delta T$, ΔV, Δt	**Input Offset Voltage Drift** — The change in input offset voltage with time, voltage or temperature. ($\mu V/°C$, V, s)
	Input-Output Voltage Differential — The voltage range between the unregulated input voltage and the regulated output voltage in which a regulator operates within specifications.
R_{IN}	**Input Resistance** — The equivalent resistance seen looking into either input terminal with the other terminal grounded. (MΩ)
I_R	**Input Reverse Current** — See Input HIGH Current. (μA)
	Input to Output Delay — See Propagation Delay.
V_{IN}	**Input Voltage** — The voltage potential between the input terminal and the device ground reference. (V)
$V_{IN(MIN)}$	**Input Voltage (Min)** — The minimum voltage required to bias the reference to specification limits. (V)
V_{IN}	**Input Voltage Range** — The range of voltage on an input terminal over which the device operates as specified. (V)
	Large Signal Voltage Gain — The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.
$\Delta V_{OUT}/\Delta V_{IN}$	**Line Regulation** — The change in output voltage for a specified change in input voltage. (mV or %)
	Linearity — The deviation of the characteristic from a straight line.
$\Delta V_{OUT}/\Delta I_L$	**Load Regulation** — The change in output voltage for a specified change in load current. (mV or %)
L	**LOW** — Applying to a LOW voltage level.
t_{LZ}	**LOW to Disable** — The delay time from a control input change to the three-state output LOW-level to high-impedance transition (measured at 0.5V change).
V_{ILMAX}	**Maximum input LOW voltage** — The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.
V_{IHMIN}	**Minimum input HIGH Voltage** — The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.
V_{T-}	**Negative-going Threshold Voltage** — The input voltage of a variable threshold device that is interpreted as a V_{IL} as the input transition falls from above $V_{T+(MAX)}$
	Negative Current — Current flowing out of the device.
NF	**Noise Figure** — The ratio of the input signal-to-noise ratio to the output signal-to-noise ratio. Usually expressed as common log. (dB)
	1/F Noise — The noise measured at a specified low frequency below the frequency range where the device noise spectrum is essentially flat. (nV)
A_{VOL}	**Open Loop Voltage Gain** — The ratio of the output signal voltage to the differential input signal voltage, with no feedback applied. (dB or V/mV)
	Oscillator Control Sensitivity — The ratio of the change in oscillator frequency to the change in control voltage causing it.
	Oscillator Pull-In Range — The range of free-running frequency over which the oscillator is locked to the incoming signal.
O	**Output.**
	Output Common Mode Voltage — The arithmetic mean of the two output voltages for devices with differential outputs.
I_{OH}	**Output High Current** — The current flowing out of an output which is in the HIGH state.
V_{OH}	**Output HIGH Voltage** — The minimum voltage at an output terminal for the specified output current I_{OH} and at the minimum value of V_{CC}.
V_{OL}	**Output Low Voltage** — The maximum voltage at an output terminal sinking the maximum specified load current I_{OL} and at the minimum value of V_{CC}.
Z_O	**Output Impedance** — The equivalent impedance seen looking into the output terminal. (Ω)
I_{CEX}	**Output Leakage Current** — The leakage current into the output transistor at the specified output voltage potential for uncommitted or open-collector outputs. (μA)
I_{OL}	**Output LOW Current** — The current flowing into an output which is in the LOW state.

GLOSSARY (Cont.)

e_{no}	Output Noise Voltage – The rms value of the noise voltage measured at the output with constant load current and no input ripple. (μV)
I_{OZH}	Output Off Current HIGH – The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.
I_{OZL}	Output Off Current LOW – The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.
	Output Offset Voltage – The voltage difference between the two outputs with both inputs grounded.
R_O	Output Resistance – The small signal ac resistance seen looking into the output with no feedback applied and the output dc voltage near zero. For comparators, it is the resistance seen looking into the output with the dc output level at the logic threshold. (Ω)
	Output Saturation Voltage – The dc voltage between output and ground in the saturated condition.
I_{SC}	Output Short Circuit Current – The current flowing out of an output which is in the HIGH state when that output is short circuited to ground (or other specified potential).
I_{SINK}	Output Sink Current – The maximum current into the collector of an open-collector device. (mA)
V_{OUT}	Output Voltage – The voltage present at the output terminal referred to ground. (V)
ΔV_{OUT}	Output Voltage Range – The range of output voltages over which the specifications apply. (V)
$\pm V_{OUT}$	Output Voltage Swing – The peak output voltage swing, referred to zero, that can be obtained wihtout clipping the output voltage waveform. (V)
	Overshoot – The difference between the peak amplitude of the output and the final value of the output divided by the output times 100%. (%)
$I_{OUT(Pk)}$	Peak Output Current – The maximum current delivered by the device for a period too short for thermal protection to be activated. (A)
	Phase Margin – The difference between 180° and the phase shift at the frequency where the open loop gain equals unity.
V_{T+}	Positive-going Threshold Voltage – The input voltage of a variable threshold device that is interpreted as a V_{IH} as the input transition rises from below $V_{T-(MIN)}$.
t_{PW}	Pulse Width – The time between the leading and trailing edges of a pulse.
	Power Bandwidth The maximum frequency at which the maximum output can be maintained without significant distortion.
	Power Consumption – The dc power required to operate the device under no load conditions.
$P_{D(MAX)}$	Power Dissipation (Max) – The maximum power that can be dissipated in the device with a given heat sink beyond which the device may not perform to specification. (mW)
I_{SS}	Power Supply Current – The current required from the power supply to operate the amplifier with no load and no signal applied. (mA)
PSRR	Power Supply Rejection Ratio – The ratio of the change in input offset voltage to the change in power supply voltage producing it. (μV/V)
	Power Supply Sensitivity – The ratio of the change of a specified parameter to the change in supply voltage.
t_{pd}	Propagation Delay – The time interval between application of an input voltage step and its arrival at the output.
I_Q	Quiescent Current – That part of a regulator input current that is not delivered to the load. (mA)
	Quiescent Output Current – The output current with no signal applied to the input.
I_{REF}	Reference (Control) Current – The current drawn or supplied by the reference (control) terminal. (μA)
V_{REF}	Reference Voltage – The output of the reference amplifier measured with respect to the negative supply. (V)
I_{RIN}	Response Control Input Current – The current flowing out of the response control pin that is available to charge the response control capacitor.
t_{resp}	Response Time – The interval between the application of an input step function and the time when the output voltage crosses the logic threshold level. (ns)
t_{rr}	Reverse Recovery Time – The time taken for the reverse recovery current to fall to a specified value after removal of the reverse bias under specified conditions. (ns)
t_R	Release Time – The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

GLOSSARY (Cont.)

Symbol	Term and definition
	Ripple Rejection – The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage. (dB)
t_r	**Rise Time** – The time interval required for a signal to rise from 10% to 90% of its final amplitude. (ns or μs)
	Settling Time – The time from a step change of input to the time the corresponding output settles to within a specified percentage of the final value. (ns)
t_s	**Set-up Time** – The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.
	Short-Circuit Current Limit – The output current of a regulator with the output shorted to common (ground). (mA)
	Short-Circuit Load Current – The maximum output current which the device will provide into a short-circuit.
SR	**Slew Rate** – The maximum rate of change of output under large signal conditions. (V/μs)
	Standby Current Drain – The supply current drawn by a regulator with no output load and no reference voltage load (see Quiescent Current).
t_s	**Storage Time** – The propagation delay due to stored charge in the transistor. (ns)
	Strobe Activation Voltage – The voltage applied to the strobe terminal beyond which the device does not respond to the conditions at the input terminals. (V)
I_{Strobe}	**Strobe Current** – The maximum current taken by the strobe terminal during activation. (μA)
	Strobe Release Time – The time required for the outputs to rise to the logic threshold voltage after the strobe terminal has been activated.
	Strobed Output Level – The dc output voltage, independant of input voltage, with the voltage on the strobe terminal in excess of the strobe activation voltage. (V)
I_{CC}	**Supply Current** – The current flowing into the V_{CC} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst case operation.
	Supply Regulation – The change in internal device supply voltage for a specified change in external power supply voltage.
V_{CC}	**Supply Voltage** – The range of power supply voltage over which the device is guaranteed to operate within the specified limits.
	Supply Voltage Rejection Ratio – See Power Supply Rejection Ratio.
	Switching Speed – See Propagation Delay.
t_{PLH}	The propagation delay time from an input change to an output LOW-to-HIGH transition.
t_{PHL}	The propagation delay time from an input change to an output HIGH-to-LOW transition.
	Temperature Coefficient – See Average Temperature Coefficient of specific parameter.
$\Delta V_{OUT}/\Delta T_A$	**Temperature Stability** – The percentage change in output voltage over a specified ambient temperature range (V/°C)
	Terminating Resistance – The resistance normally used to provide a termination to a transmission line.
V_{TH}	**Threshold Voltage** – The input voltage at which the output logic level changes state. (V)
f_{MAX}	**Toggle Frequency/Operating Frequency** – The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.
THD	**Total Harmonic Distortion** – The rms value of the harmonic content of a signal expressed as a percentage of the rms value of its fundamental.
	Transient Response – The closed loop step function response of the circuit under small signal conditions.
	Transition Time, HIGH to LOW Output – See Fall Time.
	Transition Time, LOW to HIGH Output – See Rise Time.
t_{PHL}	**Turn-on Time** – See Propagation Delay Time, HIGH to LOW Output. (ns)
f_t	**Unity Gain Bandwidth** – The frequency at which the open loop gain is reduced to unity. (MHz)
V_{TH+}	**Upper Threshold Voltage** – The input voltage that causes the output to change logic stage, when the input voltage is increasing in a device with hysteresis.
A_V	**Voltage Gain** – The ratio of the output voltage to the input voltage under small signal conditions. For comparators, it is the ratio of the change in output voltage to the change in voltage between the input terminals, with the dc output in the vicinity of the logic threshold. (dB or V/mV)

SALES OFFICES AND REPRESENTATIVES

SOUTHWEST AREA
Advanced Micro Devices
9595 Wilshire Boulevard
Suite 401
Beverly Hills, California 90212
Tel (213) 278-9700
(213) 278-9701
TWX 910-490-2143

Advanced Micro Devices
1414 West Broadway Road
Suite 239
Tempe, Arizona 85282
Tel (602) 244 9511
TELEX 668-325
TWX 910 951-4216

Advanced Micro Devices
1201 Dove Street
Suite 250
Newport Beach, CA 92660
Tel (714) 752-6262

Advanced Micro Devices
13771 No Central Expy
Suite 1008
Dallas, Texas 75243
Tel (214) 234 5886
TWX 910 867-4795

NORTHWEST AREA
Advanced Micro Devices
3350 Scott Boulevard
Suite 1002
Santa Clara, CA 95051
Tel (408) 727-1300

Advanced Micro Devices
7100 Broadway
Bldg 6, Penthouse
Suite O
Denver, CO 80221
Tel (303) 427-3307
TWX 910-931-2562

Advanced Micro Devices
6443 S W Beaverton Highway
Suite 410
Portland, OR 97221
Tel (503) 292-2666
TWX 910-464-4792

MID-AMERICA AREA
Advanced Micro Devices
2625 Butterfield Road
Suite 225N
Oak Brook, Illinois 60521
Tel (312) 323-9600
(312) 323-9601
TWX 910-254-2295

Advanced Micro Devices
8009 34th Ave S
Bloomington, Minnesota 55420
Tel (612) 854-6500
(612) 854-6520

Advanced Micro Devices
Commerce Center
1831 N W Professional Plaza
Suite 204
Columbus, OH 43220
Tel (614) 457-7766

Advanced Micro Devices
33150 Schoolcraft
Livonia, Michigan 48150
Tel (313) 425 3440
TWX 810-242-8777

MID-ATLANTIC AREA
Advanced Micro Devices
99 Powerhouse Road
Suite 303
Roslyn Heights, N Y 11577
Tel (516) 484-4990
(516) 484-4991
TWX 510-223-0649

Advanced Micro Devices
6806 Newbrook Ave
E Syracuse, N Y 13057
Tel (315) 437-7546
TELEX 93-7201

Advanced Micro Devices
2 Kilmer Road
Edison, New Jersey 08817
Tel (201) 985-6800

NORTHEAST AREA
Advanced Micro Devices
300 New Boston Park
Woburn, Massachusetts 10801
Tel (617) 933-1234

SOUTHEAST AREA
Advanced Micro Devices
6100 Baltimore National Pike
Baltimore MD 21228
Tel (301) 744-8233

Advanced Micro Devices
1001 N W 62nd Street
Suite 409
Ft Lauderdale, FL 33309
Tel (305) 771-6510
TWX 510-955-9490

Advanced Micro Devices International Sales Offices

BELGIUM
Advanced Micro Devices
Avenue de Tervueren, 412
bte 9
1150 Brussels, Belgium
Tel (02) 771 9993
TELEX 61028

FRANCE
Advanced Micro Devices, S A
Silic 314
74, Rue D Arcueil
94588 Rungis Cedex, France
Tel (1) 686-91-86
TELEX 202053

GERMANY
Advanced Micro Devices
Mikro Elektronik GmbH
Rosenheimerstr. 139
D-8000 Muenchen 80
West Germany
Tel (089) 401976
TLX 0523883 (AMD D)

Advanced Micro Devices
Mikro Elektronik GmbH
Buro Sudwestdeutschland
Robert-Leicht-Strasse 128
D-7000 Stuttgart-Vaihingen
West Germany
Tel 0711-681001

JAPAN
Advanced Micro Devices K K
Dai-San Hoya Building
1-8-17, Kamitakaido
Suginami-ku, Tokyo 168 Japan
Tel (03) 329-2751
TLX 2324064

UNITED KINGDOM
Advanced Micro Devices U K Ltd
16 Grosvenor Place
London SW1X 7HH England
Tel (01) 235-6380
(01) 235-6388
(01) 235-6389
TELEX 88-68-33

International Sales Representatives and Distributors

AUSTRALIA
A J Ferguson Pty Ltd
44 Prospect Rd
Prospect, S Australia 5082
Tel (8) 269-1244
TELEX 82635

R and D Electronics
Post Office Box 206
Burwood 3125
Australia
Tel (03) 2888232
TLX AA33288

R and D Electronics
P O Box 57
Crows Nest NSW 2065
Sydney, Australia
Tel 4395488
TLX (790) 25468

AUSTRIA
Elbatex GmbH
Endresstrasse 54
A-1238 Wien
Austria
Tel (0222) 88 56 11
TWX 01 3128

BELGIUM
MCA Tronix
62 Route Du Condroz
4200 Dugree Belgium
Tel 041-362780
TELEX 42052

BRAZIL
Icotron S A
Ind de Componentes Electronicos
05110-Av Mutinga 3650-6 D Andar
Pirituba Sao Paulo
Caixa Postal 1375
Brazil
Tel (011) 261-0211
TLX (011) 22274 ICO BR

DENMARK
Advanced Electronic of Denmark
Godthabsvej 7
DK-2000-Copenhagen
Denmark
Tel (45) (1) 19 44 33
TLX 055 - 224 31 - Advel DK

FINLAND
Komdel Oy
Box 32
02211 Espoo-21
Finland
Tel (0) 88 50 11

Shipping
Maapalonkatu 8
02210 Espoo-21
Finland

FRANCE
A2M
18 Avenue Dutartre
78150 Le Chesnay
France
Tel (1) 955-32-49
TLX 698 376 (AMM)

Radio Television Francaise
73 Av Ch De Gaulle
92202 Neuilly-sur-Seine
Tel 747-11-01
TELEX 611985

GERMANY
Cosmos Electronic GmbH
Hegelstrasse 16
D-8000 Muenchen 83
West Germany
Tel (089) 602088
TELEX 0-522545

EBV-Elektronik
Gabriel Max Str 72
D-8000 Muenchen 90
Tel 089-644055
TELEX 0-524535

EBV-Elektronik
Oststr 129
D-4000 Duesseldorf
Tel 0211-84846
TELEX 0-8587267

EBV-Elektronik
In der Meineworth 9A
D-3006 Burgwedel 1
Tel 05139-4570

EBV-Elektronik
Myliusstr 54
D-6000 Frankfurt 1
Tel 0611-720416
TELEX 0-413590

EBV-Elektronik
Alexanderstr 42
D-7000 Stuttgart 1
Tel 0711-247481
TELEX 0-722271

Elbatex GmbH
Cackenstrasse 24
D-7100 Heilbronn
West Germany
Tel 07131-89001
TELEX 0-728362

Nordelektronik Vertriebs GmbH
Bahnhofstr 14
D-2301 Kiel-Raisdorf
West Germany
Tel 04307-5483

Nordelektronik Vertriebs GmbH
Harksheiderweg 238-240
2085 Quickborn
D-2085 Quickborn
West Germany
Tel (04106) 4031
TELEX 0-214299

HOLLAND
Arcobel BV
Van Almondestraat 6
B O Box 344
Oss
Holland
Tel 04120-24200
04120-27574
TELEX 50835

HONG KONG
Ace Enterprise
Suite 1212
363 Nathan Road
Kowloon, Hong Kong
Tel 3-302925
3-302927

INDIA
Zenith Electronics
541 Panchratna
Mama Parmanand Marg
Bombay 400004
India
Tel 384214
TELEX 0113152

FEGU
260 Sheridan Ave
Palo Alto, CA 94306
Tel (415) 493-1788
TELEX 345-599

Sujata Sales and Exports Ltd
11-2 Bajaj Bhavan
Nariman Point
Bombay 21, India
Tel 3254275
TLX 011-3855

American Components
1601 Civic Center Drive
Santa Clara, CA 95050
CABLE ELCOMP
TLX 352073

Ashwin Enterprises
28, IIIrd Cross
Shankarapuram
Bangalore 56004
India
Tel 62120

Ashwin Enterprises
86 Dix Highway
Dix Hills
New York, NY 11746
Tel (516) 667-4819

Hindustan Semiconductor
24 Sayed Abdulla
Brelvi Road
Bombay India
Tel 818105 812772
TLX (953) 112726 APAR IN

IRELAND
ITT Electronic Services
142 Phibsborough Rd
Phibsborough
Dublin
Ireland

ISRAEL
Talviton Electronics
P O Box 21104
9 Baltimor Street
Tel-Aviv, Israel
Tel 444572
TELEX VITKO 33400

RN Electronics Agencies Ltd
103 Hagolan Street
Ramat Hachayal, Israel
P O B 10205, 10299 Zahala
Tel 03-471658
TLX 32470 341730

ITALY
AMD - Elettronica S R L
Via Pascoli 70/4
Ground Floor
I-20133 Milan, Italy
Tel (2) 2364284
TELEX AMD Elettronica
Via Pascoli 70-TF2364284
Via Milan P O TELEX 311250 PPMI

Indelco, S R L Rome
Via C Colombo, 134
I-00147 Rome Italy
Tel 5140722
TELEX 611517

Indelco, S R L Milan
Via S Simpliciano 2
I-20121 Milan Italy
Tel 862963

JAPAN
Advanced Technology Corporation
of Japan
Tashi Bldg , 3rd Floor
No 8 Minami Motomachi
Shinjuku-ku, Tokyo 160 Japan
Tel (03) 265 9416
TELEX (781) 22180

Dainichi Electronics
Kohraku Building
1 8 1-Chome Koraku
Bunkyo-ku, Tokyo Japan
Tel (03) 813-6876

ISI Ltd
8-3 4-Chome Iidabashi
Chiyoda-ku, Tokyo 102 Japan
Tel (03) 264 3301

Kanematsu-Denshi K K
Takanawa Bldg , 2nd Floor
19-26 3-Chome Takanawa
Minato-ku, Tokyo 108 Japan

Microtek Inc
No Building
7-9-17
Nishishinjuku
Shinjuku-Ku Tokyo 160 Japan
Tel 03-363 2317
TWX J28497

Dainichi Electronics
Kintetsu-Takama Building
38-3 Takama-Cho
Narashi-Japan 630

KOREA
Cassia Electronics Products, Inc
Woodside Financial Center
2055 Woodside Road
Suite 160
Redwood City, CA 94061
Tel
TWX

Caduceus Limited
Room 508
Sindo Building
65-4, 2-Ka, Chung Mu Ro
Chung-ku, Seoul - Korea
Tel 777-2325
TLX K26453 NAMSTRA

NORWAY
A S Kjell Bakke
Nygata 48
P O Box 143
2011 Stroemmen
Norway
Tel (02) 715350
715351
TLX 19407

SOUTH AFRICA
South Continental Devices (Pty) Ltd
Suite 516, 5th Floor
Randover House
Cor Hendrik Verwoerd
Dover Rd Randburg, Tvl
Mail address P O Box 56420
Pinegowrie 2123, South Africa
Tel 48-0515
TELEX 83324

SOUTH AMERICA
Intectra
2349 Charleston Road
Mountain View, California 94043
Tel 967-8818
967-8825
CABLE INTECTRA

SPAIN
Electronic Services S A
Adv de Ramon y Cajal 5
Madrid 6 Spain
Tel 457-6615
TELEX 42207

Regula S A
Av Ramon y Cajal 5
Madrid-16 Spain
Tel 459 33 00
459 33 04
459 33 08
TELEX 42 207

Sertem
Julio Urquijo 12
Bilbao-14 Spain
Tel 435 72 00
435 72 09

Regula S A
Avda Baro 19
Barcelona Spain
Tel 386 19 58

SWEDEN
Svenska Teleindustri
Box 502
162 05 Vallingby Sweden
Tel 08-830435
TWX 13033

SWITZERLAND
Kurt Hirt AG
Thurgauerstr 74
CH-8048 Zurich
Tel 00411-512121
TELEX 0045-53461

TAIWAN
Multitech International Corp
2nd Floor
977 Min Shen E Road
Taipei 105 Taiwan R O C
Tel 768-1232
CABLE MULTIIC

UNITED KINGDOM
Dage International Ltd
European Division
Haywood House
High Street
Pinner, Middlesex, HA5 5QA England
Tel 01-868-0024
TELEX 24506

Cramer Components Ltd
Hawke House
Green Street
Sunbury on Thames
Middlesex-England
Tel Sunbury (76) 85577
TLX 923592

ITT Electronic Services
Edinburgh Way
Harlow Essex
CM20 2DE
England
Tel Harlow 26811

Memec Ltd
Thames Park Industrial Estate
Thames
Oxon OX9 3RS
England
Tel (084 421) 3146
TLX 837508

Quarndon Electronics
(Semiconductors) Ltd
Slack Lane
Derby DE3 3ED England
Tel Derby 32651
TELEX 37163

U.S. and Canadian Sales Representatives

ALABAMA
Electronic Manufacturers Agents
2309 Starmount Circle S W
Huntsville, Alabama 35801
Tel (205) 533-6440
TWX 810-726 2110

CALIFORNIA
(Northern)
I^2 Incorporated
3350 Scott Boulevard
Santa Clara, California 95050
Tel (408) 988 3400
TWX 910 338 0192

Shipping
3641 Edward Avenue
Santa Clara, California 95050

(Southern)
Bestronics Inc
7827 Convoy Court
Suite 407
San Diego, California 92111
Tel (714) 278 2150
TWX 910-335 1267

CANADA (Eastern)
Vitel Electronics
3300 Cote Vertu, Suite 203
St Laurent, Quebec
Canada H4R 2B7
Tel (514) 331 7393
TWX 610-421 3124
TLX 05-821762

Vitel Electronics
1 Vulcan St, Suite 203
Rexdale, Ontario
Canada M9W 1L3
Tel (416) 675 2977
TWX 610-491-3728
TLX 06-967881

Shipping
Vitel Electronics
84 Main Street
Champlain, New York 12919

CANADA (Western)
Venture Electronics
P O Box 3034
Bellevue, Washington 98009
Tel (206) 454-4594
TLX 32-8951

Shipping
1645 Rambling Lane
Bellevue, Washington 98004

COLORADO
R^2 Marketing
10018 No Regency Place
P O Box 554
Parker, Colorado 80134
Tel (303) 841-5822

CONNECTICUT
Scientific Components
350 South Main Street
Cheshire, Connecticut 06410
Tel (203) 272-2160

FLORIDA
Conley & Associates, Inc
P O Box 309
235 South Central Ave
Oviedo, Florida 32765
Tel (305) 365-3283
TWX 810-856-3520

Conley & Associates, Inc
1612 N W Second Ave
P O Box 700
Boca Raton, Florida 33432
Tel (305) 395-6108
TWX 510 953-7548

Conley & Associates, Inc
7515 North Armenia Avenue
Tampa, Florida 33604
Tel (813) 933-1759

GEORGIA
Electronic Manufacturers Agents
2800 Forest Vale Lane
Suite VI
Norcross, Georgia 30093
Tel (404) 448 2921

ILLINOIS
Oasis Sales, Inc
2250K Landmeier Road
Elk Grove Village, Illinois 60007
Tel (312) 640-1850
TWX 910-222-2170

INDIANA
C-S Electronic Sales, Inc
2122-A Miami Street
South Bend, Indiana 46613
Tel (219) 291 6258
TWX 810-299-2535

C-S Electronic Sales, Inc
1157 B South Jackson
Frankfort, Indiana 46041
Tel (317) 659-1874

IOWA
Lorenz Sales, Inc
5270 No Park Pl N E
Cedar Rapids, Iowa 52402
Tel (319) 393 6912

KANSAS
Kebco Manufacturers
7070 West 107th Street
Suite 160
Overland Park, Kansas 66212
Tel (913) 649-1051
TWX 910-749 4077

MARYLAND
Burgin Kreh Associates, Inc
6100 Baltimore National Pike
Baltimore, Maryland 21228
Tel (301) 788 5200
TWX 710 862 1450

MICHIGAN
S A I Marketing Corp
P O Box N
Brighton, Michigan 48116
Tel (313) 227-1786
TWX 810 242 1518

Shipping
First Federal Bank Building
Suite 109
9880 E Grand River Avenue
Brighton, Michigan 48116

MISSOURI
Kebco Manufacturers
75 Worthington Drive
Maryland Heights, Missouri 63043
Tel (314) 576-4111

NEW MEXICO
The Thorson Company
2201 San Pedro N E
Suite 107, Building 2
Albuquerque, New Mexico 87110
Tel (505) 265 5655
TWX 910 989-1174

NEW YORK
Ossmann Component Sales Corp
280 Metro Park
Rochester, New York 14623
Tel (716) 424 4460
TWX 510-253-7685

Ossmann Component Sales Corp
154 Pickard Building
Syracuse, New York 13211
Tel (315) 455-6611
TWX 710 541-1522

NORTH CAROLINA
Burgin Kreh Associates, Inc
P O Box 19510
Raleigh, North Carolina 27609
Tel (919) 781-1100
Shipping
3901 Barrett Drive
Raleigh, North Carolina 27609

OHIO
Dolfuss Root & Co
13477 Prospect Road
Strongsville, Ohio 44136
Tel (216) 238 0300
TWX 810 427-9148

Dolfuss Root & Co
354 Silvertree Lane
Centerville, Ohio 45459
Tel (513) 433 6776

PENNSYLVANIA
(Western)
Bacon Electronic Sales
115 South High Street
Waterford, Pennsylvania 16441
Tel (814) 796 2381

(Eastern)
GCM Associates
1014 Bethlehem Pike
Erdenheim, Pennsylvania 19118
Tel (215) 646-7535
TWX 510-661 0607

TENNESSEE
(Western)
Burgin Kreh Associates, Inc
350 E Race Street
Kingston, Tennessee 37763

(Eastern)
Burgin Kreh Associates, Inc
P O Box 268
12 Skyline Dr
Kingston Heights
Kingston, Tennessee 37763
Tel (615) 690 6100

TEXAS
Bonser-Philhower Sales
13777 N Central Expressway
Suite 212
Dallas, Texas 75243
Tel (214) 234 8438

Bonser Philhower
3300 Chimneyrock, Suite 208
Houston, Texas 77056
Tel (713) 783 0063

UTAH
R^2
940 W 2100 So
Salt Lake City, Utah 84120
Tel (801) 972 5646
TWX 910 925 5607

VIRGINIA
Burgin Kreh Associates, Inc
P O Box 4254
5521 Fort Avenue
Lynchburg, Virginia 24502
Tel (804) 239 2626

WASHINGTON
Venture Electronics
P O Box 3034
Bellevue, Washington 98009
Tel (206) 454 4594
TELEX 32 8951

Shipping
1645 Rambling Lane
Bellevue, Washington 98004

1/10/79

U.S. AND CANADIAN STOCKING DISTRIBUTORS

ALABAMA
Hamilton/Avnet Electronics
805 Oster Dr. N.W.
Huntsville, Alabama 35805
Tel (205) 533-1170

Hall-Mark Electronics
4739 Commercial Drive
Huntsville, Alabama 35805
Tel (205) 837-8700

ARIZONA
Liberty Electronics
8155 North 24th Avenue
Phoenix, Arizona 85021
Tel (602) 249-2232

Hamilton/Avnet Electronics
2615 S. 21st Street
Phoenix, Arizona 85034
Tel (602) 275-7851
TWX 910-951-1535

CALIFORNIA
Avnet Electronics
350 McCormick Avenue
Irvine Industrial Complex
Costa Mesa, California 92626
Tel (714) 754-6084
TWX 910-595-1928

Bell Industries
1161 N. Fairoaks Avenue
Sunnyvale, California 94086
Tel (408) 734-8570
TWX 910-339-9378

Elmar Electronics
2288 Charleston Road
Mountain View, California 94042
Tel (415) 961-3611
TWX 910-379-6437

Hamilton Electro Sales
10912 W. Washington Blvd
Culver City, California 90230
Tel (213) 558-2100
(714) 522-8220
TWX 910-340-6364
910-340-7073
TELEX 67-36-92

Hamilton Avnet Electronics
1175 Bordeaux
Sunnyvale, California 94086
Tel (408) 743-3300
TWX 910-339-9332

Hamilton Avnet Electronics
8917 Complex Drive
San Diego, California 92123
Tel (714) 279-2421
TELEX 69-54-15

Liberty Electronics
9525 Chesapeake Drive
San Diego, California 92123
Tel (714) 565-9171
TWX 910-335-1590

Schweber Electronics
17811 Gillette
Irvine, California 92714
Tel (213) 537-4320
TWX 910-595-1720

Liberty Electronics
124 Maryland Avenue
El Segundo, CA 90545
Tel (213) 322-8100
TWX 910-348-7140
910-348-7111

CANADA
Hamilton Avnet Electronics
2670 Paulus
St. Laurent, Quebec, Canada H4S1G2
Tel (514) 331-6443
TWX 610-421-3731

Hamilton Avnet Electronics
6291-16 Dorman Road
Mississauga, Ontario, Canada L4V1H2
Tel (416) 677-7432
TWX 610-492-8867

Hamilton Avnet Electronics
1735 Courtwood Crescent
Ottawa, Ontario, Canada K2C3J2
Tel (613) 226-1700
TWX 610-562-1906

RAE Electronics
1629 Main Street
Vancouver, British Columbia,
Canada V6A2W5
Tel (604) 687-2621
TELEX 0454550

Future Electronics
5647 Ferrier Street
Montreal, Quebec, Canada H4P2K5
Tel (514)735-5775
TWX 610-421-3251
05-827789

Future Electronics
4800 Dufferin Street
Downsview, Ontario
Canada M3H 5S9
Tel (416) 663-5563

Future Electronics
Baxter Centre
1050 Baxter Rd
Ottawa, Ontario
Canada K2C 3P2
Tel (613) 820-9471

COLORADO
Elmar Electronics
6777 E. 50th Avenue
Commerce City, Colorado 80022
Tel (303) 287-9611
TWX 910-936-0770

Hamilton/Avnet Electronics
5921 N. Broadway
Denver, Colorado 80216
Tel (303) 534-1212
TWX 910-931-0510

Bell Industries
8155 W. 48th Avenue
Wheatridge, Colorado 80033
Tel (303) 424-1985
TWX 910-938-0393

CONNECTICUT
Hamilton/Avnet Electronics
643 Danbury Road
Georgetown, Connecticut 06829
Tel (203) 762-0361

Schweber Electronics
Finance Drive
Commerce Industrial Park
Danbury, Connecticut 06810
Tel (203) 792-3500

Arrow Electronics
295 Treadwell Street
Hamden, CT 06514
Tel (203) 248-3801
TWX 710-465-0780

Wilshire Electronics
2554 State Street
Hamden, Connecticut 06517
Tel (203) 281-1166
TWX 710-465-0747

FLORIDA
Arrow Electronics
115 Palm Road N.W.
Suite 10
Palm Bay, Florida 22905
Tel (305) 725-1480

Arrow Electronics
1001 N.W. 62nd St., Suite 402
Ft. Lauderdale, Florida 33300
Tel (305) 776-7790

Hall Mark Electronics
7233 Lake Ellenor Dr
Orlando, Florida 32809
Tel (305) 855-4020
TWX 810-850-0183

Hamilton Avnet Electronics
6800 N.W. 20th Ave
Ft. Lauderdale, Florida 33309
Tel (305) 971-2900

Hamilton Avnet Electronics
3197 Tech Drive North
St. Petersburg, Florida 33702

Schweber Electronics
2830 North 28 Terrace
Hollywood, Florida 33020
Tel (305) 927-0511
TWX 510-954-0304

GEORGIA
Arrow Electronics
3406 Oak Cliff Road
Doraville, GA 30340
Tel (404) 455-4054
TWX 810-757-4213
Hamilton Avnet Electronics
6700 I 85
Suite 2B
Norcross, Georgia 30071
Tel (404) 448-0800

Schweber Electronics
4126 Pleasantdale Road
Atlanta, Georgia 30340
Tel (404) 449-9170

ILLINOIS
Arrow Electronics
492 Lunt Avenue
Schaumburg, Illinois 60193
Tel (312) 893-9420

Hamilton Avnet Electronics
3901 North 25th Avenue
Schiller Park, Illinois 60176
Tel (312) 678-6310
TWX 910-227-0060

Schweber Electronics
1275 Brummel Avenue
Elk Grove Village, Illinois 60007
Tel (312) 593-2740
TWX 910-222-3453

KANSAS
Hall Mark Electronics
11870 West 91st Street
Congleton Industrial Park
Shawnee Mission, Kansas 66214
Tel (913) 888-4747
TWX 510-928-1831

Hamilton Avnet Electronics
9219 Quivira Road
Overland Park, Kansas 66215
Tel (913) 888-8900

MARYLAND
Arrow Electronics
4801 Benson Avenue
Baltimore, Maryland 21227
Tel (301) 247-5200

Hall-Mark Electronics
665 Amberton Drive
Baltimore, Maryland 21227
Tel (301) 796-9300
TWX 710-862-1942

Hamilton/Avnet Electronics
7235 Standard Drive
Hanover, Maryland 21076
Tel (301) 796-5000
TWX 710-862-1861
TELEX 8-79-68

Schweber Electronics
9218 Gaither Rd
Gaithersburg, MD 20760
Tel (301) 840-5900

MASSACHUSETTS
Arrow Electronics
96D Commerce Way
Woburn, Massachusetts 01801
Tel (617) 933-8130

Hamilton Avnet Electronics
100 East Commerce Way
Woburn, Massachusetts 01801
Tel (617) 933-8020
TWX 710-393-1201

Schweber Electronics
25 Wiggins Road
Bedford, Massachusetts 01730
Tel (617) 275-5100

Wilshire Electronics
One Wilshire Road
Burlington, Massachusetts 01803
Tel (617) 272-8200
TWX 710-332-6359

MICHIGAN
Arrow Electronics
3921 Varsity Drive
Ann Arbor, Michigan 48104
Tel (313) 971-8220
TWX 810-223-6020

Hamilton Avnet Electronics
32487 Schoolcraft
Livonia, Michigan 48150
Tel (313) 522-5700
TWX 810-242-8775

Schweber Electronics
33540 Schoolcraft
Livonia, Michigan 48150
Tel (313) 525-8100

MINNESOTA
Arrow Electronics
9700 Newton Avenue South
Bloomington, Minnesota 55431
Tel (612) 888-5522

Hall-Mark Electronics
9201 Penn Avenue South
Suite 10
Bloomington, Minnesota 55431
Tel (612) 884-9056
TWX 910-576-3187

Hamilton Avnet Electronics
7449 Cahill Rd
Edina, Minnesota 55435
Tel (612) 941-3801

Schweber Electronics
7402 Washington Avenue South
Eden Prairie, Minnesota 55343
Tel (612) 941-5280

MISSOURI
Hall-Mark Electronics
13789 Rider Trail
Earth City, Missouri 63045
Tel (314) 291-5350
TWX 910-760-0671

Hamilton Avnet Electronics
364 Brookes Lane
Hazelwood, Missouri 63042
Tel (314) 731-1144
TELEX 44-23-48

NEW JERSEY
Arrow Electronics
Pleasant Valley Road
Moorestown, New Jersey 08057
Tel (609) 235-1900

Arrow Electronics
285 Midland Ave
Saddle Brook, NJ
Tel (201) 797-5800
TWX 710-988-2206

Hamilton Avnet Electronics
10 Industrial Road
Fairfield, NJ 07006
Tel (201) 575-3390

Hamilton/Avnet Electronics
113 Gaither Drive
East Gate Industrial Park
Mt. Laurel, New Jersey 08057
Tel (609) 234-2133

Schweber Electronics
43 Belmont Drive
Somerset, New Jersey 08873
Tel (201) 469-6008
TWX 710-480-4733

Wilshire Electronics
1111 Paulison Avenue
Clifton, New Jersey 07015
Tel (201) 340-1900
TWX 710-989-7052

NEW MEXICO
Bell Industries
121 Elizabeth N.E.
Albuquerque, New Mexico 87123
Tel (505) 292-2700
TWX 910-989-0625

Hamilton/Avnet Electronics
2450 Baylor Drive S.E.
Albuquerque, New Mexico 87119
Tel (505) 765-1500

NEW YORK
Arrow Electronics
900 Broad Hollow Road
Farmingdale, New York 11735
Tel (516) 694-6800

Hamilton Avnet Electronics
167 Clay Road
Rochester, New York 14623
Tel (716) 442-7820

Hamilton Avnet Electronics
70 State Street
Westbury L.I., New York 11590
Tel (516) 333-5800
TWX 510-222-8237

Hamilton Avnet Electronics
6500 Joy Road
E. Syracuse, New York 13057
Tel (315) 437-2642
TWX 710-541-0959

Schweber Electronics
2 Town Line Circle
Rochester, New York 14623
Tel (716) 461-4000

Schweber Electronics
Jericho Turnpike
Westbury, New York 11590
Tel (516) 334-7474
TWX 510-222-9470
510-222-3660

Summit Distributors, Inc
916 Main Street
Buffalo, NY 14202
Tel (716) 884-3450
TWX 710-522-1692

Wilshire Electronics
110 Parkway South
Hauppauge
Long Island, NY 11787
Tel (516) 543-5599

Wilshire Electronics
1260 Scottsville Road
Rochester, NY 14623
Tel (716) 235-7620
TWX 510-253-5226

Wilshire Electronics
10 Hooper Road
Endwell, NY 13760
Tel (607) 754-1570
TWX 510-252-0194

NORTH CAROLINA
Arrow Electronics
1377-G South Park Drive
Kernersville, NC 27284
Tel (919) 996-2039

Hall-Mark Electronics
1208 Front Street, Building K
Raleigh, North Carolina 27609
Tel (919) 832-4465
TWX 510-928-1831

Hamilton Avnet Electronics
2803 Industrial Drive
Raleigh, NC 27609
Tel (919) 829-8030

OHIO
Arrow Electronics
6238 Cochran
Solon, Ohio 44139
Tel (216) 248-3990

Arrow Electronics
3100 Plainfield Road
Kettering, Ohio 45432
Tel (513) 253-9176
TWX 810-459-1611

Hamilton Avnet Electronics
954 Senate Drive
Dayton, Ohio 45459
Tel (513) 433-0610
TWX 810-450-2531

Hamilton/Avnet
761 Beta Drive, Suite E
Cleveland, Ohio 44143
Tel (216) 461-1400

Schweber Electronics
23880 Commerce Park Road
Beachwood, Ohio 44122
Tel (216) 464-2970

Sheridan/Cincinnati
10 Knollcrest Drive
Cincinnati, Ohio 45222
Tel (513) 761-5432
TWX 810-461-2670

OKLAHOMA
Hall Mark Electronics
4846 South 83rd E. Avenue
Tulsa, Oklahoma 74145
Tel (918) 835-8458
TWX 910-845-2290

PENNSYLVANIA
Hall Mark Electronics
458 Pike Road
Pike Industrial Park
Huntingdon Valley,
Pennsylvania 19006
Tel (215) 355-7300
TWX 510-667-1750

Schweber Electronics
101 Rock Road
Horsham, Pennsylvania 19044
Tel (215) 441-0600

TEXAS
Hall-Mark Electronics
9333 Forest Lane
Dallas, Texas 75231
Tel (214) 234-7300
TWX 910-867-4721

Hall-Mark Electronics
8000 Westglen
Houston, Texas 77063
Tel (713) 781-6100
TWX 910-881-2711

Hall-Mark Electronics
10109 McKalla Drive
Suite F
Austin, Texas 78758
Tel (512) 837-2814
TWX 910-874-2010

Hamilton Avnet Electronics
4445 Sigma Road
Dallas, Texas 75240
Tel (214) 661-8661
TELEX 73-05-11

Hamilton Avnet Electronics
3939 Ann Arbor Street
P.O. Box 42802
Houston, Texas 77042
Tel (713) 780-1771

Schweber Electronics
14177 Proton Road
Dallas, Texas 75240
Tel (214) 661-5010
TWX 910-860-5493

Schweber Electronics
7420 Harwin Drive
Houston, Texas 77036
Tel (713) 784-3600

UTAH
Bell Industries
2258 South 2700 West
Salt Lake City, Utah 84119
Tel (801) 972-6969
TWX 910-925-5686

Hamilton Avnet Electronics
1585 West 2100 South
Salt Lake City, Utah 84119
Tel (801) 972-2800

WASHINGTON
Hamilton Avnet Electronics
14212 N.E. 21st Street
Bellevue, Washington 98005
Tel (206) 746-8750
TWX 910-443-2449

Liberty Electronics
1750 132nd Avenue N.E.
Bellevue, Washington 98005
Tel (206) 453-8300

R.A.E. Industrial Electronics, Ltd
Meridian Storage Park
4653 Guide Meridian Road
Bellingham, Washington 98225

WISCONSIN
Arrow Electronics
434 W. Rawson Avenue
Oak Creek, Wisconsin 53154
Tel (414) 764-6600
TWX 910-262-1193

Hamilton Avnet Electronics
2975 Moorland Road
New Berlin, Wisconsin 53151
Tel (414) 784-4510

ADVANCED MICRO DEVICES, INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX 910-339-9280
TELEX 34-6306
TOLL FREE
(800) 538-8450

1/10/79

ADVANCED MICRO DEVICES, INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306
TOLL FREE
(800) 538-8450

AM-PUB006 1-79